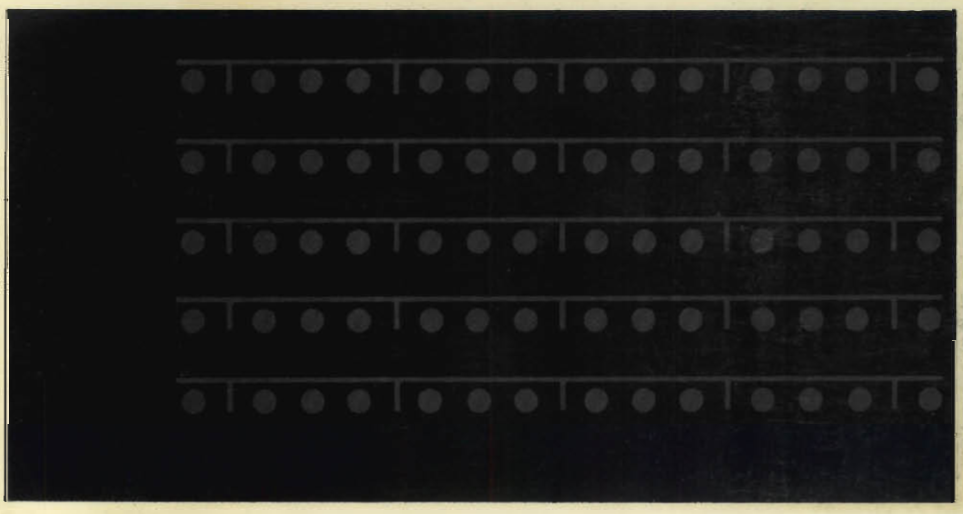
2116C COMPUTER

HEWLETT · PACKARD

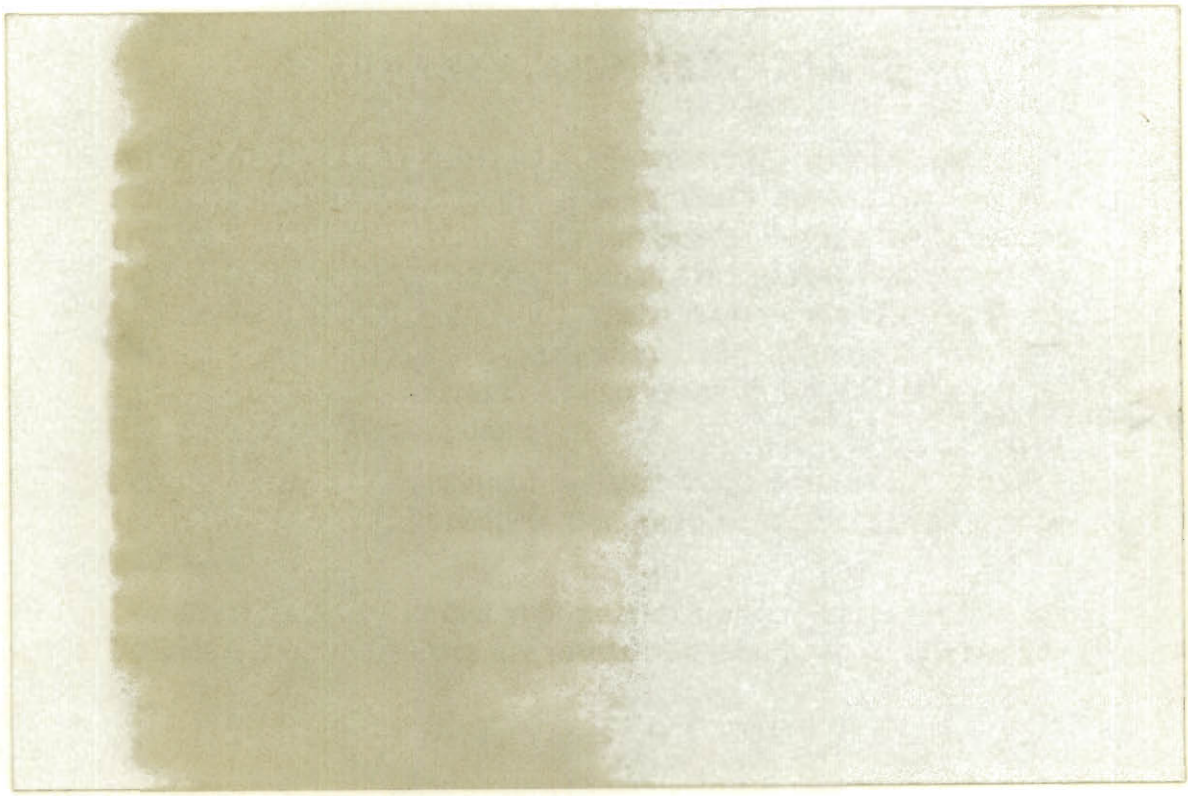


INSTALLATION AND MAINTENANCE

VOLUME 2

CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.



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2116C
COMPUTER
VOLUME TWO

UPDATING SUPPLEMENT FOR INSTALLATION AND MAINTENANCE MANUAL

15 AUG 1971

MANUAL IDENTIFICATION

Manual Serial No. Prefix: 980,998,1047A

Manual Printed: JULY 1971

Manual Part Number: 02116-91756

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change
1108A	1
1124A	1
1127A	1
1131A	1

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes
A9,A10, A19,A20	Sense Amplifier Card	5060-8320	1106, 1120, 1128	1
A302	Memory Supply Regulator Card	02116-63267	1127	1
A305	Small Heat Sink Assembly	02116-63238	–	1
A311	Transformer Assembly	02116-63225	–	1

Change 1 dated 15 August 1971.

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CHANGE	DESCRIPTION
1	a. Change 1 updates the manual to cover computers with serial number prefixes 1108A, 1124A, 1127A, and 1131A. To update the manual, remove the superseded pages listed below in the REMOVE columns and insert the new pages (attached to this updating supplement) listed in the INSERT columns.

REMOVE	INSERT	REMOVE	INSERT
Title page	Title page	–	6-34A/6-34B
Blank	A	6-35 thru 6-38	6-35 thru 6-38
xv, xvi	xv, xvi	–	6-38A/6-38B
xix, xx	xix, xx	6-39, 6-40	6-39, 6-40
1-1, 1-2	1-1, 1-2	6-43 thru 6-48	6-43 thru 6-48
2-1 thru 2-6	2-1 thru 2-6	–	6-48A/6-48B
3-11, 3-12	3-11, 3-12	6-49 thru 6-54	6-49 thru 6-54
6-5, 6-6	6-5, 6-6	7-5 thru 7-10	7-5 thru 7-10
6-9 thru 6-12	6-9 thru 6-12	–	7-108A/7-108B
6-17, 6-18	6-17, 6-18	7-265 thru 7-274	7-265 thru 7-274
6-21 thru 6-26	6-21 thru 6-26	7-279 thru 7-282	7-279 thru 7-282
6-31 thru 6-34	6-31 thru 6-34		

b. After completing step "a", check the contents of the manual against the List of Effective Pages, located on page A. When all new pages are properly inserted, discard the superseded pages. Retain this updating supplement (yellow pages) with the manual for future reference.

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VOLUME TWO

INSTALLATION AND MAINTENANCE MANUAL

MODEL 2116C COMPUTER

Serial Numbers Covered

This manual applies directly to Model 2116C Computers having serial numbers prefixed 980-, 998-, and 1047A-. When the updating supplement dated 15 August 1971 is incorporated, this manual also covers 2116C Computers having serial numbers prefixed 1108A-, 1124A-, 1127A-, and 1131A. Computers with higher prefix numbers will be covered in later updating supplements.

Options Covered

This manual covers options 005, 006, 007, and 015 as well as the basic computer. For additional information concerning options 005, 006, and 007, refer to the 12615A Installation Manual (part no. 12615-90001).

Note

To order additional copies of this manual, specify part number 02116-91756.

02116-91756

Printed: JULY 1971
Changed: 15 AUGUST 1971

LIST OF EFFECTIVE PAGES

NOTE: Pages that contain new or changed information are identified by the change date printed in the bottom corner, opposite the page number.

Dates of issue for original and change pages are:
Original . . 0 . . July 1971
Change 1 . . 1 . . 15 Aug 1971

TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 666 CONSISTING OF THE FOLLOWING:

Page No.	Change No.	Page No.	Change No.	Page No.	Change No.	Page No.	Change No.
Title	1	4-39 - 4-45	0	6-34B Blank	1	7-108B Blank	1
A	1	4-46 Blank	0	6-35	1	7-109 - 7-115	0
i - xiv	0	4-47 - 4-55	0	6-36 - 6-37	0	7-116 Blank	0
xv - xvi	1	4-56 Blank	0	6-38	1	7-117 - 7-123	0
xvii - xviii	0	4-57 - 4-59	0	6-38A	1	7-124 Blank	0
xix - xx	1	4-60 Blank	0	6-38B Blank	1	7-125 - 7-189	0
xxi	0	4-61 - 4-67	0	6-39	1	7-190 Blank	0
1-0 - 1-1	0	4-68 Blank	0	6-40 - 6-42	0	7-191 - 7-231	0
1-2	1	4-69 - 4-71	0	6-43	1	7-232 Blank	0
1-3 - 1-16	0	4-72 Blank	0	6-44	0	7-233 - 7-264	0
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3-1 - 3-10	0	5-1 - 5-15	0	6-48A	1	7-270 - 7-271	0
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3-12 - 3-29	0	6-1 - 6-4	0	6-49 - 6-54	1	7-274 - 7-277	0
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3-31 - 3-49	0	6-6 - 6-9	0	6-58 Blank	0	7-280	0
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4-31 - 4-33	0	6-21	1	7-9	0	7-288 Blank	0
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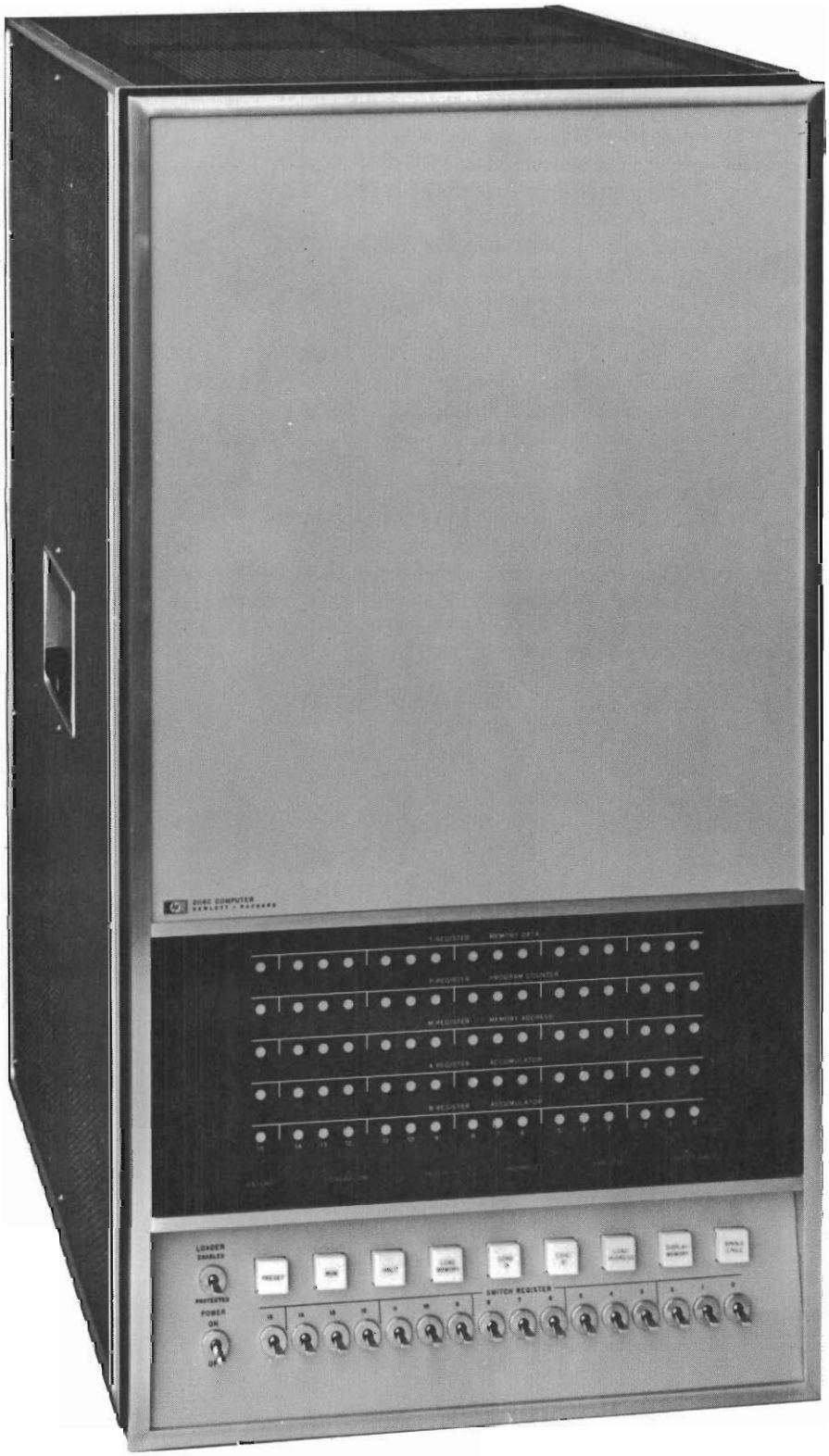

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Figure 1-1. Hewlett-Packard 2116C Computer

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. Volume Two is the second in a series of three volumes that document the Hewlett-Packard Model 2116C Computer (figure 1-1). Volume Two contains information on installation, maintenance, troubleshooting, and repair of the computer. Unless otherwise stated in future supplements, information in Volume Two is applicable to 2116C Computers having serial-number prefix 980- and higher.

1-3. Volume Two is a reference manual intended for maintenance personnel who are familiar with the circuit theory and maintenance procedures of the 2116C or similar computers in the Hewlett-Packard line. A thorough understanding of the information presented in Volume One, Specifications and Basic Operation Manual for the Model HP 2116C Computer, is essential to using and understanding the material presented in this volume.

1-4. Included in this volume are circuit theory descriptions, and testing, troubleshooting, and repair instructions, for the five major functional sections of the computer. These sections are the control, arithmetic, memory, input/output, and power supply sections (figure 1-2).

1-5. The sections and appendices of Volume Two contain the following information:

a. Section I, General Information. Section I contains general information on the physical makeup of the computer. Included are a description of the various electronic assemblies which comprise the computer, an explanation of controls and indicators, a description of identification numbers used in the computer, a description of standard accessory equipment supplied with the computer, an explanation of the principle built-in maintenance features, and a list of servicing equipment required.

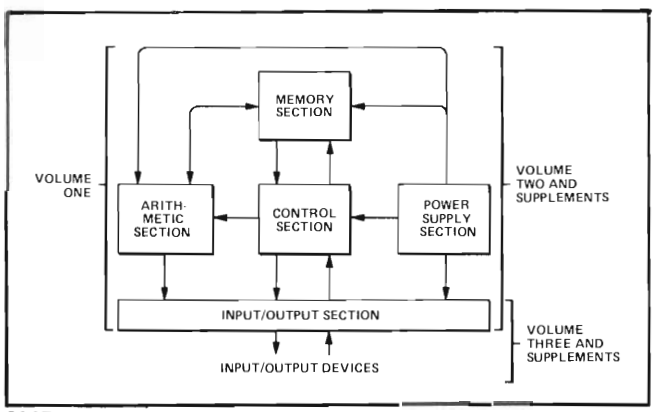

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Figure 1-2. Major Functional Sections of the 2116C Computer

b. Section II, Installation. Section II describes unpacking procedures, provides primary power data, explains initial inspection procedures, and presents instructions for installing the computer.

c. Section III, Theory of Operation. Section III describes the circuit theory of the control, arithmetic, memory, input/output, and power supply sections.

d. Section IV, Troubleshooting. Section IV presents step-by-step procedures for testing the computer. The results of these tests form the basis of fault-localizing procedures, which use servicing diagrams presented in the section. These diagrams, together with logic equations and logic diagrams in section VII, aid in the rapid location of computer faults.

e. Section V, Maintenance. Section V provides preventive-maintenance instructions and adjustment information.

f. Section VI, Replaceable Parts. Section VI contains lists and illustrations of replaceable parts. The lists give the name and part number of each part, and specify the characteristics of electronic components. The parts lists also give manufacturers' names, manufacturers' part numbers, and the total quantity of each part installed in the computer. The parts lists and total-quantity figures apply to the basic computer configuration. Parts information for optional features is covered in the manual concerned.

g. Section VII, Diagrams. Section VII consists of logic diagrams, parts location diagrams, wiring information and logic equations. Also included are definitions of the abbreviations used for signal names, and information on integrated circuit packs.

h. Appendix A, Basic Logic Symbols. Appendix A describes the logic symbols used in this manual. The explanations also apply to the logic symbols in manuals for optional devices, provided the manuals were written by Hewlett-Packard.

i. Updating Supplement. An updating supplement may be included with Volume Two. Updating supplements are used to correct errors in the existing documentation and provide additional documentation for computers having serial number prefixes other than those specified on the title page at the front of the manual.

1-6. GENERAL DESCRIPTION.

1-7. COMPUTER ASSEMBLIES.

1-8. The major electronic assemblies that make up the computer are listed in table 1-1 and shown in figure 1-3, 1-4, and 1-5. The following paragraphs describe these assemblies.

1-9. CIRCUIT CARDS. As the term is used with the 2116C Computer, a circuit card is an assembly consisting of electronic components mounted on an insulating card. An etched-foil pattern on the card makes connections between the components. The entire unit, referred to either as a circuit card or a card, plugs into a connector in the computer. A similar unit which is permanently wired to other assemblies is referred to as a board.

Table 1-1. Major Electronic Assemblies (1)

REFERENCE DESIGNATION	PART NO.	QTY	NOMENCLATURE
Card Cage Assembly			
A6	02116-6175	1	Power Fail Interrupt Card
A13	02116-63248	1	Memory Data Buffer Card
A14	02116-63212	1	Memory Address Decoder Card
A20	02116-63207 (3)	1	Sense Amplifier Card
A21	02116-63211	1	X-Y Driver/Switch Card
A22	02116-63210	1	Inhibit Driver Card
A101	02116-6208	1	Front Panel Coupler Card
A102, A103, A104, A105	02116-6026	4	Arithmetic Logic Card
A106	02116-63220	1	Timing Generator Card
A107	02116-6027	1	Instruction Decoder Card
A108	02116-6029	1	Shift Logic Card
A121	02116-63218	1	Overvoltage Protection Assembly
A201	02116-6041	1	I/O Control Card
A202	02116-6194	1	I/O Address Card
A218 (2)	02116-6047	1 (2)	Resistance Load Card
Power Supply Assembly			
A301	02116-6014	1	Logic Supply Regulator Card
A302	02116-63214 (4)	1	Memory Supply Regulator Card
A303	02116-63236	1	Capacitor Board Assembly
A304	02116-63237	1	Large Heat Sink Assembly
A305	02116-63238	1	Small Heat Sink Assembly
A306	02116-63229	1	Component Board Assembly
A307	02116-63242	1	Component Board Assembly
A308	02116-63235	1	Component Board Assembly
A309	02116-63240	1	Component Board Assembly
A310	02116-63241	1	Component Board Assembly
A311	02116-63225	1	Transformer Assembly
A312	02116-63228	1	AC Input Section
Door Assembly			
A501	02116-6043	1	Display Board Assembly
A502	02116-01115	1	Control Panel Assembly

(1) Optional assemblies are not listed.

(2) The resistance load card is installed in the lowest-numbered unused card slot between 203 and 218 inclusive. If all these slots are in use, the resistance load card is not installed.

(3) Sense amplifier card with part number 02116-63207 is interchangeable with part number 5060-8320.

(4) Computers with serial number prefix 1127A and above use a Memory Supply Regulator Card with part number 02116-63267.

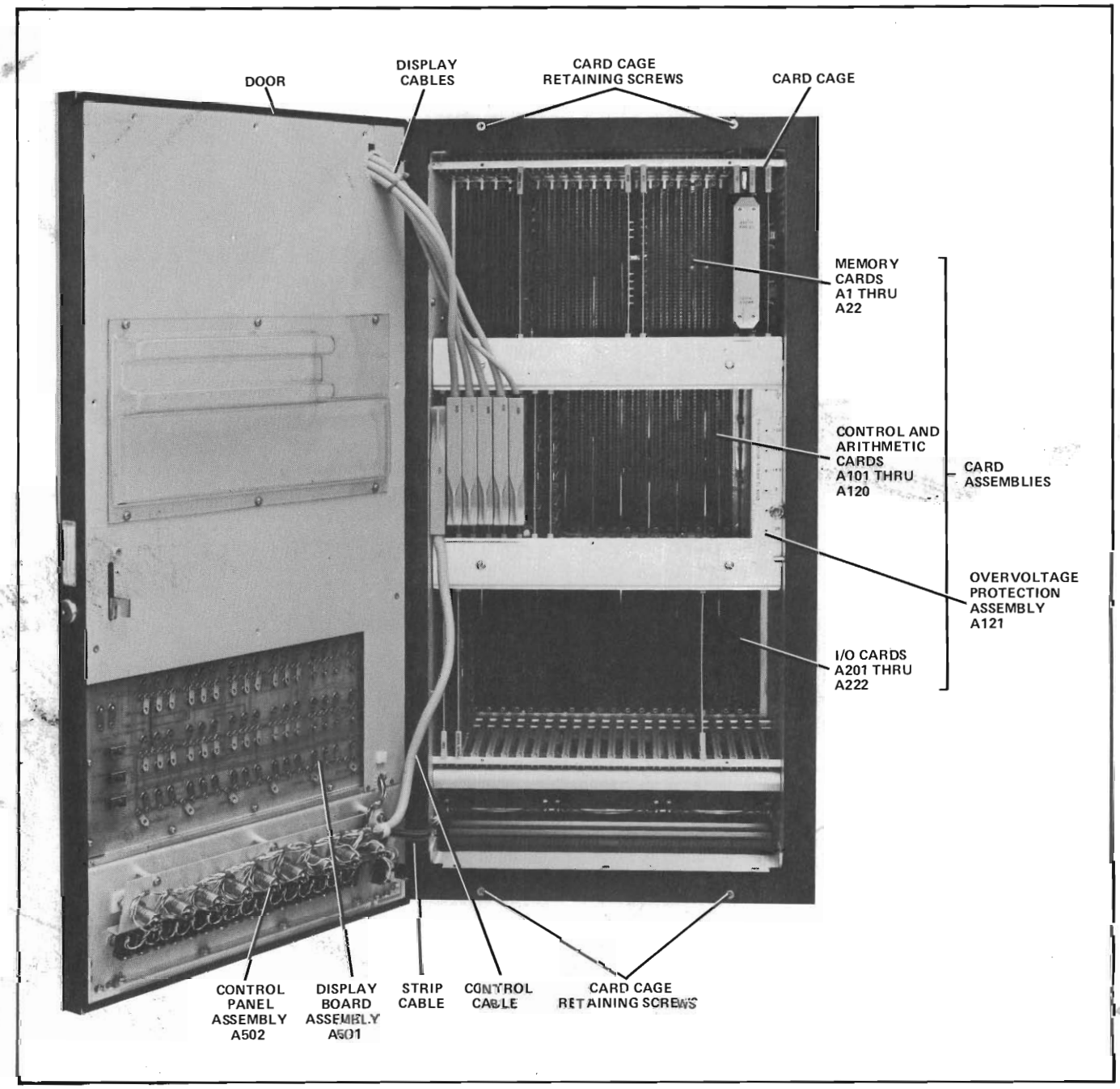

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Figure 1-3. Interior View of Computer, Card Cage Closed

1-10. The computer logic circuits are made up entirely of cards, which plug into fixed connectors in the card cage. In some cases a second connector, on the end of a flexible cable, fits on the front end of the card. Each card is assigned a reference designation beginning with the letter "A" followed by a number indicating the card-cage slot in which the card is installed. Each card also has a part number. If more than one card of a given type is used, each of the cards has the same part number but a different reference designation.

1-11. Cards with reference designations A1 through A22 contain principally the memory-section circuits, and the cards are installed in the top row of slots in the card cage. Cards A101 through A120 containing principally the control-section and arithmetic-section circuits, are situated in the center row of card-cage slots. Cards A201 through A222, containing principally I/O-section circuits, are installed in the bottom row of slots.

1-12. The cards shown in figure 1-3 are those used for the basic computer configuration. For optional features, additional cards may be installed in the card cage. Figure 7-2 shows the complete card complement.

1-13. Two additional cards, not shown in figure 7-2 but part of the basic computer configuration, are situated in the power supply at the back of the computer cabinet.

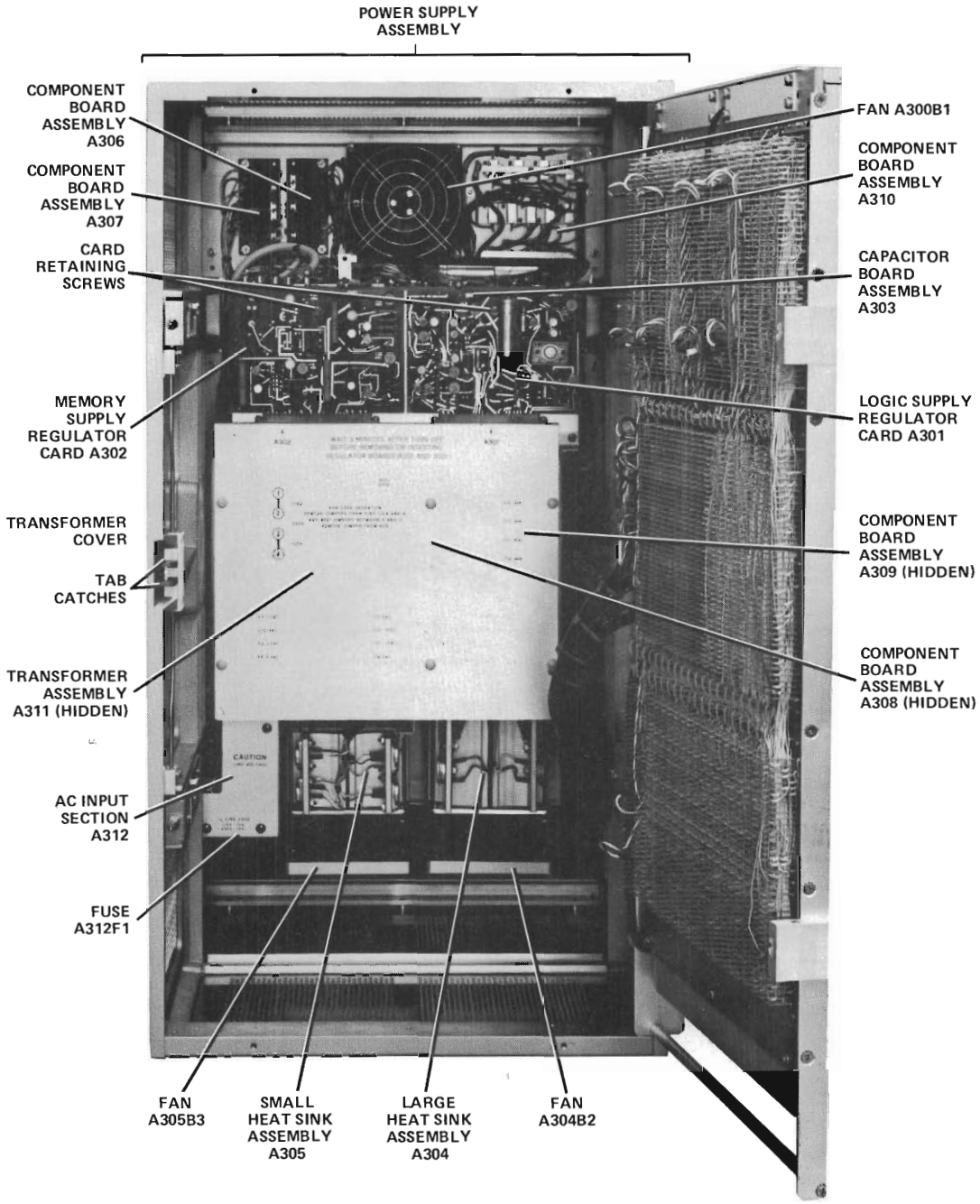

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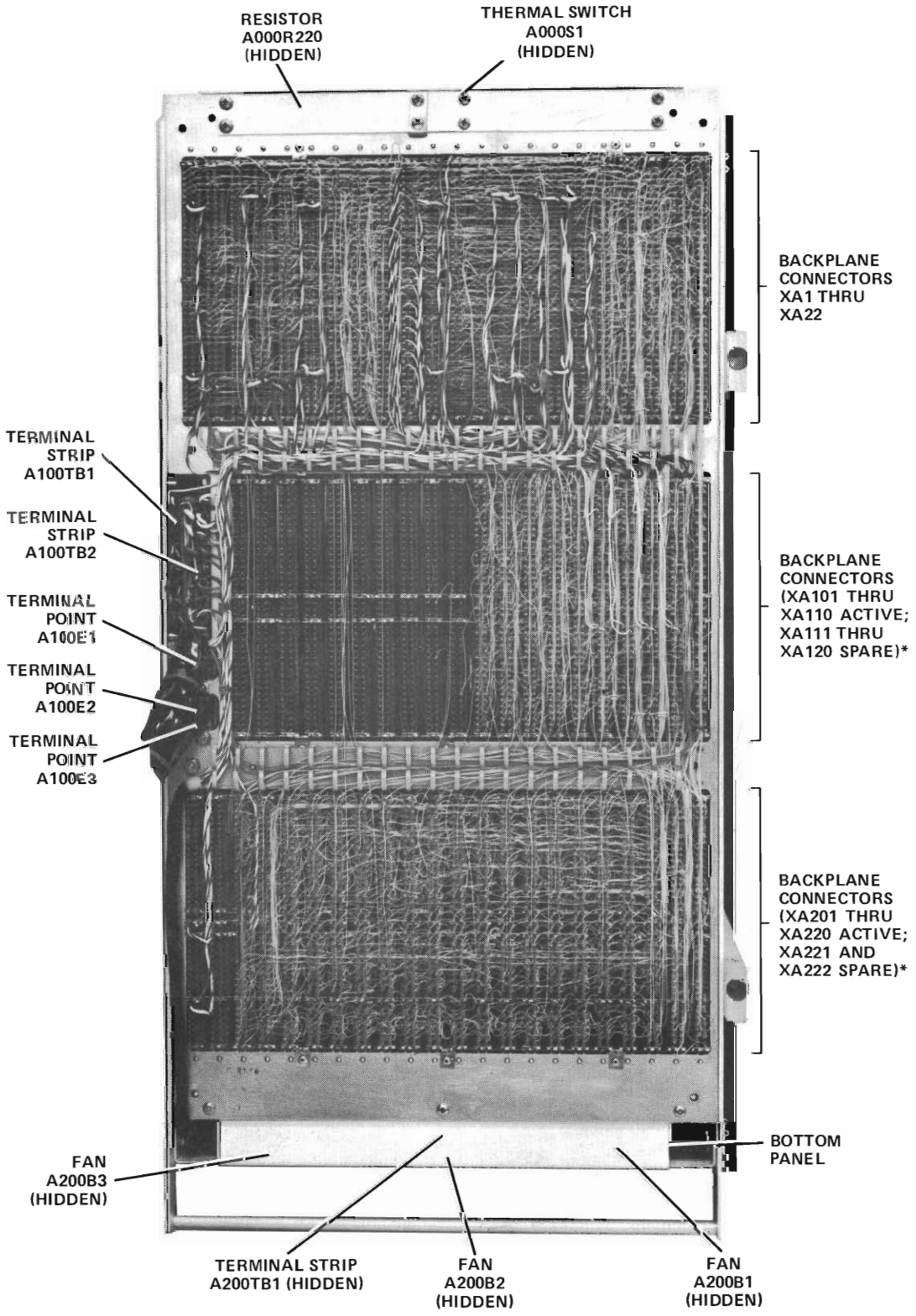
Figure 1-4. Interior View of Computer, Card Cage Open



* SOME BACKPLANES ARE EQUIPPED WITH FILLER PLATES INSTEAD OF THE SPARE CONNECTORS WHICH ARE SHOWN.

2107-4A

Figure 1-5. Rear View of Card Cage

1-14. DISPLAY BOARD ASSEMBLY. The display board assembly, reference designation A501, provides a visual indication of computer operating conditions and displays the contents of the principal computer registers. The unit mounts in the computer door assembly, as shown in figures 1-3 and 1-6. Connection to the display board assembly is made by the display cables (figure 1-3), which plug onto the front ends of arithmetic-section and control-section cards in the card cage. An additional cable, referred to as the strip cable, connects the display board assembly with the power supply section. On the back of the display board are three switches, used for troubleshooting purposes, and two spare lamps.

1-15. CONTROL PANEL ASSEMBLY. The control panel assembly, reference designation A502, contains the computer operating controls. The unit is situated immediately beneath the display board assembly, as shown in figures 1-3 and 1-7. The controls on the panel are principally push-type switches, and some have internal indicating lamps. Connection to the control panel assembly is made by the control cable (figure 1-3), which plugs onto the front end of the front panel coupler card A101. Additional connections are made by wires in the strip cable, which connect with the power supply section and with power fail interrupt card A6 in the card cage.

1-16. POWER SUPPLY ASSEMBLY. The power supply assembly, reference designation A300, is at the rear of the computer cabinet (figure 1-4). Access to this part of the computer is gained by removing the card cage retaining screws, sliding out the card cage, and swinging the card cage open. When sliding the card cage back into the cabinet, it is necessary to first squeeze together the two tab catches.

1-17. The power supply, made up of 12 assemblies, provides the regulated and unregulated dc voltages required by the computer. The power supply also provides dc voltages for plug-in cards in the card cage which are installed as optional devices. Most optional units external to the computer cabinet furnish their own ac and dc voltages, derived from a separate connection to the ac power line. When an

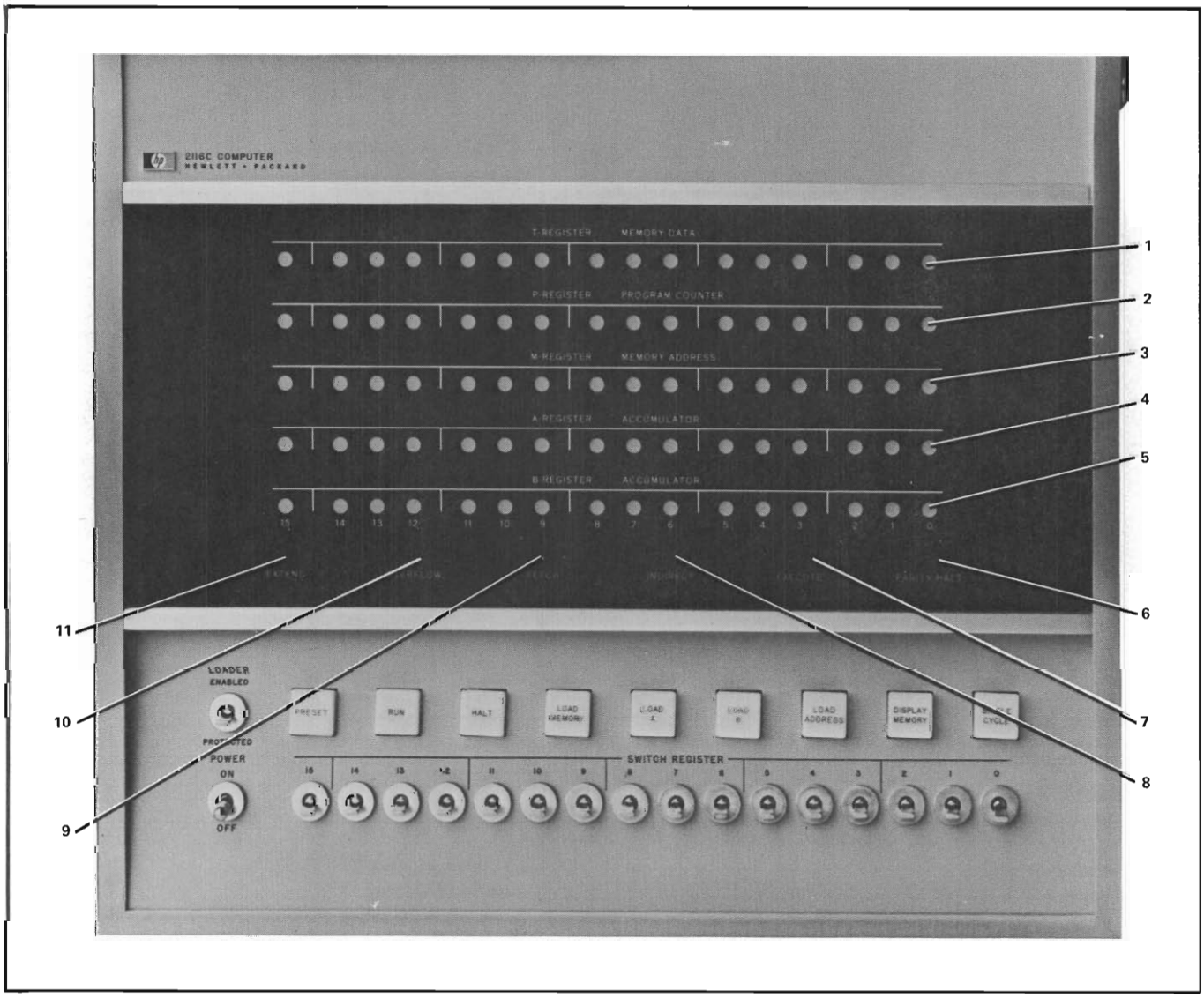


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Figure 1-6. Display Board Assembly A501, Indicators

external device does obtain a dc operating voltage from the computer, the voltage is furnished through the 48-pin connector of the interface card in the computer. (An example is the +12 and -12 volts used by the model 2752A Teleprinter.)

1-18. BACKPLANE CONNECTORS. The backplane connectors are at the rear of the card cage (figure 1-5). The connectors receive the plug-in cards installed in the card cage, and provide connections to the cards.

1-19. CONTROLS AND INDICATORS.

1-20. The locations of operator's controls and indicators are shown in figures 1-6 and 1-7. The reference designation of each control and indicator, together with a description of the purpose of each, is given in tables 1-2 and 1-3.

1-21. IDENTIFICATION.

1-22. COMPUTER SERIAL NUMBER.

1-23. The computer is identified by an 8-digit or 9-digit and one letter (000-00000 or 0000A-00000) serial-number marked on the rear of the computer (item 4, figure 1-11). The first three or four digits are a serial-number prefix used to indicate design changes. If the serial-number prefix on the computer does not agree with the prefix number on the title page of this manual, manual-change information is supplied in a supplement accompanying this volume. The letter, when used, designates the country in which the computer was manufactured ("A" indicates the United States). The remaining five digits are a sequential suffix number that changes with each computer.

1-24. COMPUTER MODEL NUMBER.

1-25. The computer model number (2116C) is marked beneath the serial number on the back of the computer. The model number is also marked on the front door of the computer.

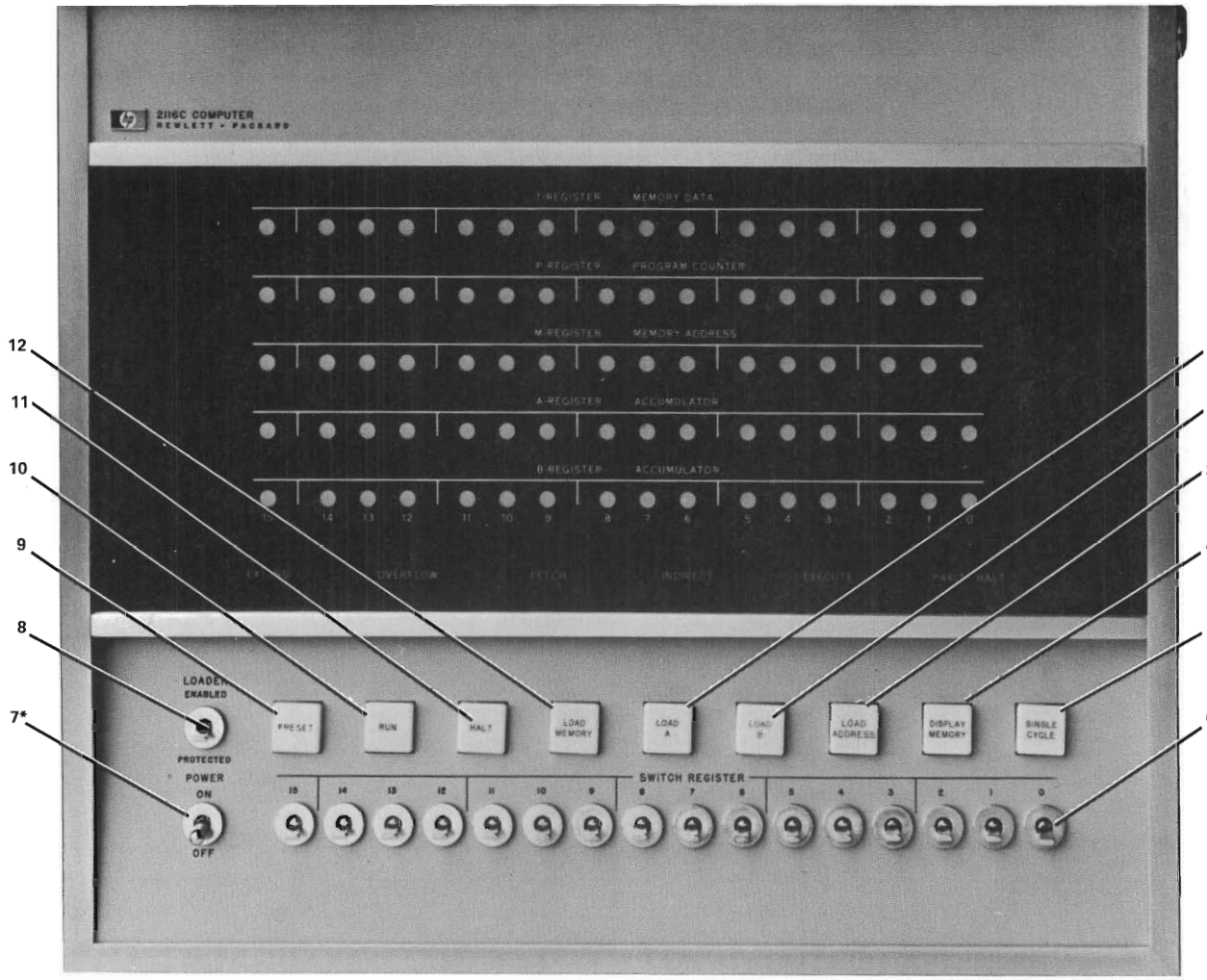
1-26. OPTION NUMBERS.

1-27. On the rear of the computer, beneath the model number, is marked the identifying number of each factory-installed optional feature. When optional features are supplied for installation in the field, the installation instructions require that the appropriate option number be marked in the same place as for a factory-installed option.

1-28. To determine the meaning of option numbers, refer to a Hewlett-Packard sales catalog, or request the nearest Hewlett-Packard Sales and Service Office to furnish a list of optional features for the 2116C. (Sales and Service Offices are listed in the back of this manual.)

Table 1-2. Indicators on Display Board Assembly A501

ILLUSTRATION CALLOUT (FIGURE 1-6)	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
1	T-REGISTER MEMORY DATA	A501DS1 thru A501DS16	Indicator lamps	Displays the contents of the T-register.
2	P-REGISTER PROGRAM COUNTER	A501DS17 thru A501DS32	Indicator lamps	Displays the contents of the P-register.
3	M-REGISTER MEMORY ADDRESS	A501DS33 thru A501DS48	Indicator lamps	Displays the contents of the M-register.
4	A-REGISTER ACCUMULATOR	A501DS49 thru A501DS64	Indicator lamps	Displays the contents of the A-register.
5	B-REGISTER ACCUMULATOR	A501DS65 thru A501DS80	Indicator lamps	Displays the contents of the B-register.
6	PARITY HALT	A501DS81	Indicator lamp	Used by an optional feature. Refer to Memory Parity Check Operating and Service Manual (part no. 12591-9001).
7	EXECUTE	A501DS82	Indicator lamp	Lights when the computer is in the execute phase.
8	INDIRECT	A501DS83	Indicator lamp	Lights when the computer is in the indirect phase.
9	FETCH	A501DS84	Indicator lamp	Lights when the computer is in the fetch phase.
10	OVERFLOW	A501DS85	Indicator lamp	Lights when the Overflow FF is set.
11	EXTEND	A501DS86	Indicator lamp	Lights when the Extend FF is set.



* SOME COMPUTERS WITH SERIAL NUMBER PREFIX 980- HAVE A LIGHTED, PUSH-TYPE POWER SWITCH INSTEAD OF THE TOGGLE-TYPE POWER SWITCH WHICH IS SHOWN.

2107-305

Figure 1-7. Control Panel Assembly A502, Controls and Indicators

Table 1-3. Controls and Indicators on Control Panel Assembly A502

ILLUSTRATION CALLOUT (FIGURE 1-7)	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
1	LOAD A	A502S104	Push-switch (momentary action)*	When pressed, loads the contents of the S-register into the A-register.
2	LOAD B	A502S103	Push-switch (momentary action)*	When pressed, loads the contents of the S-register into the B-register.
3	LOAD ADDRESS	A502S102	Push-switch (momentary action)*	When pressed, loads the contents of the S-register into the M-register and P-register, and places the computer in fetch phase.
4	DISPLAY MEMORY	A502S101	Push-switch (momentary action)*	When pressed, displays in the T-register the contents of the core storage location specified by the M-register. Then advances the P-register by 1, sets the contents of the M-register equal to the contents of the P-register, and places the computer in fetch phase.
5	SINGLE CYCLE	A502S100	Push-switch (momentary action)*	When this switch is pressed, the computer performs one machine cycle in the phase indicated on display panel A501. The address of the instruction performed is displayed in the M-register.
6	SWITCH REGISTER	A502S1 through A502S16	Toggle switches	Provides the means for manually entering data, addresses, or instructions into the computer. The low-order bit is SWITCH REGISTER switch 0. A switch is set to the up position for logic 1, to the down position for logic 0. After a number is entered, one of the following push-switches is pressed: a. LOAD MEMORY. b. LOAD A. c. LOAD B. d. LOAD ADDRESS. e. DISPLAY MEMORY.
7	POWER	(A502S109 and A502DS109)	Toggle switch (Lighted push-switch)**	The switch turns the computer on or off. (Indicator is lighted when the computer is on, extinguished when the computer is off.)**
8	LOADER	A502S110	Toggle switch	In the ENABLED position, allows the program to read or write in the protected area in memory where the binary loader program is stored.
9	PRESET	A502S108 and A502DS108	Lighted push-switch (momentary action)*	When pressed, the switch places the computer in the fetch phase and extinguishes the PRESET indicator (if lighted). The switch also resets the entire I/O system and the power-fail interrupt system by: a. Clearing the Interrupt Control FF on I/O Control Card A201. b. Clearing the Control FF on each I/O interface card. c. Setting the Flag Buffer FF (if any) and the Flag FF on each I/O interface card. d. Clearing the Flag Buffer FF and Flag FF on Power Fail Interrupt Card A6.

*Inoperative when a program is running.
**Used on some computers having serial number prefix 980-.

Table 1-3. Controls and Indicators on Control Panel Assembly A502 (Continued)

ILLUSTRATION CALLOUT (FIGURE 1-7)	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
9 (Cont)				The PRESET indicator lights when a power-fail interrupt occurs as a result of low line-voltage applied to the computer or to the 2150B I/O and Memory Extender (if used). The indicator also lights in the event of overheating in any of the following: a. Interior of the 2116C cabinet. b. Large heat sink assembly A304. c. Small heat sink assembly A305. d. 2160A Power Supply Extender (if used). e. 2150B I/O and Memory Extender (if used). f. 2151A I/O Extender (if used). The PRESET indicator always lights for the conditions specified above, regardless of whether the computer is running. The indicator also lights when power is initially applied to the computer. After being lighted for any reason, the indicator remains lighted until the PRESET switch is pressed. (The indicator immediately relights if an undervoltage or overheating condition continues.)
10	RUN	A502S107 and A502DS107	Lighted push-switch (momentary action)*	When pressed, the switch starts the program in the phase (fetch, indirect, or execute) indicated on display panel A501. The address of the instruction performed (or continued) is displayed in the P-register before the switch is pressed. While the program is running, the RUN indicator is lighted.
11	HALT	A502S106 and A502DS106	Lighted push-switch (momentary action)	When pressed, the switch stops the program at the end of the current phase. The HALT indicator is lighted when the program is not running.
12	LOAD MEMORY	A502S105	Push-switch (momentary action)*	When pressed, stores the contents of the SWITCH REGISTER switches (S-register) in the core storage location specified by the M-register. Then increments the P-register by 1, sets the contents of the M-register equal to the contents of the P-register, and places the computer in the fetch phase.

*Inoperative when a program is running.

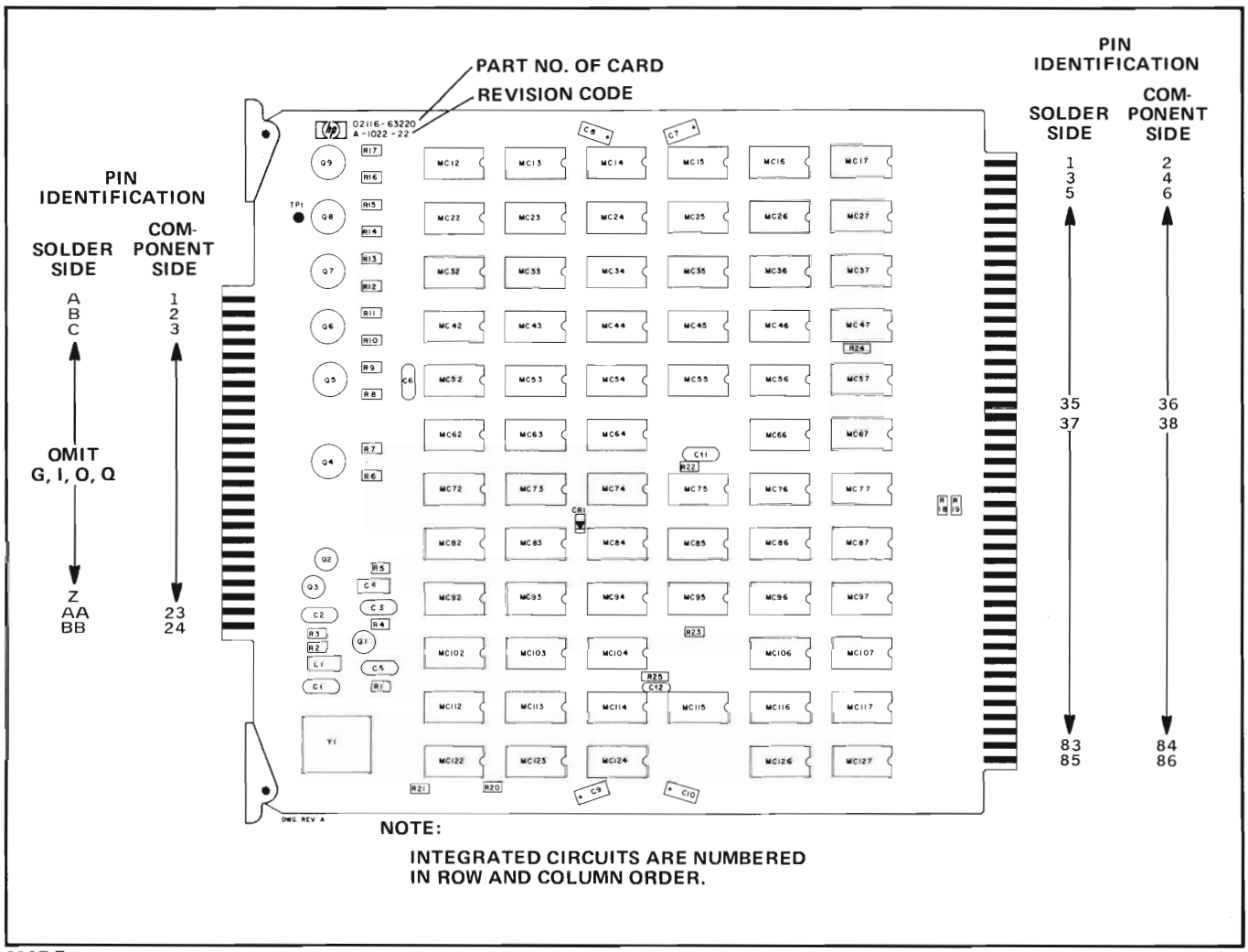
1-29. ASSEMBLY IDENTIFICATION.

1-30. The majority of the electronic assemblies in the computer are plug-in etched-circuit cards and are identified by a part number and revision code. A typical card of the type installed in the card cage, is shown in figure 1-8. In the illustration, the identification block which consists of the trademark, part number, and revision code, is in the upper left corner of the card. (Table 1-4 gives a detailed explanation of this identification block.) Also shown in the illustration are the identifying numbers and letters of the card pins, and the means used for identifying integrated circuits (microcircuits) mounted on the card.

1-31. Assemblies other than circuit cards usually are not marked with their part number and do not have revision codes. Part numbers for these assemblies are found in section VI of this volume, where electronic assemblies are identified by their location in the computer and their appearance.

1-32. CIRCUIT-CARD REVISION CODE.

1-33. Marked beneath the part number on each circuit card is a revision code (see figure 1-8). The first character of the code is a letter, known as the revision notice, which identifies the etched-foil pattern on the card. The next three or four digits, known as a series notice or date code, identify the electrical characteristics of the card with parts mounted. The date code is followed by a one or two digit number, known as the division prefix number, which identifies the Hewlett-Packard division which assembled the completed card. The entire revision code is either stamped on the card with marking ink, or it appears in etched metal letters. If both a stamped and an etched code are used, the stamped revision code supersedes the etched revision code and indicates a parts difference.



2107-7

Figure 1-8. Typical Card Cage Circuit Card

1-34. DOCUMENTATION OF EQUIPMENT IMPROVEMENTS.

1-35. When factory changes are made in the design and construction of the computer, manuals issued with the computer cover the changes by means of an updating supplement.

1-36. The factory may request that changes be made to the computer after it is in the field. When instructions are issued for making such a change, updating supplements or change sheets are issued for all manuals affected by the change.

1-37. STANDARD ACCESSORIES AND SERVICE ITEMS.

1-38. Standard accessories for the 2116C Computer consist of an accessory kit and a rack mounting kit (figure 1-9). The accessory kit contains an ac power cable, an extender card, two extender cables, and a punched-tape loading instruction card. The accessory kit and rack mounting kit are furnished with the computer, and need not be ordered separately.

1-39. AC POWER CABLE.

1-40. The ac power cable is a heavy-duty electrical cable, 10 feet in length, used for supplying 115-volt or 230-volt power to the computer. The cable has a 3-prong male connector, NEMA type 5-15P, for insertion into a NEMA type 5-15R or 5-20R female connector serving as the source of ac power for the computer. If local building codes prohibit use of the NEMA 5-15P connector, it must be replaced with an acceptable type.

1-41. EXTENDER CARD.

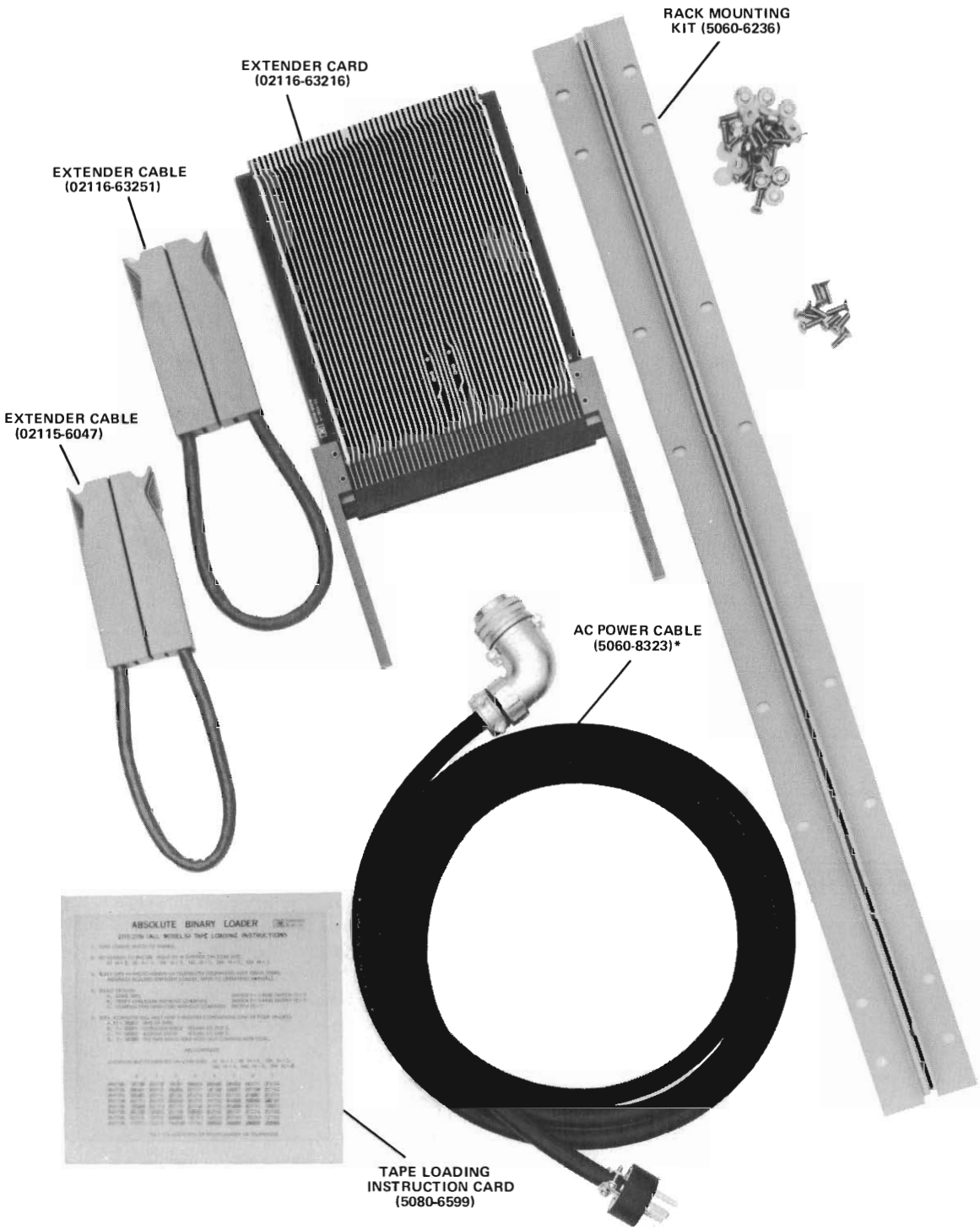
1-42. The extender card allows circuit cards in the card cage to be extended for troubleshooting.

1-43. EXTENDER CABLE.

1-44. Two types of extender cables are supplied. They allow cards that have a cable plugged to their 48-pin connector to be used with the extender card.

1-45. TAPE-LOADING INSTRUCTION CARD.

1-46. An instruction sheet, encased in clear plastic, provides information on how to load binary punched tapes



* AC POWER CABLE 5060-8323, USED WITH COMPUTERS HAVING SERIAL NUMBER PREFIX 1047A- AND ABOVE, IS FURNISHED IN ACCESSORY KIT 02116-63266. AC POWER CABLE 5060-2267 (NOT SHOWN), USED WITH COMPUTERS HAVING SERIAL NUMBER PREFIXES BELOW 1047A-, IS FURNISHED IN ACCESSORY KIT 02116-63221. EXCEPT FOR THIS DIFFERENCE, THE TWO ACCESSORY KITS ARE IDENTICAL.

2107-306

Figure 1-9. Accessory Kit (02116-63266) and Rack Mounting Kit (5060-6236)

into the computer. Included on the instruction card is a listing of the loader program, which may be manually reloaded into the computer if the original stored program is destroyed. The computer is shipped with the required binary-tape loader program stored in core memory.

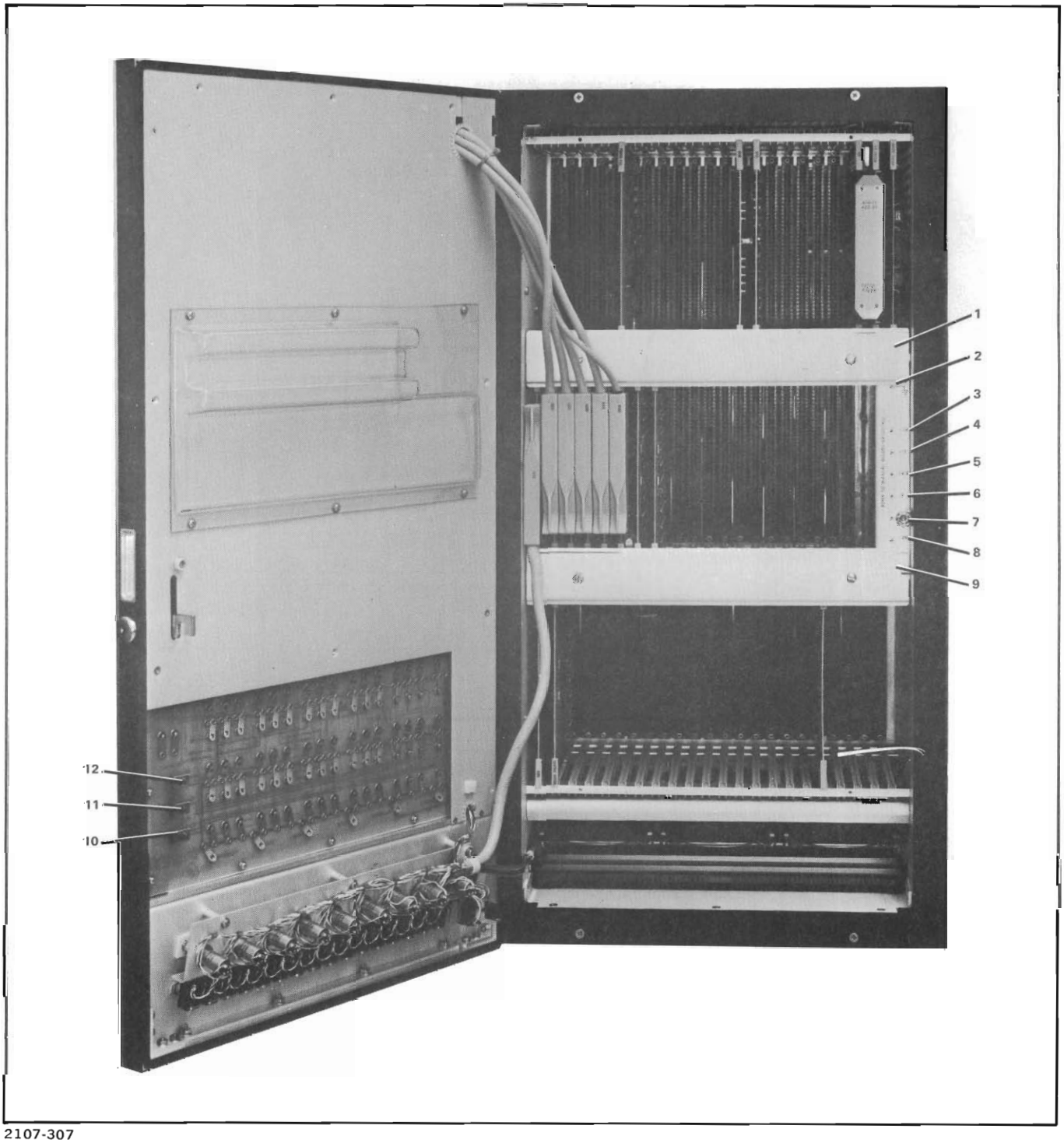
1-47. RACK MOUNTING KIT.

1-48. The rack mounting kit allows the computer to be installed in a standard 19-inch equipment rack.

1-49. MAINTENANCE.

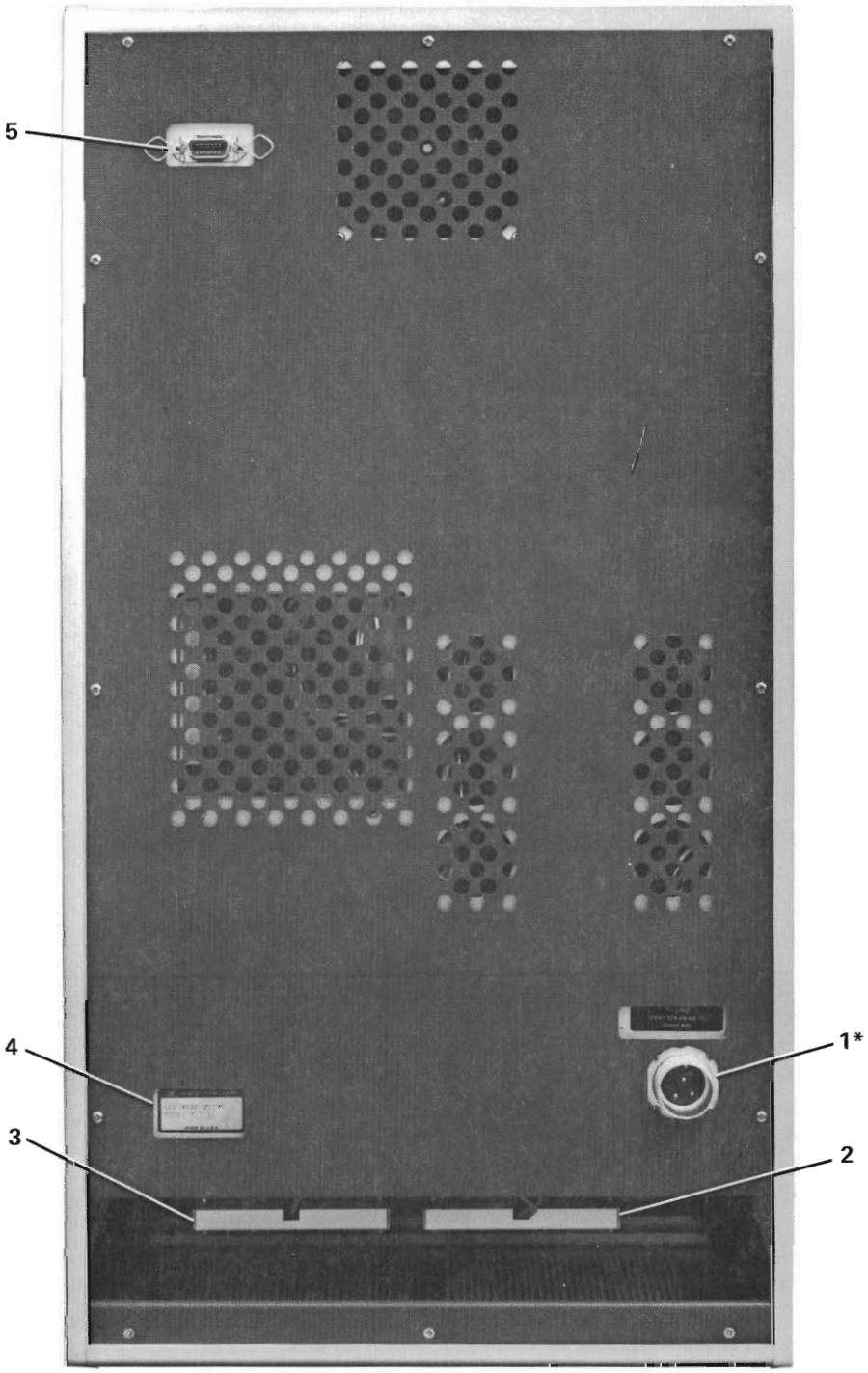
1-50. PRINCIPAL MAINTENANCE FEATURES.

1-51. Facilities for adjusting and servicing the computer are shown in figures 1-10 and 1-11. A brief description of each feature is given in table 1-4.



2107-307

Figure 1-10. Maintenance Features of Display Board Assembly A501 and Card Cage



* COMPUTERS WITH SERIAL NUMBER PREFIX 1047A- AND ABOVE HAVE A THREADED-TYPE POWER CONNECTOR (SHOWN) COMPATIBLE WITH AC POWER CABLE 5060-8323. COMPUTERS WITH SERIAL NUMBER PREFIXES BELOW 1047A- HAVE A TWIST-TYPE POWER CONNECTOR COMPATIBLE WITH AC POWER CABLE 5060-2267.

2107-308

Figure 1-11. Maintenance Features at Rear of Computer

Table 1-4. Computer Maintenance Features

ILLUSTRATION AND CALLOUT NUMBER	PANEL MARKING	REFERENCE DESIGNATION	DESCRIPTION	USE
Fig. 1-10 (1,9)	–	–	Card retainer	Keeps circuit cards in place.
Fig. 1-10 (2)	⏚	A121TP1	Test jack	Ground-return test point.
Fig. 1-10 (3)	+20	A121TP2	Test jack	+20 volt supply test point.
Fig. 1-10 (4)	+12	A121TP3	Test jack	+12 volt supply test point.
Fig. 1-10 (5)	+4.5	A121TP4	Test jack	+4.5 volt supply test point.
Fig. 1-10 (6)	-2	A121TP5	Test jack	-2 volt supply test point.
Fig. 1-10 (7)	-12	A121TP6	Test jack	-12 volt supply test point.
Fig. 1-10 (8)	-20	A121TP7	Test jack	-20 volt supply test point.
Fig. 1-10 (10)	INSTRUCTION	A501S113	Slide switch	Prevents the P-register contents from being changed, thereby causing the same instruction to be executed repeatedly.
Fig. 1-10 (11)	PHASE	A501S112	Slide switch	Causes the computer to remain in the phase existing at the time the switch is set.
Fig. 1-10 (12)	MEMORY	A501S111	Slide switch	Turns memory section off. Makes all memory locations appear as if containing zeros.
Fig. 1-11 (1)	–	A300J1	Power connector	AC power input to computer.
Fig. 1-11 (2)	–	–	Air filter	Filters cooling air.
Fig. 1-11 (3)	–	–	Air filter	Filters cooling air.
Fig. 1-11 (4)	–	–	Identification label	Used to identify computer model number and serial number to determine technical-manual effectivity. Optional features installed in the computer are also listed on this label.
Fig. 1-11 (5)	–	A300J2*	Cable connector	Connector for cable to optional power supply extender, or memory and I/O extender.

*The manual for the 2160A Power Supply Extender refers to this connector on the 2116C as J2.

1-52. MAINTENANCE TOOLS, PARTS, MATERIALS, AND EQUIPMENT.

1-53. TOOLS. A standard electronics tool kit will provide the tools required for normal servicing of the computer. The kit must include a soldering iron designed for removing and installing 14-pin and 16-pin integrated circuits, and a rubber bulb with suction tube for withdrawing molten solder. Also required is a torque wrench, capable of indicating 15 inch-pounds, with 3/8-inch, 7/16-inch, and 9/16-inch sockets.

1-54. If changes are made to backplane wiring, the following wiring tools are required:

a. A-MP TERMI-POINT Strip-Fed Service Tool, Amp part no. 69525-1.

b. A-MP TERMI-POINT Mandrel for above tool, Amp part no. 69551-1, used with no. 26 wire (American Wire Gauge), 7 strands, wire insulation thickness 0.022 to 0.045 inches, wiring-post size 0.031 x 0.062 inch.

c. A-MP TERMI-POINT Pull Test Tool, Amp part no. 69358-2, 2.25 lbs test force, for 0.031 x 0.062 inch wiring post.

d. A-MP TERMI-POINT Extraction Tool, Amp part no. 69357-3, used for removing Amp 1-330495-5 clip.

1-55. In addition to the wiring tools, the following tool is required if a contact in a backplane connector must be replaced: A-MP TERMI-TWIST Contact Replacement Tool, Amp part no. 69514-1, for 0.031 x 0.062 inch wiring post.

1-56. The A-MP tools may be obtained from Amp Incorporated, Harrisburg, Pennsylvania. However, these tools are rarely required and it may be preferable to have backplane wiring work done by Hewlett-Packard service personnel. A list of Hewlett-Packard Sales and Service Offices is furnished at the back of this volume.

1-57. PARTS AND MATERIALS. Spare parts that may be required for the computer are listed in section VI of this volume. Part numbers and ordering information are included. When ordering components which install on circuit cards, refer to section VII for part numbers.

1-58. Materials and chemicals normally used for electronics service work must be available to the serviceman. These must include heat-conducting compound; a suitable type is Wakefield 120-2 Thermal Joint Compound (HP part no. 6040-0239).

1-59. SERVICING EQUIPMENT. Equipment recommended for maintenance, troubleshooting, and repair of the computer is listed in table 1-5. Equipment equivalent to that specified may be substituted.

1-60. FIELD OFFICE ASSISTANCE.

1-61. Should servicing assistance be required, contact the nearest Hewlett-Packard Sales and Service Office. These offices are listed at the back of this volume.

Table 1-5. Recommended Servicing Devices

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED HP MODEL
Dual-trace oscilloscope	Rise time: ≤10 ns. Vertical deflection: 1 volt/division and 10 volts/division (including attenuator probe, if used). Horizontal sweep speed: 0.1 microsecond/division to 1 second/division.	HP 180A Oscilloscope with 10004A Probe and the following plug-in units: HP 1801A Dual Channel Vertical Amplifier HP 1820A Time Base or HP 1821A Time Base and Delay Generator.
Digital voltmeter	At least 4-digit readout. Minimum input resistance: 10 megohms. Full-scale ranges: 9.999 and 99.99V dc.	HP 3439A Digital Voltmeter with HP 3441A Range Selector
AC voltmeter	Expanded-scale or digital-readout type, capable of reading the ac voltage supplied to the computer to ±1%. Voltage range must be at least 100-115 volts (for a 115-volt computer), or 200-230 volts (for a 230-volt computer).	HP3445A AC/DC Range Unit. (Also performs functions of HP 3441A Range Selector listed above. Requires HP 3439A Digital Voltmeter.)
Multimeter	Accuracy: ±3% of full scale. Full-scale ranges: 100 mV to 300V (dc and ac), 10 ohms center-scale to 10 megohms center-scale.	HP 427A
Logic probe	Indication: logic true >+1.4 volts.	HP 10525A
Variable auto-transformer	Capable of reducing computer input line-voltage to 98 volts rms (196 volts for a 230-volt computer), and able to furnish the power required by the computer (1000 to 1600 watts, depending on the optional features installed).	None
Centigrade thermometer	General-purpose type, accurate to ±1°C.	HP 0440-0004
High-pressure air source	25-50 psi pressure	None
Vacuum cleaner	Must have flexible hose with small nozzle, vacuum port for hose, and pressure port for hose.	None
IC test clip	None	None

NOTES:

1. The logic probe is optional. Operating voltage for the probe can be obtained from the +4.5 volt test jack on overvoltage protection assembly A121. Insert a plug into the test jack and connect the probe, using the alligator clip on the adaptor supplied with the probe. Use care not to cause a short.

2. Ambient-temperature and humidity specifications of test equipment must suit the computer environment.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section presents instructions for installing the HP 2116C Computer. Included are procedures for initial inspection and performance testing of the computer. Also described are claims procedures and methods of repacking the computer for shipment.

2-3. INSPECTION OF SHIPMENT.

2-4. The computer and its accessories may be shipped in more than one container. When the shipment is received, check the carrier's papers to ensure that they indicate the number of containers that has been received.

2-5. If damage to a shipping carton is evident, or if a carton is water-stained, ask the carrier's agent to be present when the carton is opened.

2-6. When ready to unpack the shipment, open the carton or cartons, and find the envelope marked "CUSTOMER RECORDS." One of the items in this envelope is a list of the equipment shipped. Check this against the original ordering papers sent to Hewlett-Packard, Cupertino, to ensure that all items correspond.

2-7. Unpack the carton or cartons, and examine each item for external damage. Look for such things as broken controls, dented corners, bent panels, and scratches. Also check the rigid foam-plastic cushioning material (if used) for signs of deformation which could indicate rough handling in transit.

2-8. Open the door of the computer, and check for loose parts inside the computer. Remove the card cage retaining screws (shown in figure 1-3), pull out the card cage, and swing it to the right. Examine the interior of the computer for loose parts or other signs of damage. Press upward on the air filters beneath fans A304B2 and A305B3 (figure 1-4) to ensure that the filters are fully seated. If one of these filters has dropped off, install it by pressing it upward beneath the fan. The notch in the filter frame must be at the back of the computer.

2-9. If the above examination reveals damage to the computer or its accessories, follow the damage-claim procedure described in paragraph 2-45. Retain the shipping containers and packing materials for examination in the settlement of claims, or for future use.

2-10. Upon completing the inspection for damage in transit, proceed with a physical inventory of the material received, as described in the following paragraphs.

2-11. PHYSICAL INVENTORY.

2-12. MANUALS.

2-13. Check to ensure that all manuals listed in the "CUSTOMER RECORDS" envelope have been received.

2-14. EQUIPMENT.

2-15. Check the model number marked on the front door of the computer to ensure that a 2116C has been received.

2-16. Check the model number marked on the back of the computer (figure 1-11, item 4) to ensure that a 2116C is indicated. Also check the serial number on the back of the computer and the number given in the "CUSTOMER RECORDS" envelope to ensure that the numbers compare. Compare the list of optional features marked on the back of the computer to be sure that it includes all optional features listed in the "CUSTOMER RECORDS" envelope.

2-17. Check to ensure that each equipment item listed in the "CUSTOMER RECORDS" envelope has been received. In the case of certain optional features, it may be necessary to refer to the Operating and Service Manual for the optional feature to determine how to identify it. If an option consists of more than one physical unit, make sure that all parts have been received.

2-18. PROGRAM TAPES.

2-19. Check the punched tapes received with the shipment to ensure that all tapes listed in the "CUSTOMER RECORDS" envelope have been received.

2-20. INSTALLATION PROCEDURE.

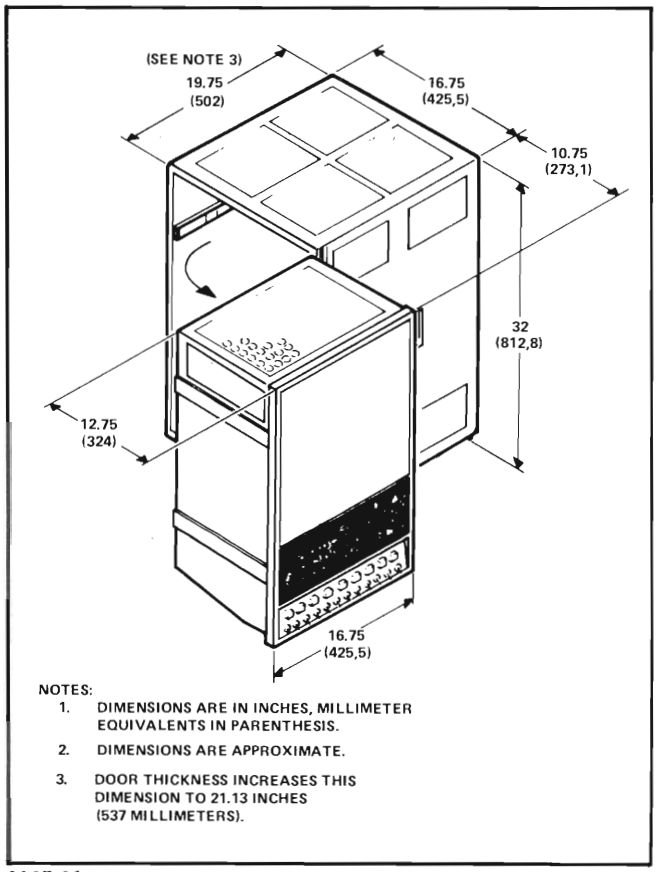
2-21. MANUAL UPDATING.

2-22. Before installing the computer, perform any updating that may be required for Volumes One, Two, and Three of this technical manual. First, check the first four digits of the serial number marked on the back of the computer (item 4, figure 1-11). If this serial-number prefix is higher than 1047A- , one or more updating supplements are furnished with Volumes One, Two, or Three. Follow the updating instructions given in the supplements. Then mark the serial number of the computer on the title page of each volume.

2-23. ENVIRONMENTAL REQUIREMENTS.

2-24. The computer must be installed in a location where the ambient temperature is 0° to 55°C (32° to 131°F) when the computer is operating. Relative humidity must be 50 to 95 percent within the temperature range 25° to 40°C; no moisture condensation, water drips, or spray can be permitted. When the computer is turned off, the permissible temperature range is -40° to 75°C (-40° to 167°F).

2-25. Computer dimensions are shown in figure 2-1. To maintain proper cooling, there must be at least two inches of clear space at the sides of the computer, and three inches above the computer. Clearance at the back must be at least five inches to permit passage of cooling air and to prevent sharp bends in cables entering the computer. Heat dissipated by the computer is 5500 BTU per hour. Internal fans produce an airflow of 600 cubic feet per minute through the computer cabinet.



2107-11

Figure 2-1. Computer Dimensions

2-26. POWER REQUIREMENTS.

2-27. The computer operates from a power source supplying an ac voltage of 115 or 230 volts rms ±10 percent, single-phase. The required power frequency is 47.5 to 66 Hz. (As an optional feature, 400-Hz operation is available. Tolerance for this frequency is ±40 Hz.) Power consumption for all voltages and frequencies ranges from 1000 to 1600 watts, depending on the optional features included in the computer. Note that optional features not within the computer cabinet, and which make separate connection to the power line, have their own power specifications, and the power they require is additional to that consumed by the computer. For the computer itself, there is a line–current surge of about 100 amperes at power turn-on.

2-28. If the computer is ordered with option 015 to enable operation from a 230-volt power source, jumpers are used to modify the power supply. The computer is shipped with these jumpers connected in accordance with the customer's order. However, before the computer is connected to the power line, the jumpers must be checked to ensure that they are correctly connected. This is done as follows:

a. Make sure the computer power cable is not plugged into a voltage source.

b. Swing the card cage out of the computer cabinet.

c. Remove the transformer cover by pulling out the four white studs in the cover. The cover is shown in figure 1-4.

d. Locate terminal strip A311TB1. This terminal strip is mounted on the power transformer, and is the top terminal strip on the left side of the transformer. (See figure 2-2.)

e. Check jumpers B and C on terminal strip A311TB1 to ensure that they are properly connected. (The transformer cover also provides instructions on connetcing the jumpers.)

f. Locate terminal strip A311TB8 (figure 2-2).

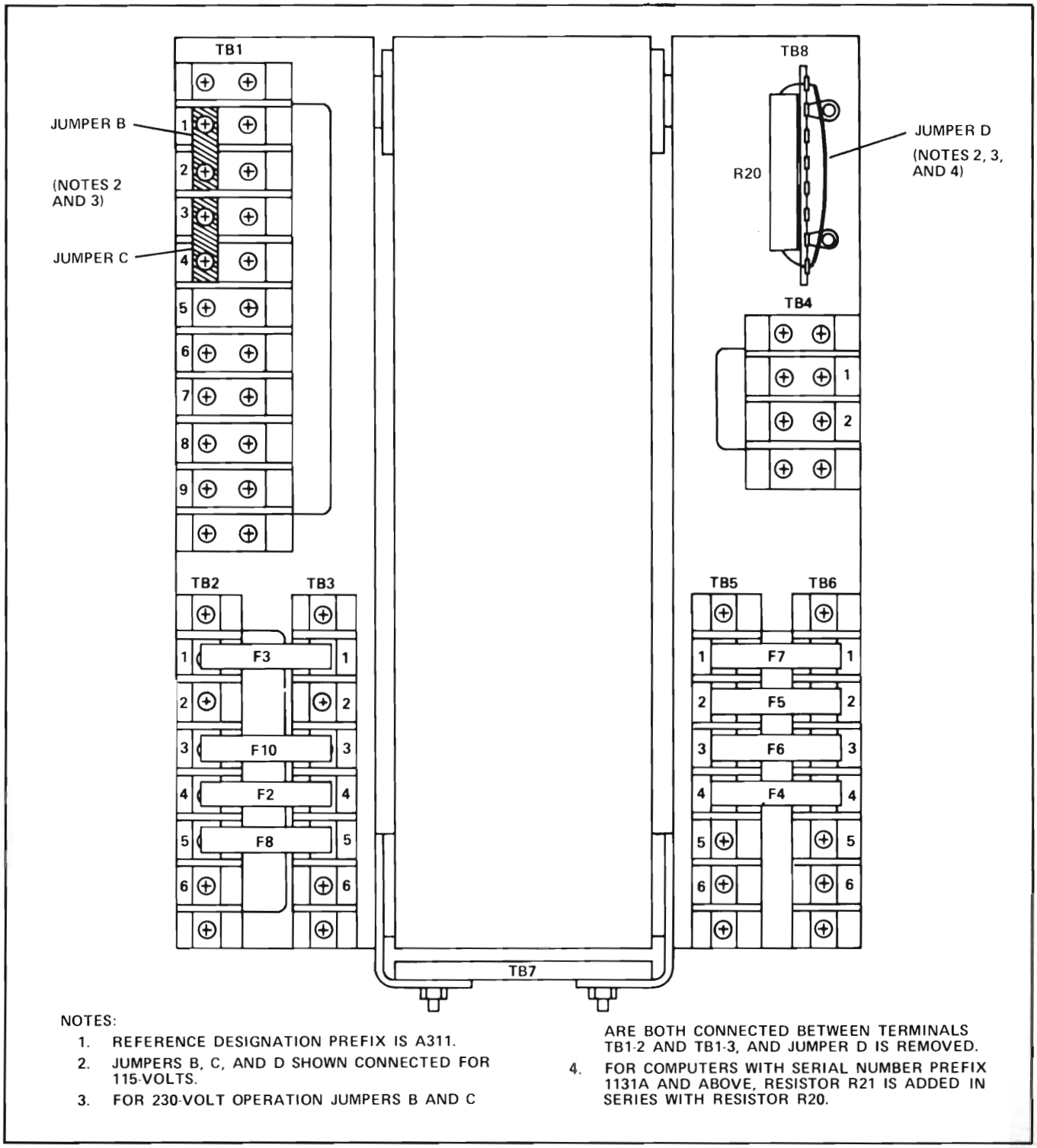
g. Check jumper D on terminal strip A311TB8. For 115-volt operation, jumper D is installed between A311TB8-1 and A311TB8-7. For 230-volt operation, jumper D is removed and resistor A311R20 is connected between A311TB8-1 and A311TB8-7. (On computers with serial number prefix 1131A and above, resistor A311R21 is connected in series with A311R20.)

h. Replace the transformer cover.

2-29. AC POWER OUTLET AND EXTERNAL GROUND.

2-30. The ac outlet which will supply power to the computer must be checked to ensure that it furnishes the correct voltage for the computer. Furthermore, the ac outlet and its associated wiring and fuses (or circuit breakers) must be capable of carrying at least 15 amperes for a 115-volt computer, or 7 amperes for a 230-volt computer.

2-31. The ac power cable supplied with the computer fits a NEMA (National Electrical Manufacturers Association) type 5-15R or 5-20R female power outlet (figure 2-3). If the computer is to be installed in a building, make sure the local electrical codes permit use of this type of electrical outlet for the line voltage and load current used by the computer. (The 5-15R or 5-20R outlet must never be used for 230-volt operation.) If necessary, change the plug on the ac power cable to fit an acceptable type of outlet, as described in paragraph 2-36.



2107-12B

Figure 2-2. Location of Voltage-Change Jumpers

2-32. Check at the ac outlet with a voltmeter to be sure the required voltage is supplied, and that it is single-phase. If the computer is connected for 115-volt operation, the voltage must be 103.5 to 126.5 volts ac (rms). For 230-volt operation, the voltage must be 207 to 253 volts ac (rms). Bear in mind that the electrical load imposed by the computer and its optional features may reduce the line voltage below the no-load value.

2-33. If the voltage is in the correct range, check the ac outlet to ensure that it is correctly wired with respect to high-potential ac voltage, ac neutral, and earth ground. Use a low impedance voltmeter, 20,000 ohms per volt or less, for making these measurements. If the outlet is improperly wired, correction must be made by a qualified electrician, and local electrical codes must be observed if the installation is in a building.

2-34. If the electrical system has only two wires (that is, if there is not separate earth ground wire), the computer will operate with the earth ground lead in the ac power cable unconnected. However, for safety reasons, it is strongly recommended that attachment be made to a good earth ground. This connection must be made through the earth ground wire in the ac power cable used by the computer.

2-35. For installation in a ship, airplane, motor vehicle, or train, the earth ground wire in the computer ac power cable must be connected to the hull or metal frame of the vehicle.

2-36. AC POWER CABLE.

WARNING

If the connector at either end of the ac power cable (part no. 5060-2267 or 5060-8323) is changed, the replacement connector must be correctly wired to the cable. The procedure for checking the connections is described in paragraph 2-38 below. If the connector is incorrectly wired, fuse A312F1 in the computer will be in the neutral side of the power line. As a result, when the fuse blows ac high potential will remain in certain circuits in the computer, presenting a hazard to the serviceman.

2-37. Check the ac power cable to be sure it is long enough to connect the computer with the ac outlet to be used. The cable is 10 feet (3 meters) long. If necessary, use a longer cable or add an extension cable. Also, make sure the connector on the cable fits the ac outlet. Any added cabling must have three conductors, each no. 14 American wire gauge (AWG) or heavier, and connectors must be rated at 15 amperes or more.

2-38. If an extension cord is used, or if the connector at either end of the ac power cable has been removed, make sure that fuse A312F1 remains on the high-potential side of the power line. This is done as follows. (Read the entire procedure before starting.)

a. Plug the power cable into the back of the computer. Do not make connection with the ac power source.

b. Plug the extension cord, if used, into the power cable. Do not make connection with the ac power source.

c. Extend the card cage and remove the protective cover from assembly A312. (See figures 1-4 and 7-33.)

d. Set an ohmmeter to the R x 1 scale, and zero the meter.

e. Connect one lead of the ohmmeter to the high-potential prong of the male connector which will plug into the ac source.

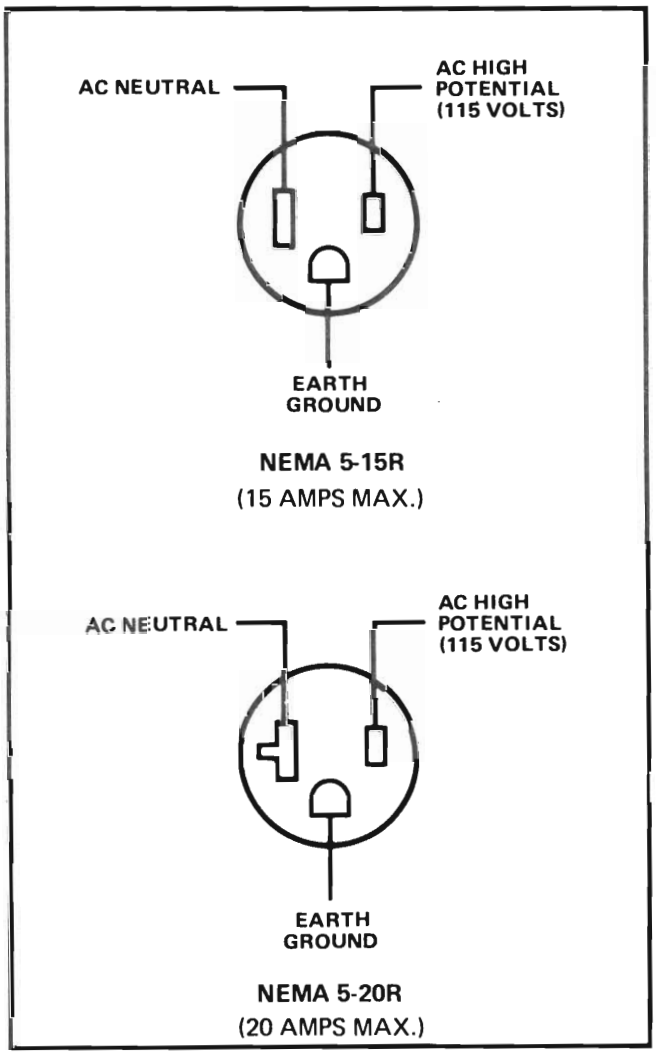


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Figure 2-3. NEMA 5-15R and R-20R Female Connectors, Mating Side

f. Connect the other ohmmeter to terminal A of relay A312K2.

g. Check the ohmmeter reading. If an open circuit is indicated, actuate the POWER switch to close the switch contacts (see figure 2-4). With the POWER switch contacts closed, the ohmmeter reading should be approximately zero. If the reading is not approximately zero ohms, the power cable connections are incorrect. Make the necessary corrections as described in step "1" below.

h. If the test in step "g" is correct, actuate the POWER switch once again to open the switch contacts. The ohmmeter should indicate infinity. If the reading is not infinity, the power cable connections are incorrect.

i. If step "h" is satisfactory, remove the ohmmeter lead from the high potential prong of the power connector, and connect it to the ac neutral prong of the connector.

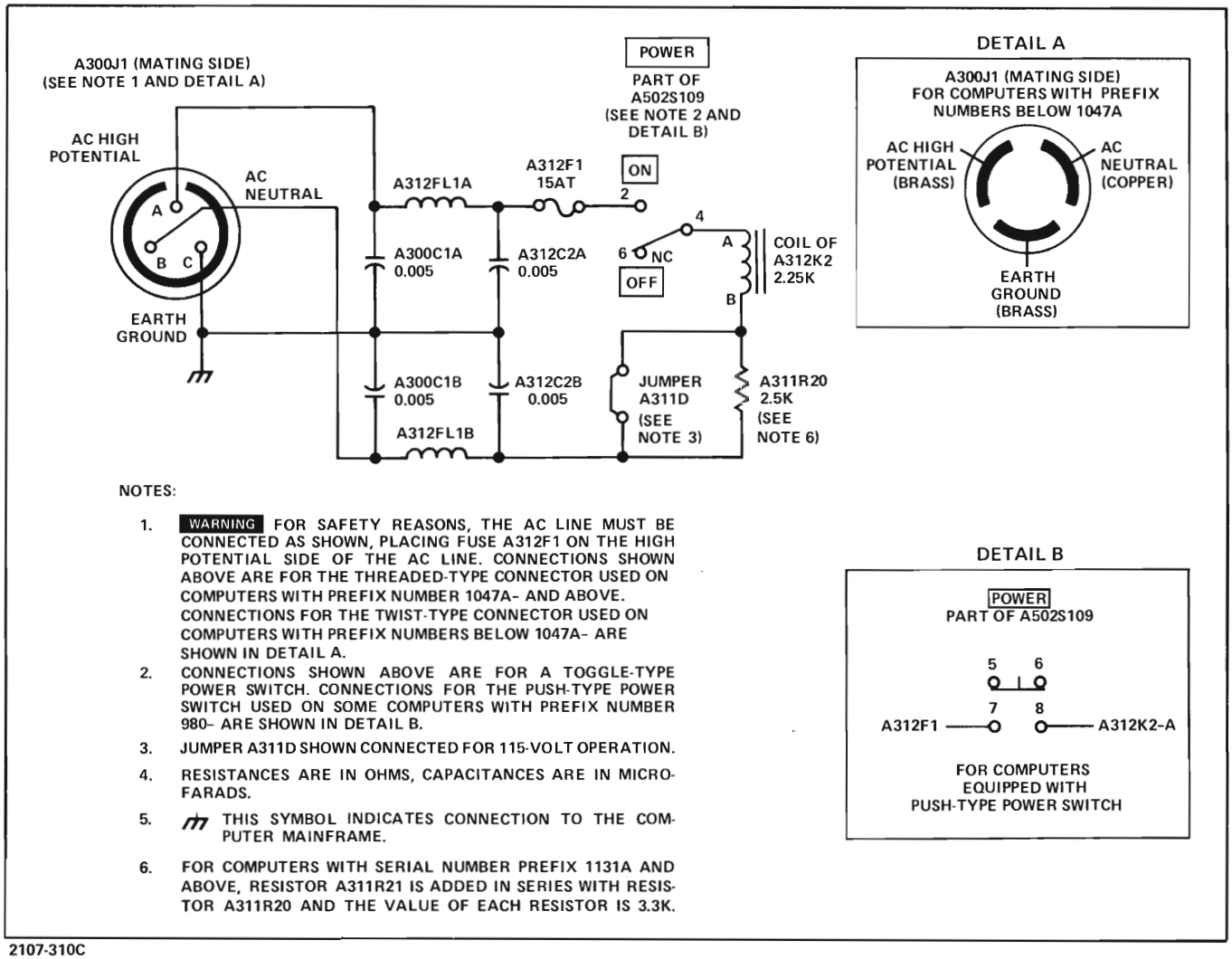

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Figure 2-4. AC Power Connector Check Diagram

j. Check the ohmmeter reading. The indication should be between 2,000 and 10,000 ohms. If the resistance is zero or infinity, the power cable connections are incorrect.

k. If step "j" is satisfactory, check the resistance between the earth ground prong of the power connector and the frame of the computer. Zero ohms should be indicated. If the reading is infinity, the power cable is incorrectly wired.

l. If any of the preceding measurements is incorrect, make the necessary changes in connector wiring. If an extension cord is used, change connections in one of the extension-cord connectors, rather than in the factory-wired ac power cable. After making the correction, repeat the entire procedure, starting with step "d".

2-39. MOUNTING.

WARNING

If the 2116C is mounted in a rack which has slide-out drawers, heavy doors, or heavy protruding devices, the rack must be bolted to the floor or heavily weighted at the base. Otherwise, when the 2116C card cage is extended, there is danger of the rack tipping forward. This possibility does not exist if the rack has no protrusions, or if the 2116C is placed on a bench or table.

2-40. The computer is designed either for bench installation or for mounting in a standard 19-inch equipment rack. When rack mounted, the computer fits within the normal 22-inch rack depth. When installed on a shelf, bench, or table, the computer need not be fastened down except for shipboard, aircraft, or other mobile use. For these mobile installations, shock mounts must be used. When installed in a rack, mount the computer in accordance with the instructions included with the rack-mounting kit. In mobile installations the entire rack, rather than the computer itself, must be shock mounted.

2-41. After the computer has been mounted, install and connect optional devices which are external to the computer. (Internal devices are factory-installed.)

2-42. Set the LOADER switch to the PROTECTED position and connect the computer and external devices to the ac power source. Turn on the computer and all other electrical devices which will load the computer power line. Measure the power line voltage under this maximum load condition to ensure that at least 103.5 volts (rms) is supplied (or 207 volts for a 230-volt computer). Then perform the dc voltage checks using the procedure specified in Section V of this volume. When this has been completed, make a performance check of the computer and all optional features.

2-43. PERFORMANCE CHECK.

2-44. Computer performance is checked by performing the basic checkout and diagnostic checkout procedures presented in Section IV of this volume. Basic checkout consists of using front panel controls and indicators to check the overall performance of key circuit functions within the basic computer, particularly those circuits involved in program loading. Diagnostic checkout consists of using test programs to dynamically check logical operations performed by the basic computer. Performance checks of optional circuits and devices are described in separate manuals included with the computer documentation.

2-45. CLAIMS.

2-46. If the computer is incomplete or damaged when received, or if it fails to meet specifications, notify the nearest Hewlett-Packard Sales and Service Office. (Sales and Service Offices are listed in the back of this volume.) If damage occurred in transit, notify the carrier also. Hewlett-Packard will arrange for replacement or repair without waiting for settlement of claims against the carrier. In the event of damage in transit, retain the packing carton and packaging materials for inspection.

2-47. REPACKAGING FOR SHIPMENT.

2-48. SHIPMENT USING ORIGINAL PACKAGING.

2-49. The same containers and materials used in factory packaging can be used for reshipment of the computer. Alternatively, containers and packing materials may be obtained from Hewlett-Packard Sales and Service Offices. If the computer is being sent to the factory for servicing, attach a tag to the computer specifying the return address, the type of service required, the computer model number, and the full serial number of the computer. Mark the container "FRAGILE" to assure careful handling. In any correspondence, refer to the computer by model number and full serial number.

2-50. SHIPMENT USING NEW PACKAGING.

2-51. The following instructions should be followed when packaging the computer with commercially available materials:

a. Wrap the computer in heavy paper or sheet plastic. If shipping the computer back to the factory, first attach a tag to the computer with the return address and indicating the type of service required, the computer model number, and full serial number.

b. Use a strong shipping container. A double-wall carton of 350-pound test material is adequate.

c. Use enough shock absorbing material (3- to 4-inch layer) on all sides of the computer to provide a firm cushion and to prevent movement inside the container. Use particular care to protect the corners and front of the computer.

d. Seal the shipping container securely, and mark it "FRAGILE."

e. In any correspondence with the factory, refer to the computer by model number and full serial number.

2-52. WARRANTY.

2-53. The terms of the warranty for the HP 2116C Computer are described inside the front cover of this manual. For any additional information concerning the warranty, contact the nearest Hewlett-Packard Sales and Service Office.

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section explains the theory of operation of the 2116C Computer. The discussion is conducted at the block-diagram level, with circuit-diagram analysis of complex nondigital circuits. Complex logic circuits are also given detailed treatment in this section. However, complete coverage of logic circuits is reserved for section IV of this volume, where troubleshooting charts together with the logic diagrams in section VII present a fully detailed view of computer functioning.

3-3. REFERENCE INFORMATION.

3-4. The following paragraphs present general information which is required for understanding the theory discussions in this section.

3-5. ABBREVIATIONS.

3-6. Abbreviations of flip-flop names, and abbreviated designations of signals, are defined in the signal lists in section VII.

3-7. BINARY SIGNAL LEVELS.

3-8. The binary signal levels in the computer are approximately +2.3 volts and +0.2 volts. The levels may vary from these approximate amounts, depending on the type of integrated circuit providing the signal, its condition, and its load. The minimum and maximum input and output voltages for each type of integrated circuit are specified in table 7-1.

3-9. In this manual, +2.3 volt logic level is referred to by the term "true," and the +0.2 volt level is referred to as "false."

3-10. LOGIC CIRCUITS.

3-11. The logic circuits principally employ positive logic. That is to say, all inputs to an "and" or "nand" gate must be +2.3 volts for coincidence to occur. When coincidence does occur at the inputs to these gates, the output of the "and" gate becomes +2.3 volts and the output of the "nand" gate becomes +0.2 volts. Similarly, if any input to an "or" or "nor" gate is +2.3 volts, the "or" gate output will be +2.3 volts and the "nor" gate output will be +0.2 volts. The output from the "set" side of a flip-flop is approximately +2.3 volts when the flip-flop is set, and +0.2 volts when the flip-flop is clear.

3-12. The logic symbols used in this manual are described in appendix A.

3-13. SIGNAL NAMES.

3-14. Signals are named in one of the following ways:

a. As a condition which either exists or does not exist.

b. In accordance with the name of a flip-flop, amplifier, or panel switch which is the source of the signal.

c. In accordance with the name of the bus which carries the signal.

d. As a command or order, expressed in the imperative grammatical mode.

3-15. Since most circuits in the computer employ positive logic, signal names are positive-true. The following paragraphs describe the expression "positive-true name" as applied to the four types of signal names enumerated above.

3-16. When a signal is named in accordance with a condition, the signal level is +2.3 volts when the condition exists, and +0.2 volts when the condition does not exist. For instance, the MRT (memory read time) signal is +2.3 volts during memory read time, and +0.2 volts at other times. Similarly, the "not" OPO (one phase operation) signal is +2.3 volts when a one-phase instruction is not being performed.

3-17. When a signal is named in accordance with the flip-flop which is its source, the signal taken from the set side of the flip-flop is +2.3 volts when the flip-flop is set, and +0.2 volts when the flip-flop is clear. For instance, when the Flag Buffer FF is in the set state, the FBFF signal is +2.3 volts.

3-18. When a signal is named in accordance with the bus which carries it, the signal is +2.3 volts when the bus carries a logic 1, and +0.2 volts when it carries a logic 0.

3-19. When a signal is named in the imperative mode, it becomes +2.3 volts to bring about the action commanded. For instance, the Flag FF is cleared when the CLF (clear flag) signal changes from +0.2 volts to +2.3 volts.

3-20. COMPUTER FUNCTIONAL SECTIONS.

3-21. From a functional standpoint, the computer consists of five sections. These are the control section, arithmetic section, memory section, input/output section, and

power supply section. Various circuit options can augment these sections by extending their capabilities. Circuit options are covered in supplementary operating and service manuals.

3-22. The physical grouping of electronic assemblies in the computer corresponds to the functional sections. As figure 1-3 shows, the circuit cards for the memory, control, arithmetic, and I/O sections are grouped together in the card cage in accordance with function. The power supply is in the back of the computer cabinet, behind the card cage. Controls and indicators for the various functional sections are mounted on the door assembly (figures 1-6 and 1-7).

3-23. Figure 3-1 illustrates the internal makeup and relationships of the five major computer sections. Paragraphs 3-24 through 3-120 describe the function of the various blocks shown in the diagram. The remainder of section III provides a more detailed explanation of computer functions, making use of block diagrams, logic diagrams, and schematic diagrams.

3-24. OVERALL BLOCK DIAGRAM DISCUSSION.

3-25. CONTROL SECTION.

3-26. The control section directs the overall functioning of the computer. The control function is exerted by pulse signals which result from decoded instruction words read from the memory section. These control signals are furnished at a rate, and have a duration, that is determined by the timing circuits.

3-27. TIMING CIRCUITS. The timing circuits consist of the basic timing circuits and the memory timing circuits. Both sets of circuits are on timing generator card A106.

3-28. Basic Timing Circuits. The basic timing circuits produce pulses which control the rate of computer functions. The pulses are produced in a 1.6-microsecond cycle, under control of a 10-MHz oscillator. Principally, eight pulses are produced (figure 3-2). These are referred to as clock pulses, and are designated "T0" through "T7." They are furnished in the sequence in which they are numbered, with each pulse rising as the preceding one falls. After pulse T7, T0 is produced without interruption of the sequence. Each pulse has a duration of 200 nanoseconds. The eight pulses, lasting for 1.6 microseconds, make up the basic machine cycle of the computer. This cycle starts at the beginning of pulse T0.

3-29. As well as identifying the clock pulses, the terms "T0" through "T7" designate the time periods corresponding to the pulses. For instance, time period T3 is the time during which the T3 pulse is true.

3-30. In addition to the clock pulses, the basic timing circuits also produce double-length pulses, lasting for 400 nanoseconds. These coincide in time with two consecutive clock pulses, and are named in accordance with the clock pulses during which they are furnished. For instance, the T0T1 pulse is true during time periods T0 and T1.

3-31. Two further pulses produced by the basic timing circuits are the Time Strobe (TS) pulse, and the Time Strobe A (TSA) pulse. These are 45- to 50-nanosecond pulses, occurring simultaneously, produced at the end of each clock pulse. The trailing edge of each TS and TSA pulse coincides with the trailing edge of each clock pulse. The TS pulse is used in the control and arithmetic sections when a short pulse, synchronized with computer timing, is required. The TSA pulse is used for the same purpose by certain optional devices.

3-32. Memory Timing Circuits. The memory timing circuits are on timing generator card A106, and they provide pulse signals for controlling the transfer of data to and from core storage. The signals are generated from clock pulses, panel controls, and pulses received from the instruction decoder. Through the use of gates, the memory timing circuits produce from these inputs the required pulses for controlling core-storage writing and reading.

3-33. CONTROL SECTION REGISTERS. The registers in the control section are the transfer register (T-register), memory address register (M-register), program address register (P-register), and instruction register (I-register).

3-34. T-Register. The T-register receives 16-bit words which will be stored in, or which have been read from, the memory section (see figure 3-1). The various stages of the T-register are on four arithmetic logic cards, with reference designations A102, A103, A104, and A105.

3-35. M-Register. The M-register specifies the core memory address in which a word will be stored, or from which a word will be retrieved (see figure 3-1). The various stages of the M-register are on arithmetic logic cards A102, A103, A104, and A105.

3-36. P-Register. The P-register specifies the core memory address from which the next instruction word will be read (see figure 3-1). When the P-register contents are used, they are gated onto the R bus, passed through the arithmetic gates, and gated into the M-register. From here, the address is forwarded to the memory section.

3-37. I-Register. The I-register is a 6-bit register which receives bits 15 through 10 of each instruction word read from the memory section (see figure 3-1). The I-register holds these bits while they are decoded by the instruction decoder. The register is on instruction decoder card A107.

3-38. INSTRUCTION DECODER. The instruction decoder examines each instruction word read from the memory section, and produces control pulses in accordance with the type of instruction indicated. These pulses activate flip-flops, gates, and registers in the memory, arithmetic, control, and I/O sections to bring about the functions required by the instruction.

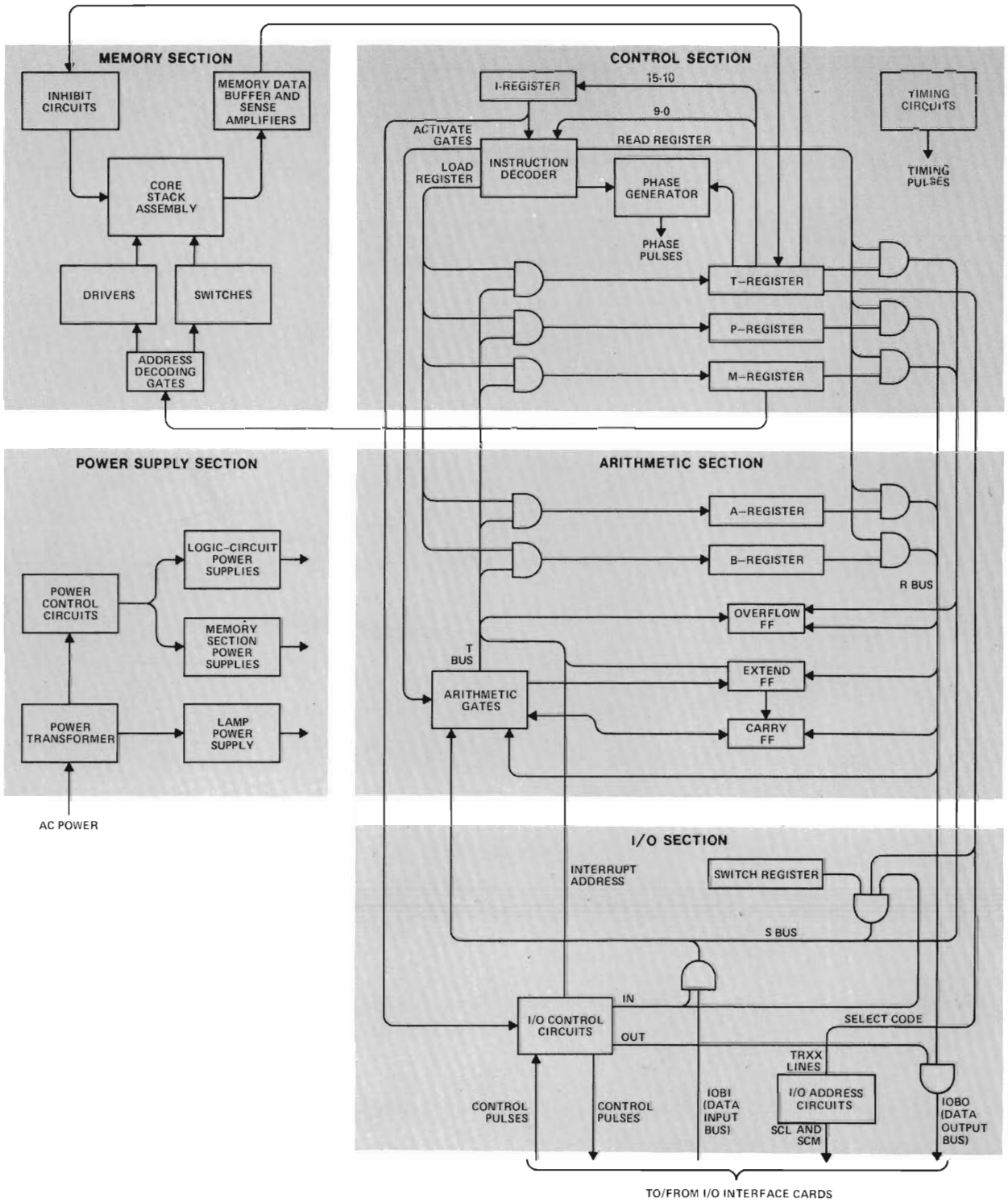

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Figure 3-1. 2116C Computer, Functional Block Diagram

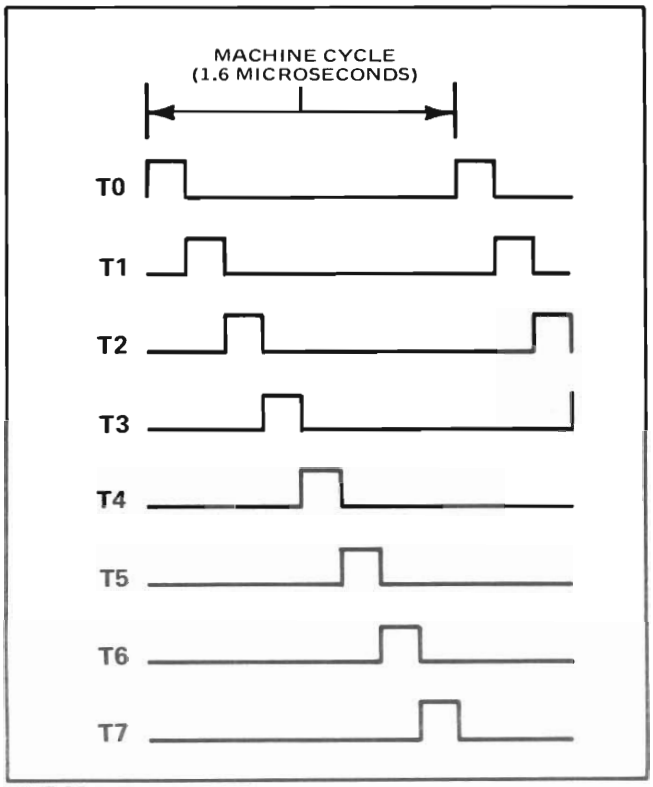

Figure 3-2. Clock Pulses

3-39. When an instruction word is read from the memory section, it is placed in the T-register (see figure 3-1). Bits 15 through 10 are forwarded to the 6-bit I-register, and from there to the instruction decoder. Bits 9 through 0 of the T-register are furnished directly to the instruction decoder.

3-40. To bring about the functions required by each instruction, the instruction decoder gates register contents onto the R bus or S bus, loads registers from the T bus, and activates the arithmetic gates.

3-41. In the case of a memory reference instruction, the instruction decoder brings about the reading of the required word from the memory section. This is done by activating the memory timing circuits with appropriate control pulses. The word read is placed in the T-register. This destroys the instruction word itself. However, six bits of the word remain in the I-register. These bits, together with various flip-flops set earlier in the instruction, control the computer during the remainder of the instruction.

3-42. The instruction decoder is on instruction decoder card A107 and shift logic card A108.

3-43. PHASE GENERATOR. The phase generator, situated on timing generator card A106, produces four pulse-type signals which determine the basic function performed by the computer during each 1.6-microsecond machine cycle. The four signals are named phase 1, 2, 3, and 4, in accordance with the four types of machine cycle. These machine cycles serve the following purpose:

a. Phase 1, referred to as the fetch phase, is the machine cyle in which an instruction word is obtained from the memory section. This is the first phase of each instruction, and in some cases the entire instruction is completed during this machine cycle.

b. Phase 2, called the indirect phase, is used when indirect addressing is indicated by the instruction word. (Bit 15 of the word, when logic 1, specifies indirect addressing.) Indirect addressing is used only with memory reference instructions. In instruction words of this type, bits 9 through 0 normally are an operand address. With indirect addressing, however, the word in the memory location indicated by these bits is itself used as an operand address. Another reference is then made to the memory section to obtain the operand. The computer is in phase 2 for the machine cycle during which the 16-bit operand-address word is obtained from the memory section. Multiple-step indirect addressing is also possible. If bit 15 of the word obtained during phase 2 is logic 1, another phase 2 machine cycle is performed, and the word acquired in the first phase 2 is used as the address from which another operand-address word is obtained. Phase 2 machine cycles continue until a word is acquired in which bit 15 is a logic 0.

c. Phase 3, the execute phase, is a machine cycle in which the computer acquires an operand from core storage. During the latter part of phase 3 the computer operates on the operand as indicated by the instruction word acquired in the preceding fetch phase.

d. Phase 4, the interrupt phase, results from an interrupt initiated by an optional device or it is the result of a power fail interrupt. Phase 4 interrupts the computer program for performance of an instruction stored at the core memory location corresponding to the type of interrupt. These core locations, in descending interrupt priority, are as follows:

(1) Core location 00004 (octal), power fail interrupt.

(2) Core location 00005 (octal), memory protect interrupt or memory parity error interrupt.

(3) Core locations 00006 and 00007 (octal), interrupt occurring after all words have been transferred in a DMA (direct memory access) operation. Core location 00006 is used at the end of a DMA channel 1 operation, and location 00007 is used at the end of a channel 2 operation.

(4) Core locations 00010 through 00077 (octal), interrupts from I/O devices.

3-44. In phase 4 the address corresponding to the type of interrupt is placed in the M-register (figure 3-1). The computer then enters the fetch phase, acquires an instruction word from the specified address, and acts in accord-

ance with the instruction. Normally this instruction is JSB, and it takes the computer to a subroutine corresponding to the type of interrupt. At the end of the subroutine the computer will usually be returned to the program that was interrupted, the return address having been stored by the JSB instruction. In the case of a power fail interrupt, however, the power fail subroutine must end with an HLT instruction, otherwise data in core storage may be destroyed during power shut-down. If there is no power fail subroutine in the computer, core location 00004 (octal) must contain an HLT instruction.

3-45. An additional phase, phase 5, is used for DMA operations. This phase is used each time the DMA system reads or writes a word in core memory.

3-46. The computer can be in only one phase at a time. Phase 2, if performed, follows phase 1 or a prior phase 2. Phase 3 follows phase 1 or phase 2. The last phase of an instruction is phase 1 (for a single-phase instruction), or phase 3 (for a multiple-phase instruction).

3-47. The FETCH, INDIRECT, or EXECUTE lamp on display board assembly A501 lights when the computer is in the fetch, indirect, or execute phase. Because of the speed of operation of the computer, these lamps serve a useful function only when the computer is stopped or when it is being stepped with the SINGLE CYCLE switch.

3-48. ARITHMETIC SECTION.

3-49. The arithmetic section of the computer performs the addition, subtraction, or other data manipulation for each instruction requiring such operations. The data manipulation is performed by three major circuit groups: the accumulators, the computational registers, and the arithmetic gates.

3-50. ACCUMULATORS. The computer has two accumulators: the A-register and the B-register. Each accumulator holds a 16-bit data word before, during, and after the performance of data manipulation on the word.

3-51. When using an instruction that uses an accumulator, only one accumulator is normally used. That accumulator being specified by bit 11 of the instruction word. However, the address portion of the instruction word can specify the address of the other accumulator, thereby permitting inter-accumulator operations. For instance, the contents of the A-register can be compared with the contents of the B-register, by using a Compare A (CPA) instruction with the address portion of the instruction specifying the B-register address.

3-52. The address of the A-register for inter-accumulator operations is 00000 (octal). The address of the B-register is 00001 (octal).

3-53. The various stages of the two accumulators are on arithmetic logic cards A102, A103, A104, and A105.

3-54. COMPUTATIONAL REGISTERS. Three 1-bit computational registers aid in performing data manipulation and recording the results obtained. The registers are the Overflow, Extend, and Carry FFs. The Overflow FF is used to hold control information and to record positive arithmetic overflows from the accumulators. The Extend FF detects a carry from position 15 of the accumulators, and links the two accumulators during ELA/B and ERA/B instructions. The Carry FF, when set, indicates that a program skip will take place.

3-55. Lamps on display board assembly A501 light when the Overflow FF or Extend FF is set.

3-56. The Overflow, Extend, and Carry FFs are on shift logic card A108.

3-57. ARITHMETIC GATES. The principal data-manipulations in the computer are performed by the arithmetic gates (figure 3-1). The gates use timing and control signals to regulate the transfer of 16-bit (parallel) data words from the R and S buses to the T bus. In doing this, the gates can perform any of the following arithmetic operations:

a. Add the number on the R bus to the number on the S bus.

b. Add 1 or 2 to the number on the R bus.

c. Combine the number on the R bus with the number on the S bus, using any of the following logic functions:

(1) "And."
(2) Inclusive "or."
(3) Exclusive "or."

d. Complement the number on the R bus.

e. Shift the number on the R bus to the right one position, to the left one position, or to the left four positions.

f. Transfer data unchanged from the R or S bus to the T bus.

3-58. After passing through the arithmetic gates, data can be loaded into the T-register, P-register, M-register, A-register, B-register, Overflow FF, Extend FF, or Carry FF.

3-59. MEMORY SECTION.

3-60. Before reading the theory discussion of the memory section, the reader must be familiar with the principles of core storage memories. An explanation of this type of storage device can be found in most text books dealing with the basics of digital computers.

3-61. The 2116C memory section employs core storage units of the conventional coincident-current parallel-readout type. Employment of a single wire for sensing

and for write inhibiting permits the use of only three wires through each core, rather than the more usual four wires.

3-62. In its basic configuration, the computer has one 8,192-word (8K) core stack. This core stack, together with its associated sense amplifiers, is situated on sense amplifier card A20. To complete the memory section, X-Y driver switch card A21, and inhibit driver card A22, are provided. As optional features, one, two, or three additional sense amplifier cards, each with an attendant X-Y driver card and an inhibit driver card, can be installed in the computer. Each additional set of three cards furnishes 8K of added storage capacity.

3-63. The discussion which follows deals with a memory section incorporating the full storage capacity (32K) of which the 2116C is capable. If the computer has only 8K, 16K, or 24K of storage capacity, references to memory cards and storage addresses beyond the installed capacity do not apply.

3-64. Each core stack includes provisions for storing a parity bit with each word. Use of the parity bit is an optional feature, and the circuit theory of this facility is covered in the Operating and Service Manual for the Parity Error Option.

3-65. CORE STACK CONSTRUCTION. Each 8K core stack is made up of ferrite cores which provide 8,192 word-storage locations. Each word location consists of 17 ferrite cores. Of these, 16 are used for storing a word, while the remaining core is reserved for the parity bit. If the circuit card for the Parity Error Option is not installed, the 17th core remains unused.

3-66. ORGANIZATION OF DATA. The word locations in each core stack are divided into two 4K groups, referred to as the lower module and the upper module. (The terms "lower" and "upper" refer to address assignments, rather than to the physical arrangement of word locations in each core stack.) The octal addresses in each module of each core stack are listed in table 3-1. In the table, core stacks are identified by the reference designation of the sense amplifier card on which they are installed. It will be noted that the lowest address in the table is 00002. Addresses 00000 and 00001 are used for addressing the A-register and B-register, respectively.

3-67. In each module word locations are divided into four pages, each containing 1,024 (decimal) words. The eight pages in each core stack are illustrated in figure 3-3.

3-68. ADDRESSING METHOD. Memory addressing utilizes two address formats. These are described in the following paragraphs.

3-69. Full Address Word. Figure 3-4 shows the address word used by the computer. Bit 15 is the direct/indirect (D/I) bit. The function of this bit is described in a later paragraph. Bits 14 and 13 designate the core stack to be used. Bits 12, 11, and 10 identify the page in the stack. Bits 9 through 0 specify the location within the page. Table 3-2 lists the address range (first and last address) of each page of the four core stacks.

3-70. Addressing by Instruction Word. Memory reference instructions specify a partial core address. This permits the 16-bit instruction word to include in its structure an operation code as well as a memory address. The format is shown in figure 3-5. Bit 15 is the direct/indirect bit, and bits 14 through 11 constitute the operation code. Bits 9 through 0 identify the address within the page (see table 3-2). The page to be used can be specified in any of three ways, as described below:

a. In the first method, bit 10 of the instruction word (the zero/current bit) is logic 1, and the direct/indirect bit is logic 0. The instruction makes reference to a location in

Table 3-1. Stack and Module Address Assignments

CORE STACK	MODULE	
	LOWER	UPPER
A20	00002 thru 07777	10000 thru 17777
A19	20000 thru 27777	30000 thru 37777
A10	40000 thru 47777	50000 thru 57777
A9	60000 thru 67777	70000 thru 77777

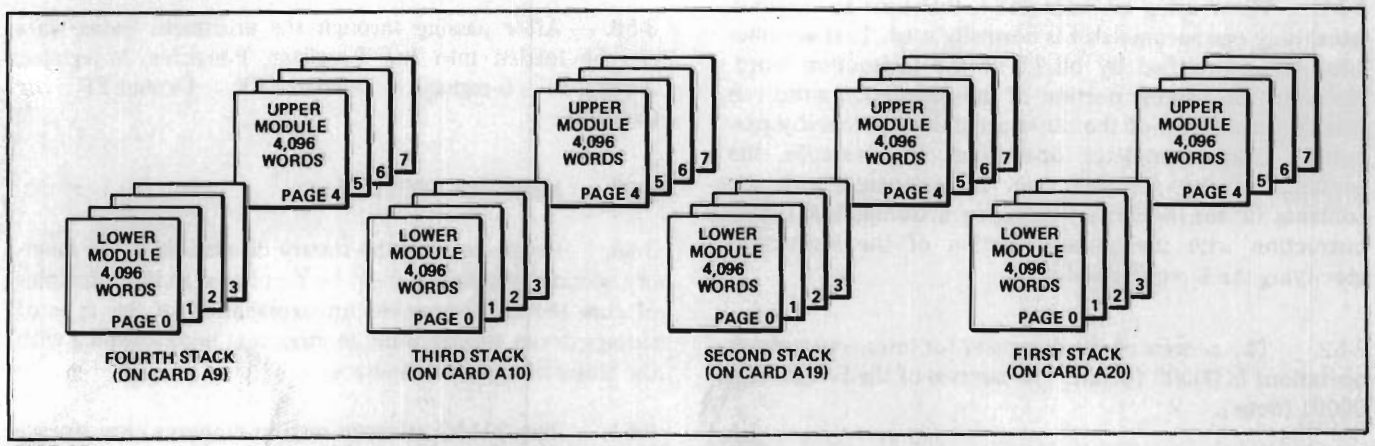

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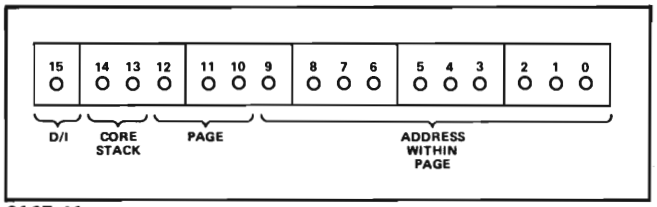
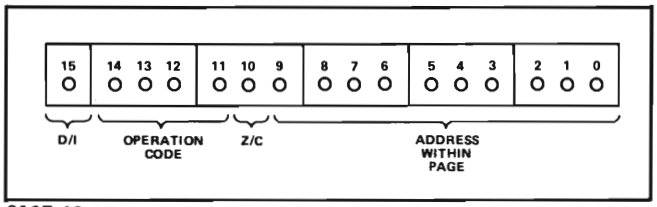
Figure 3-3. Core Stack Pages



2107-41

Figure 3-4. Format of Address Word



2107-42

Figure 3-5. Format of Memory Reference Instruction Word

Table 3-2. Core Storage Addresses

STACK	MODULE	PAGE	ADDRESS RANGE (OCTAL)	ADDRESS WORD (BINARY)															
				D/I	ADDRESS RANGE (BINARY)														
					STACK		PAGE			ADDRESS WITHIN PAGE									
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A20	Lower	0	00002	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
			01777	0/1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
A20	Lower	1	02000	0/1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
			03777	0/1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
A20	Lower	2	04000	0/1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
			05777	0/1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
A20	Lower	3	06000	0/1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
			07777	0/1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
A20	Upper	4	10000	0/1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
			11777	0/1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
A20	Upper	5	12000	0/1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
			13777	0/1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
A20	Upper	6	14000	0/1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
			15777	0/1	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
A20	Upper	7	16000	0/1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
			17777	0/1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
A19	Lower	0	20000	0/1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
			21777	0/1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
A19	Lower	1	22000	0/1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
			23777	0/1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
A19	Lower	2	24000	0/1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
			25777	0/1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1
A19	Lower	3	26000	0/1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
			27777	0/1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
A19	Upper	4	30000	0/1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
			31777	0/1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1
A19	Upper	5	32000	0/1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
			33777	0/1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
A19	Upper	6	34000	0/1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
			35777	0/1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
A19	Upper	7	36000	0/1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
			37777	0/1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 3-2. Core Storage Addresses (Continued)

STACK	MODULE	PAGE	ADDRESS RANGE (OCTAL)	ADDRESS WORD (BINARY)															
				D/I	ADDRESS RANGE (BINARY)														
					STACK		PAGE			ADDRESS WITHIN PAGE									
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A10	Lower	0	40000	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			41777	0/1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1
A10	Lower	1	42000	0/1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
			43777	0/1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
A10	Lower	2	44000	0/1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
			45777	0/1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1
A10	Lower	3	46000	0/1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
			47777	0/1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
A10	Upper	4	50000	0/1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
			51777	0/1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
A10	Upper	5	52000	0/1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
			53777	0/1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
A10	Upper	6	54000	0/1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
			55777	0/1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
A10	Upper	7	56000	0/1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
			57777	0/1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
A9	Lower	0	60000	0/1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
			61777	0/1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
A9	Lower	1	62000	0/1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
			63777	0/1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
A9	Lower	2	64000	0/1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
			65777	0/1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1
A9	Lower	3	66000	0/1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
			67777	0/1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
A9	Upper	4	70000	0/1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
			71777	0/1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
A9	Upper	5	72000	0/1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
			73777	0/1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
A9	Upper	6	74000	0/1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
			75777	0/1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
A9	Upper	7	76000	0/1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
			77777	0/1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: Core stacks are identified by the reference designation of the card on which they are mounted.

the current page. That is, to the page in which the instruction word itself is located.

b. In the second addressing method, the zero/current bit is logic 0, and the direct/indirect bit is logic 0. The instruction makes reference to page 0 of the core stack on card A20. The octal address is therefore in the range 00002 through 01777, with bits 9 through 0 of the instruction word specifying the low-order 10 bits of the address.

c. The third addressing method used by memory reference instructions is indirect addressing. In this type of operation the zero/current bit of the instruction word can be logic 0 or logic 1; the direct/indirect bit is logic 1. The instruction acquires a 16-bit word from page 0 or the current page, as determined by the zero/current bit. If bit 15 of the acquired word is logic 0, bits 14 through 0 of the word are used as a full address word for carrying out the memory reference operation specified by the instruction

word. By this means any word-location in the memory section can be referenced. If bit 15 of the acquired word is logic 1, another 16-bit word is acquired, using the word-location specified by the first word read from the memory section. The new word, in turn, is used as an address word. This process continues until a 16-bit word is obtained in which bit 15 is logic 0. This full address word is then used by the instruction to carry out its particular memory reference operation.

3-71. MEMORY READ OPERATIONS. When a word is to be read from the core stack assembly, its address is first placed in the 16-bit M-register (refer to figure 3-1). The address is then forwarded to the memory section, the word is acquired from the specified word-location, and the T-register receives the word read. This operation is performed for each of the three basic types of readout operation which are as follows:

a. Readout of a word for display by the T-register lamps.

b. Readout of an instruction word to be executed by the computer.

c. Readout of an operand which will be used by an instruction.

3-72. Readout for Display. When a word is to be displayed in the T-register the computer must be stopped because the controls which bring about readout are disabled when the computer is running. The readout for display is brought about by setting into the SWITCH REGISTER switches the address of the required word. The LOAD ADDRESS switch is pressed, then the DISPLAY MEMORY switch. When the LOAD ADDRESS switch is pressed, the number in the switch register is placed on the S bus. From there it passes unchanged through the arithmetic gates, and is loaded into the M-register.

3-73. When the DISPLAY MEMORY switch is pressed, the address decoding gates in the memory section decode the contents of the M-register, and the word at the specified address is read from memory by a selected driver and switch. The word is sensed by the sense amplifiers, and placed in the T-register. The word is then available for visual inspection in the T-register display lamps.

3-74. The memory readout operation leaves zeros in the 16 ferrite cores at the addressed location. Therefore, it is necessary to rewrite the word in these cores. This is done immediately after the memory readout has taken place, and occurs without manual intervention by the operator. Immediately after the readout operation the M-register still indicates the addressed location, and the memory timing circuits restore the word in the memory section by attempting to store logic 1 in each bit position of the addressed word-location. However, the inhibit circuits prevent this in the ferrite cores that originally contained logic 0. The word that was read out is in the T-register, and from this word the inhibit circuits determine the cores that must remain in the logic 0 state.

3-75. Instruction-Word Readout. The second type of memory readout occurs when the computer acquires an instruction word to be performed. At the end of the preceding instruction, the address of the next instruction word is placed in the M- and P-registers. When the new instruction starts, the contents of the M-register are decoded in the memory section, and the word is read from its memory location and rewritten. In this case, after the word is placed in the T-register, bits 15 through 10 are forwarded to the I-register, and the I-register and T-register contents are decoded to determine the kind of instruction to be performed. The readout and decoding of the instruction word take place in phase 1, the fetch phase.

3-76. In the type of memory readout described earlier, a word was acquired from the memory section for display purposes. This operation was not followed by decoding of the word by the instruction decoder. It is the decoding process which brings about actions in the computer under control of the instruction, and this is the distinguishing feature between words treated as data and words which are handled as instructions. A word acquired during phase 1 is decoded; words acquired during other phases are not decoded.

3-77. Operand Readout. The third method of addressing a core memory location is used by memory reference instructions. Instructions of this type acquire an operand from the memory section, and perform an arithmetic or logic operation using the operand. The operand word is acquired either by direct addressing or by indirect addressing, as designated by bit 15 of the instruction word. If bit 15 is logic 0, the operand is acquired from the memory section by direct addressing. If the bit is logic 1, indirect addressing is employed.

3-78. When direct addressing is used, the computer enters phase 3 (the execute phase) after acquiring and decoding the instruction word in phase 1. In phase 3 the operand is acquired from the memory section, and acted upon in accordance with the type of instruction being performed.

3-79. When direct addressing is used, the operand must be obtained either from page 0 of the first core stack, or from the page in which the instruction word is located. Bit 10 of the instruction word identifies the page to be used, logic 0 indicating page 0 and logic 1 the current page.

3-80. When the instruction word is acquired from the memory section, it is placed in the T-register (figure 3-1). When the word is decoded and found to be a memory reference instruction, bits 9 through 0 of the T-register are gated onto the S bus, passed unchanged through the arithmetic gates, and are loaded into the M-register. This takes place near the end of phase 1. If the memory page being

referenced is the current page, positions 15 through 10 of the M-register retain the contents they had when the instruction word was acquired. These bits designate the core stack, module, and page to be referenced, and since they remain unchanged, the operand is obtained from the page in which the instruction word is stored. If bit 10 of the instruction word indicates page 0, bits 15 through 10 of the M-register are cleared, and page 0 of the first core stack is referenced.

3-81. After the M-register is loaded, the computer enters phase 3, and the referenced word is acquired from the memory section. The use then made of the operand depends on the type of instruction being performed.

3-82. Near the end of phase 3, the M-register is loaded with the address of the next instruction. This is done by passing the P-register contents through the arithmetic gates (figure 3-1) into the M-register. As the number passes through the arithmetic gates, it is incremented by 1. As well as being loaded into the M-register, the incremented number replaces the original contents of the P-register, keeping the P-register contents current as the program advances.

3-83. With indirect addressing, the instruction word is acquired from the memory section and placed in the T-register as before. The M-register is also loaded with the operand address in the same manner as for direct instruction addressing. However, because bit 15 of the instruction word is logic 1, the computer enters phase 2 (the indirect phase) after the completion of phase 1. In phase 2 the referenced word is acquired from page 0 or the current page and placed in the T-register as before. However, the word acquired is not treated as an operand to be operated on by the instruction, nor is it handled as an instruction word. Instead, it is forwarded to the M-register and treated as an address word. This time, bits 14 through 0, rather than 9 through 0, are routed from the T-register to the M-register. Consequently, any address in any core stack can be referrenced.

3-84. When the word is acquired from the memory section during phase 2, it is placed in the T-register in the normal way. Bit 15 of the word is then checked to determine whether another indirect addressing operation is to be performed. If bit 15 is logic 1, the new word is treated as an address word, the full computer word is forwarded to the M-register, and another phase 2 machine cycle is performed. The computer continues to perform phase 2 machine cycles until a word is acquired in which bit 15 is logic 0. The computer then enters a phase 3 machine cycle, and the word acquired in the last phase 2 cycle is treated as an operand address.

3-85. MEMORY WRITE OPERATIONS. Memory write operations are very similar to memory read operations. During the processing of a memory reference instruction, such as Store the A-register (STA), bits 9 through 0 of the instruction word (brought from memory to the T-register during phase one) are routed from the T-register to the M-register during phase 1 (figure 3-1). This establishes the memory address of the data to be manipulated during phase 3 of the memory reference instruction. During phase 3, the word to be written into memory is gated onto the T-bus and into the T-register. A memory cycle is initiated and during the read portion of this cycle the data in the addressed memory location is inhibited from being gated into the T-register. During the write portion of the memory cycle the new data currently in the T-register is gated into the addressed memory location via the inhibit driver circuits thus destroying the old data in that location and replacing it with new data. The same phase 3 operations take place when the LOAD MEMORY switch is pressed.

3-86. PROGRAM FOLDOVER. If the computer has less than 32K of storage capacity, an attempt to read or write at an address beyond the installed capacity will result in reading or writing from an address that is within the installed capacity. In doing this, the computer ignores the high-order bits of the address, and uses only the bits which apply to the installed capacity. This effect, referred to as foldover, can occur only with improper indirect addressing within an operating program (such as a program configured for a 32K computer being run on a 24K computer) or with improper addressing from the switch register by the person operating the computer. Once foldover has occurred, and the program has returned to direct addressing, the computer will read or write in the normal manner but in the area it has been forced into by the foldover effect. If the program has no data checking routines, no error conditions will occur and the program will continue to operate using the data in the foldover area of memory.

3-87. INPUT/OUTPUT SECTION.

3-88. The general theory of the input/output section is covered in Volume III, 2116C Computer Input/Output System Operation. Detailed circuit theory is dealt with later in this section.

3-89. POWER SUPPLY SECTION.

3-90. The power supply section of the 2116C computer provides the regulated and unregulated dc voltages required by the computer. Protective circuits are included, which remove dc power from the computer in the event of excessive heat in the computer cabinet, low ac line-voltage, excessively low or high dc voltage, or excessive dc current.

3-91. Optional circuit cards which install in the computer cabinet receive their operating voltages from the 2116C power supply section. If these optional cards require more power than the power supply section is capable of furnishing, an auxiliary power source (referred to as a power supply extender), installed in a separate cabinet, provides additional dc power. The externally-furnished voltages connect in parallel with the corresponding dc voltages produced in the 2116C power supply.

3-92. Optional I/O devices and extender units provide their own ac and dc operating voltages, derived from a separate connection to the ac power line.

3-93. The power supply section furnishes the following dc voltages to other sections of the computer:

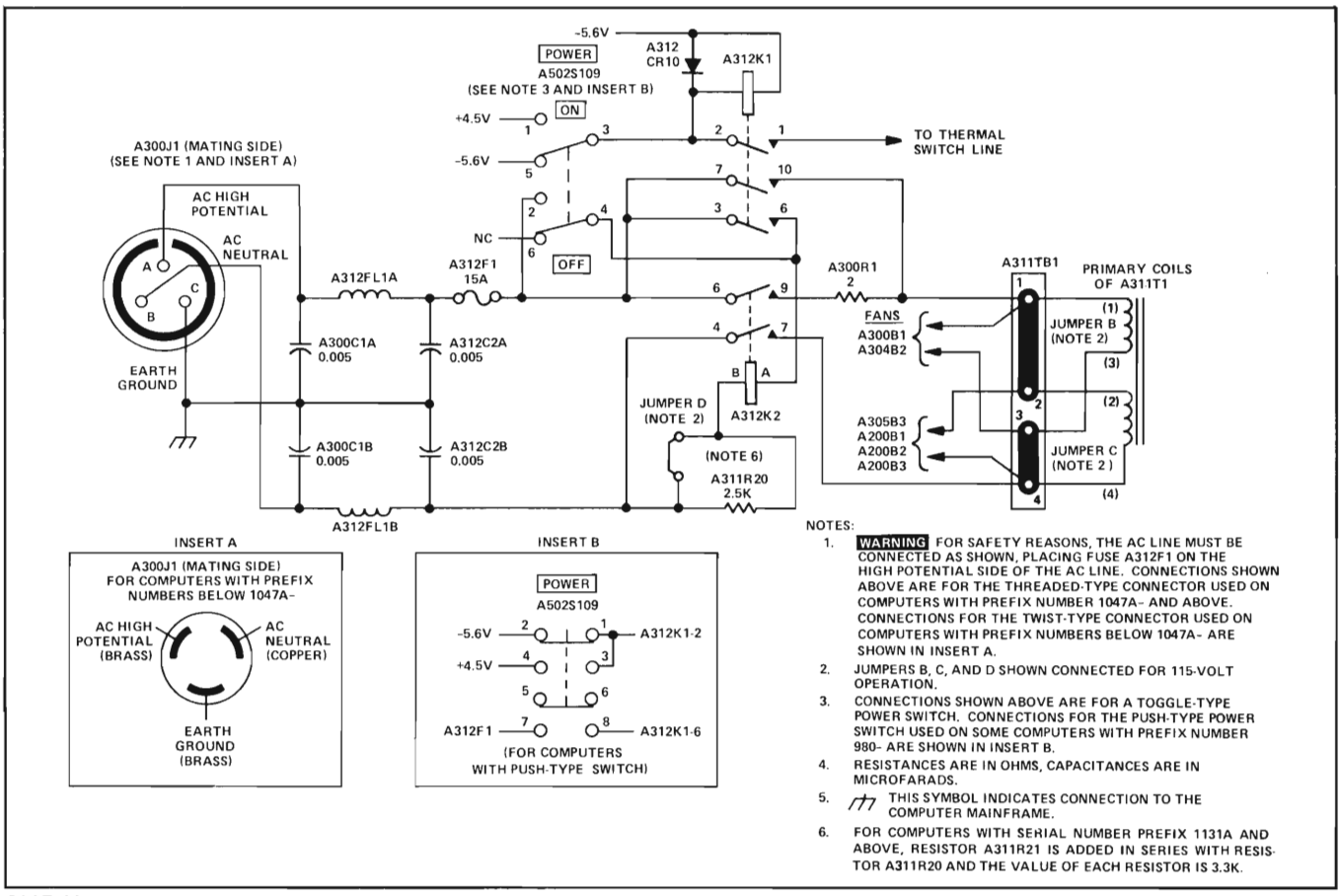
a. -2 volts regulated.
b. +4.5 volts regulated.
c. +7 volts unregulated.
d. +12 volts regulated.
e. -12 volts regulated.
f. +20 volts regulated.
g. -20 volts regulated.
h. +32 volts regulated.
i. +35 volts unregulated.

3-94. Additional dc voltages are produced for use within the power supply section itself.

3-95. AC DISTRIBUTION. The distribution of ac power in the computer is shown in figure 3-6. All components shown in the illustration are part of the power supply assembly, with the exception of POWER switch A502S109 and fans A200B1, A200B2, and A200B3. The POWER switch is on control panel assembly A502, and the fans are at the bottom of the card cage assembly.

3-96. The ac operating power for the computer, single-phase 115 volts or single-phase 230 volts if option 15 is installed, is furnished to connector A300J1 (figure 3-6). POWER switch A502S109 applies or removes this power from the power supply section. As noted in figure 3-6, early computers are equipped with a push-type POWER switch. One push on the face of this type switch causes its movable contacts to lock in the "on" position; a second push releases these contacts allowing them to return to the "off" position. (All switch and relay contacts shown in figure 3-6 are in the off or de-energized position.) The push-type POWER switch assembly includes indicator lamp A502DS109 (not shown in figure 3-6). This lamp, located behind the switch face, operates from the +12-volt supply and lights to indicate when computer power is turned on. It extinguishes when computer power, and hence the +12-volt supply, is turned off. Later computers are equipped with a conventional two-position toggle-type POWER switch. Power status for these computers is indicated by ON and OFF panel markings corresponding to the appropriate setting of the toggle.

3-97. AC Power Turn-On. When the POWER switch is actuated to turn on computer power, ac power is applied through fuse A312F1 to the coil of relay A312K2. The coil is designed for 115-volt ac operation; for 230-volt use, resistor A311R20 reduces the applied voltage to a suitable level. The contacts of A312K2 apply ac line voltage to the primary of transformer A311T1 and to the six cooling fans in the computer. The transformer then furnishes low-voltage ac power to all power supplies. Resistor A300R1



NOTES:
1. WARNING FOR SAFETY REASONS, THE AC LINE MUST BE CONNECTED AS SHOWN, PLACING FUSE A312F1 ON THE HIGH POTENTIAL SIDE OF THE AC LINE. CONNECTIONS SHOWN ABOVE ARE FOR THE THREADED-TYPE CONNECTOR USED ON COMPUTERS WITH PREFIX NUMBER 1047A- AND ABOVE. CONNECTIONS FOR THE TWIST-TYPE CONNECTOR USED ON COMPUTERS WITH PREFIX NUMBERS BELOW 1047A- ARE SHOWN IN INSERT A.
2. JUMPERS B, C, AND D SHOWN CONNECTED FOR 115-VOLT OPERATION.
3. CONNECTIONS SHOWN ABOVE ARE FOR A TOGGLE-TYPE POWER SWITCH. CONNECTIONS FOR THE PUSH-TYPE POWER SWITCH USED ON SOME COMPUTERS WITH PREFIX NUMBER 980- ARE SHOWN IN INSERT B.
4. RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
5. /// THIS SYMBOL INDICATES CONNECTION TO THE COMPUTER MAINFRAME.
6. FOR COMPUTERS WITH SERIAL NUMBER PREFIX 1131A AND ABOVE, RESISTOR A311R21 IS ADDED IN SERIES WITH RESISTOR A311R20 AND THE VALUE OF EACH RESISTOR IS 3.3K.

2107-43B

Figure 3-6. AC Distribution

reduces the initial ac line current as power supply filter capacitors acquire a charge.

3-98. When filter capacitors become substantially charged, -5.6 and +4.5 volts become available; relay A312K1 then energizes and resistor A300R1 is shorted out. Full ac voltage is applied to transformer A311T1, and power control circuits make dc voltages available to the computer in a predetermined sequence.

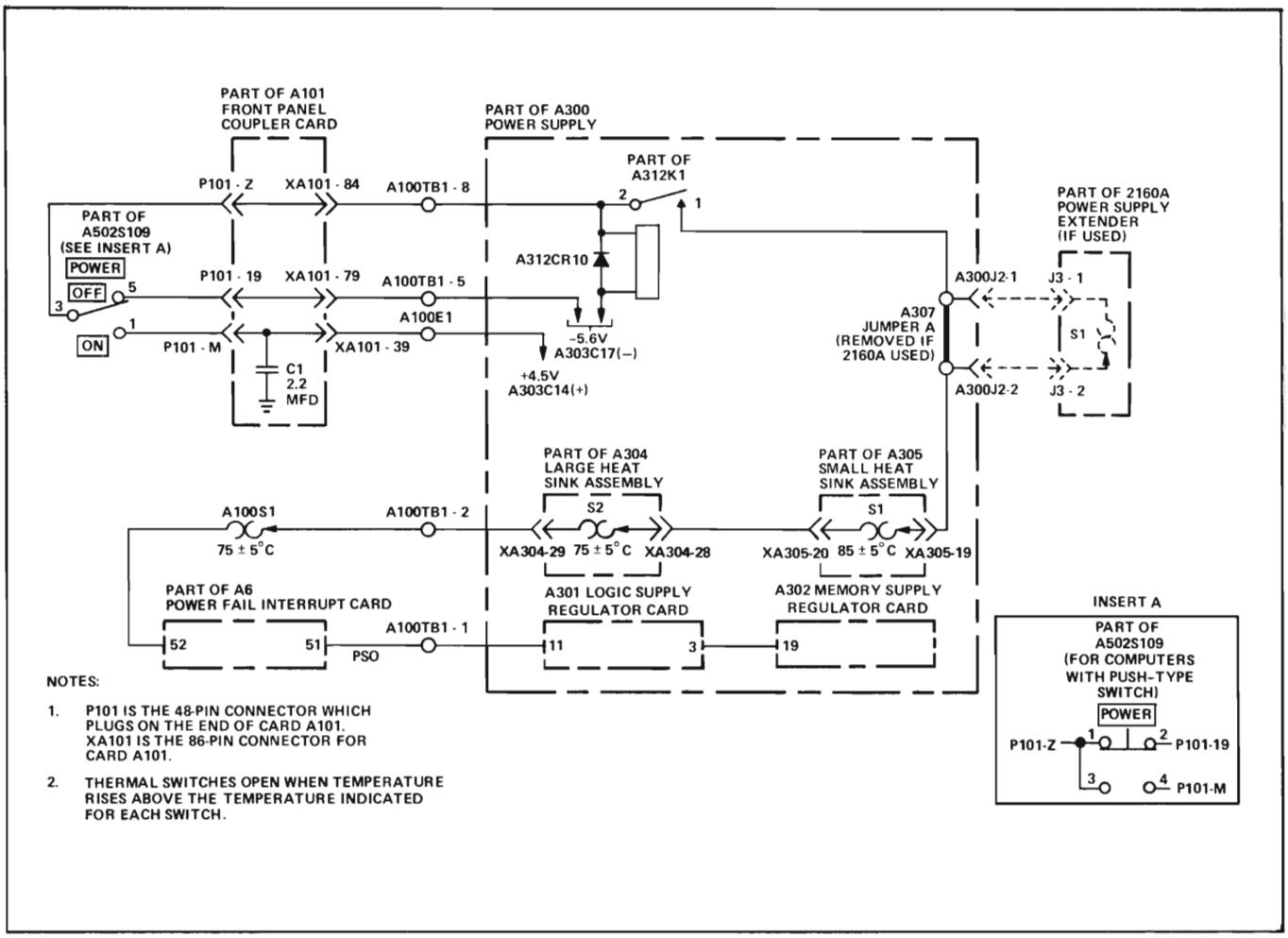
3-99. AC Power Shut-Down. When the POWER switch is actuated to turn off computer power, +4.5 volts is removed from the coil of A312K1. Diode A312CR10 provides a path for the current induced in the relay coil by its own collapsing magnetic field. Because of this path for current, arcing at the contacts of the POWER switch is eliminated, and voltage spikes are not applied to the transistor at the end of the thermal switch line. Approximately 50 milliseconds after the POWER switch is actuated, relay A312K1 de-energizes. Contacts 3 and 6 of the relay then remove actuating voltage from the coil of relay A312K2; relay A312K2 de-energizes about 15 milliseconds later, removing ac power from transformer A311T1 and the fans. It will be noted that contacts 3 and 6 of relay A312K1 are in parallel with the ac power contacts of the POWER switch. Because of this parallel connection, A312K2 remains energized until A312K1 de-energizes. This prevents the autorestart option (if installed in the computer) from attempting to turn on power during the power-off process.

3-100. DC POWER CONTROL. Figure 3-7 shows the manner in which dc power is applied to and removed from the computer.

3-101. DC Power Turn-On. As noted earlier, relay A312K1 energizes when ac power is initially turned on. Contacts 2 and 1 of the relay furnish +4.5 volts through normally-closed thermal switches to power fail interrupt card A6. Circuits on this card produce a true PSO signal, which is forwarded to logic supply regulator card A301.

3-102. After the PSO signal becomes true, regulated -2 volts is furnished to the computer. The dc power control circuits then furnish the computer with the remaining five regulated voltages. These are supplied in a predetermined sequence. Then, if all thermal switches shown in figure 3-7 are closed, the computer is ready for use. The computer is in the halted condition, and the following indicators are lighted; PRESET, HALT, FETCH and POWER if included. Register display lamps on display board assembly A501 are lighted or off in a random pattern.

3-103. If one or more thermal switches are open during the power-on sequence, or if any of the regulated voltages is



2107-48A

Figure 3-7. DC Power Control Circuits

not furnished, the dc shut-down sequence is initiated. Shut-down starts about 300 ms after regulated +4.5 volts is made available. If +4.5 or -5.6 volts is not available, relay A312K1 remains de-energized and the dc power-on sequence does not start.

3-104. DC Power Shut-Down. When the ac power is initially turned off, relay A312K1 remains energized for about 50 milliseconds as the magnetic field about the relay coil collapses. However, the open contacts of the POWER switch (figure 3-7) immediately remove +4.5 volts from pin 52 of power fail interrupt card A6. As a result, card A6 generates a power fail program interrupt. Then, if programmed to do so and if it is running, the computer stores register contents and performs other actions in preparation for later startup. (It is advisable to stop the program before turning power off, otherwise information in core storage may be destroyed during dc power shut-down. Also to protect data in core storage, the power-failure program should end with an HLT instruction. If there is no power-failure program in the computer, core storage location 00004 should contain the HLT instruction.)

3-105. In the event of complete loss of ac line voltage, power fail interrupt card A6 generates a power fail interrupt. Then, when filter capacitors can no longer maintain the required voltage levels, the dc shut-down sequence is performed. The filter capacitors and voltage regulators can maintain full voltage, under maximum dc load conditions, for at least 1 millisecond after complete and sudden failure of ac line voltage. Therefore, the power-fail interrupt program must be completed within this time. When the ac line voltage returns to normal, dc voltages are again supplied to the computer circuits, but the computer is halted. This halt condition exists regardless of whether the computer was running prior to dc shut-down.

3-106. If the ac line voltage drops below a level which is between 100 and 102 volts rms (200 to 204 volts for a 230-volt computer), a power fail interrupt occurs, Then, if the computer is running and a power-fail interrupt program is stored in the memory section, the program is performed. If the ac line voltage continues to fall and drops below approximately 75 volts rms (150 volts for a 230-volt computer), dc shut-down takes place and dc voltages are removed from the computer circuits. When line voltage returns to normal dc voltages are re-applied, but the computer is halted.

3-107. Thermal switches A305S1, A304S2, and A100S1 (figure 3-7) remove dc power from the computer in the event of overheating during operation. When overheating occurs, one of the thermal switches opens, +4.5 volts is removed from card A6, and a power-fail interrupt takes place. Eight milliseconds later the PSO signal becomes false, and the dc shut-down sequence is initiated. In this case, relay A312K1 remains energized, ac distribution in the computer remains unchanged (figure 3-7), and the fans in the computer cabinet maintain their cooling function. When the thermal switch closes the normal dc power-on sequence is performed, but the computer is halted.

3-108. In addition to low line voltage and overheating, a third fault can cause dc power shut-down. If one of the dc regulated voltages fails, partial or complete shut-down of the remaining regulated voltages takes place.

3-109. Specific information on the dc turn-on and shut-down sequence is presented later in this section.

3-110. +7 VOLT POWER SUPPLY. The +7 volt power supply furnishes unregulated and unfiltered dc voltage. This voltage is used for lighting all lamps on display panel assembly A501 and control panel assembly A502 (with the exception of the POWER indicator which, if present, is powered by +12 volts). No other use is made of the +7 volt power.

3-111. +4.5 VOLT AND -2 VOLT POWER SUPPLIES. The +4.5 volt and -2 volt power supplies furnish the operating voltages required by the logic circuits in the computer. (Logic elements on power fail interrupt card A6 and certain I/O interface cards require +12 volts as well.) A block diagram of the +4.5 and -2 volt power supplies is presented in figure 3-8. The diagram is simplified to the extend that the common, tapped transformer secondary used by both power supplies is not indicated. Unregulated voltages shown in figure 3-8 are approximate, and will vary in accordance with component differences, the amount of current required for optional devices, and the power-line voltage.

3-112. The +4.5 volt power source and the +4.5 volt regulator make up the +4.5 volt power supply. The power source provides approximately 7.9 volts unregulated dc. Of this, 3.4 volts is dropped across the +4.5 volt regulator, leaving regulated +4.5 volts across Ra, the computer circuits which use this voltage.

3-113. The -2 volt source and the -2 volt regulator make up the -2 volt power supply. The power source provides approximately 10.1 volts unregulated dc. Of this, 3.6 volts is dropped across the regulator. The resulting 6.5 volts is applied across Rb, which represents the load imposed by the CTL logic circuits in the card cage. Although it furnishes 6.5 volts, the output of the regulator is at a potential of -2 volts with respect to ground; therefore the regulator and its power source are referred to as the -2 volt regulator and -2 volt power source. As well as being applied to Rb, the output of the -2 volt regulator is furnished to Rc, which represents the pull-down resistors in the card cage. In some cases these resistors are discrete components and in other instances they form part of integrated circuits in micropacks. Also to be considered as part of Rc are paths from -2 volts to ground within the power supply section itself. These paths to ground in the power supply result in a current of 0.5 to 0.75 amp.

3-114. The -2 volt power supply can furnish up to 22.5 amps. The +4.5 volt supply furnishes 22.5 amps, plus the current drawn from the -2 volt supply. (In figure 3-8, note that the current through Rc also flows through Ra.) When optional circuit cards are installed, these current limitations

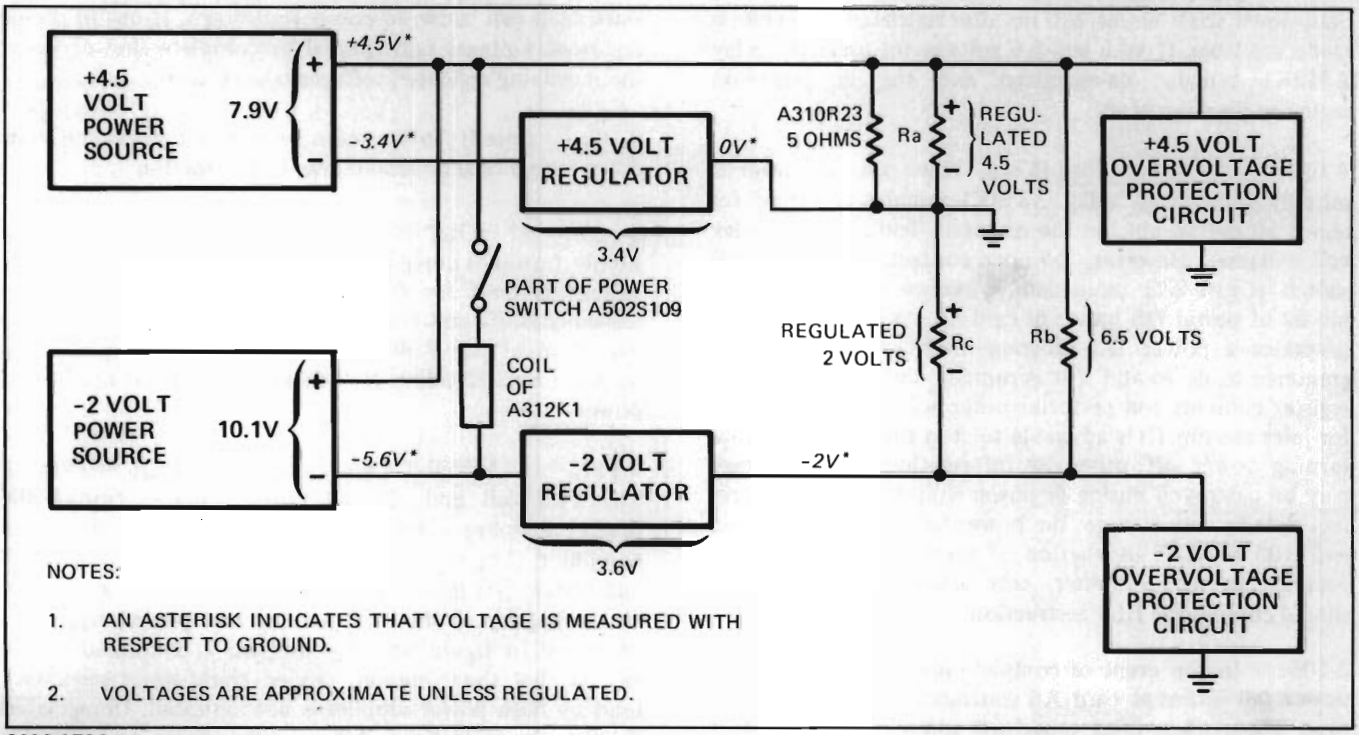


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Figure 3-8. +4.5 Volt and -2 Volt Power Supplies, Block Diagram

must be taken into consideration. If an attempt is made to draw excessive current from the +4.5 volt or -2 volt power supply, dc shut-down takes place. The +4.5 volt regulator is between the power source and ground, rather than in the more usual position between the power source and the high potential end of the load. The reason for this is that the top end of Ra and Rb are connected together inside integrated circuits, and if the +4.5 volt regulator were in the common return of Ra and Rb to the power sources, the +4.5 volt regulator would not be able to control the +4.5 volt output without affecting the output of the -2 volt regulator. Another reacting element between the two power supplies is the common current which flows through Rc and Ra. Both Rc and Ra may include circuits on optional cards. If Rc becomes sufficiently small in resistance because of added cards, the current through Rc will exceed the normal current through Ra. Current then ceases to flow through the +4.5 volt regulator, and excessive current flows through Ra. As a result, the voltage across Ra rises above 4.5 volts and shut-down takes place. To prevent difficulty from this effect, resistor A310R23 is installed in the power supply. This resistor draws current from the +4.5 volt power supply in addition to that drawn by Ra, and as a result the current through Rc will not exceed that normally flowing through Ra and A310R23.

3-115. Included in figure 3-8 is the coil of A312K1. Although one end of this coil is connected to +4.5 volts, the voltage across the coil is 10.1 volts, the output of the -2 volt power source.

3-116. The overvoltage protection circuits for the +4.5 and -2 volt power supplies prevent damage to components due to excessively high output voltage from the power supply. If, because of a fault in the voltage regulator, the power supply output voltage rises, the overvoltage protection circuit permits short-circuit current to flow. The increased current from the power supply causes current limiting, protecting the power supply from damage. When the short is imposed across the computer load, the voltage across the load drops to zero, and this loss of voltage initiates dc power shut-down.

3-117. +12, -12, +20, AND -20 VOLT POWER SUPPLIES. The +12, -12, +20, and -20 volt power supplies furnish regulated voltages to the following circuit cards:

a. +12 volts is supplied to:

(1) Power fail interrupt card A6.
(2) Sense amplifier cards A9, A10, A19, and A20.
(3) I/O address card A202.
(4) I/O interface cards A203 through A218.
(5) I/O-1 extender driver card A219.
(6) I/O-2 extender driver card A220.

b. -12 volts is supplied to:

(1) Power fail interrupt card A6.
(2) Sense amplifier cards A9, A10, A19, and A20.
(3) I/O control card A201.
(4) I/O interface cards A203 through A218.
(5) I/O-1 extender driver card A219.
(6) I/O-2 extender driver card A220.

c. +20 volts is supplied to:

(1) Power-failure auto-restart card A6.
(2) Inhibit driver cards A7, A12, A17, and A22.
(3) X-Y driver/switch cards A8, A11, A18, and A21.

d. -20 volts is supplied to:

(1) Power-failure auto-restart card A6.
(2) X-Y driver/switch cards A8, A11, A18, and A21.

3-118. Figure 3-9 is a block diagram portraying each of the power supplies, +12, -12, +20, or -20 volts. The +20 and -20 volt outputs vary in accordance with the air temperature in the computer cabinet. This change in voltage counteracts the changes in core stack operation resulting from temperature change.

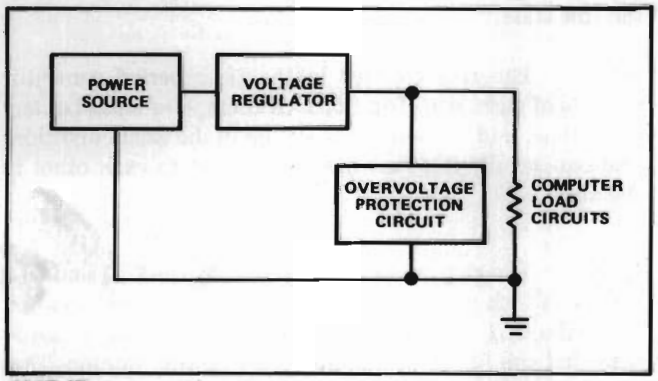

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Figure 3-9. +12, -12, +20, or -20 Volt Power Supply, Block Diagram

3-119. +35 VOLT POWER SUPPLY. The +35 volt power supply furnishes filtered, unregulated dc to circuit cards A203 through A218. This voltage is also furnished to I/O-1 extender driver card A219, and to I/O-2 extender driver card A220.

3-120. +32 VOLT POWER SUPPLY. The +32 volt power supply furnishes regulated +32 volts to power fail interrupt card A6 for use when the auto-restart option is installed. The voltage is also furnished to logic supply regulator card A301.

3-121. DETAILED THEORY, CONTROL SECTION.

3-122. TIMING CIRCUITS.

3-123. BASIC TIMING CIRCUITS. It has been explained that the basic timing circuits produce 200-ns clock pulses, 400-ns double-length clock pulses, and 45- to 50-ns strobe pulses. The trailing edge of each strobe pulse coincides with the trailing edge of each pulse.

3-124. The basic timing circuits make up part of timing generator card A106. They consist of an oscillator, a frequency divider, time-strobe generator circuits, and a time period generator. These are illustrated in block diagram form in figure 3-10, and described in the following paragraphs.

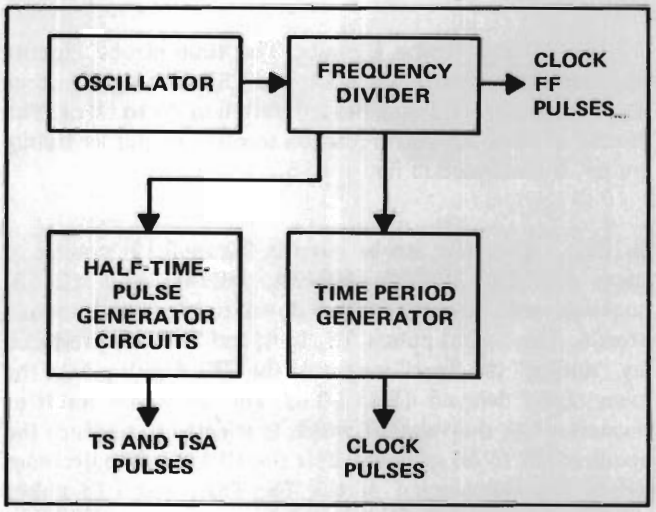

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Figure 3-10. Basic Timing Circuits, Block Diagram

3-125. Oscillator. The oscillator utilizes a crystal-controlled Colpitts circuit, followed by an amplifier stage and a buffer stage (figure 3-11). The Colpitts oscillator, consisting of transistor Q1 and its associated components, is the fundamental timing element within the computer. The output of the oscillator is amplified by transistor Q2, buffered by Q3, and furnished to the frequency divider. The output waveform of Q3 is illustrated in figure 4-16. For test purposes, this waveform is available at pin 3 of card A106.

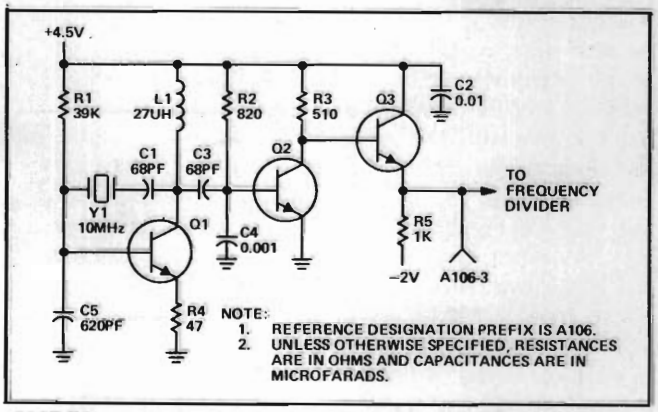

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Figure 3-11. Oscillator, Schematic Diagram

3-126. Frequency Divider. The frequency divider (figure 3-12) consists of flip-flops CF1 and CF2, and gates MC62A and MC62B. The J and K inputs to each of the flip-flops are connected to +4.5 volts. The flip-flops therefore function as divide-by-two counters, each triggered by a negative-going input to pin 1. The CF1 flip-flop receives the output of the 10-MHz oscillator circuit, and furnishes a square wave with

a period of 200 ns. The CF2 flip-flop receives this signal, and provides a square wave with a period of 400 ns. (See figure 4-15.)

3-127. Gates MC62A and MC62B combine the outputs of the CF1 and CF2 flip-flops to produce the CL1 and CL2 signals. (See figure 4-15.)

3-128. Time Strobe Circuits. The time strobe circuits produce three signals, TS, TSA, and TSB. The signals occur simultaneously, and each has a duration of 45 to 50 ns. The timing of these signals, in relation to other computer timing pulses, is illustrated in figure 4-15.

3-129. The time strobe circuits (figure 3-12) consist of gates MC52A, MC52B, MC42A, MC75B, and MC16B, together with associated pull-down resistors and capacitor C6. The output pulses, TS, TSA, and TSB, are produced by "anding" the "not" output of the CF1 flip-flop with the same signal delayed 45 to 50 ns. The delay is a result of capacitor C6, the value of which is selected to produce the required 45 to 50 ns delay after the CF1 flip-flop becomes reset. The termination of the TS, TSA, and TSB pulses occurs when the CF1 flip-flop is set.

3-130. Gates MC42A, MC75B, and MC16B perform corresponding functions for the TS signal, the TSA signal, and the TSB signal, respectively.

3-131. If a component in the discharge path of C6 is changed, it may also be necessary to change the capacitor itself in order to retain the required 45 to 50-ns duration of the time strobe pulses. (Components in the discharge path are MC52A, MC52B, and MC52R2.) The value of C6 typically ranges from 100 to 180 pf.

3-132. Time Period Generator. The time period generator consists of a ring counter and associated "and" gates (figure 3-13). This unit produces the eight clock pulses T0 though T7, each lasting 200 ns. The time period generator also produces double-length pulses, each true for the duration of two clock pulses. One more pulse produced is the T7S pulse, which is true during the last quarter of T7. The various outputs of the time period generator are included in figure 4-15.

3-133. The T6 pulse is used only by cards A109 and A110, which comprise the optional Extended Arithmetic Unit. Integrated circuits on these two cards contain TTL gates which receive the T6 pulse and furnish resistive paths to -2 volts. These paths function as pull-down resistors, required for development of the T6 pulse. If the A109 and A110 cards are not installed, the absence of pull-down resistors results in the T6 output remaining permanently in the true state.

3-134. The ring counter in the time period generator consists of eight latch flip-flops. Of these, two are set at any given time, and the remaining six are in the clear condition. The two set flip-flops are always adjacent to each other in the ring.

3-135. The ring counter is operated by the CL1 and CL2 signals, which trigger alternate flip-flops in the counter. From the CL1 and CL2 waveforms in figure 4-15, it can be seen that the flip-flops operate in a leap-frog fashion. That is, the positive-going edge of each CL1 and CL2 pulse clears

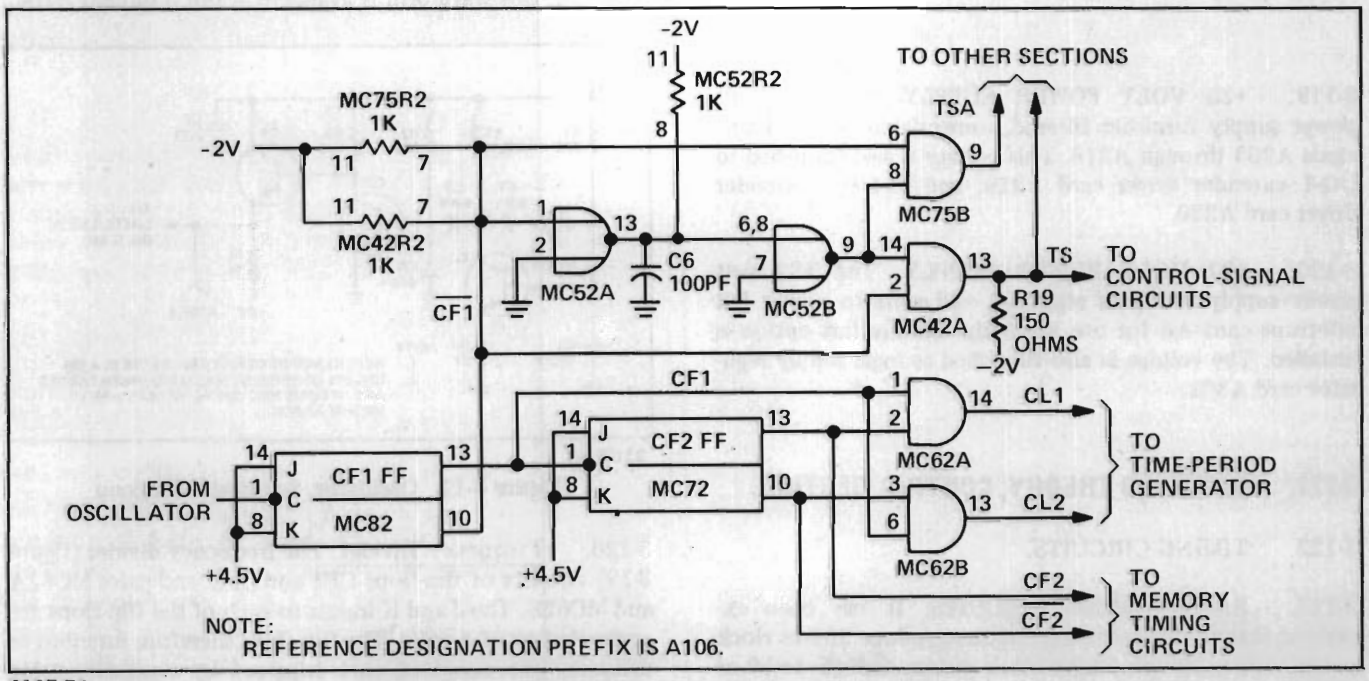

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Figure 3-12. Frequency Divider and Time Strobe Circuits, Logic Diagram

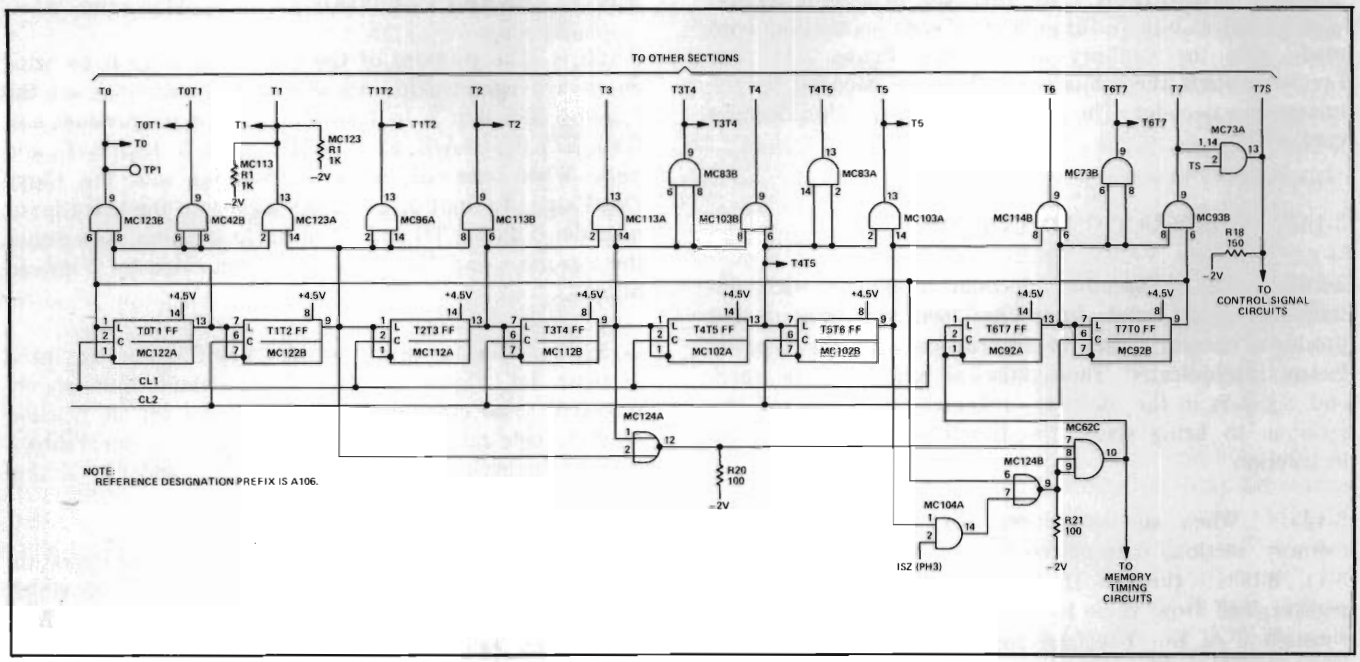

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Figure 3-13. Time Period Generator, Logic Diagram

the trailing flip-flop of the two that are set, and sets the flip-flop immediately ahead of the second flip-flop.

3-136. When power is applied to the computer, the flip-flops in the ring counter assume a random state. Within one machine cycle (four CL1 pulses and four CL2 pulses), the ring counter is in the required condition, with two adjacent flip-flops set and the remaining flip-flops clear. At this time the clock pulse furnished is T6, and for this reason the clock pulses in figure 4-15 begin with T6. The circuits which bring about the initial condition are the following A106 gates: MC124A, MC124B, and MC62C. Gate MC104A is enabled only during an ISZ instruction; operation of this gate is dealt with in the explanation of the ISZ instruction in section IV.

3-137. MEMORY TIMING CIRCUITS. The memory timing circuits, on timing generator card A106, provide pulse signals for controlling the transfer of data to and from the memory section. The signals are generated from clock pulses, pulses received from the instruction decoder, and front panel controls. Through the use of gates, the memory timing circuits produce from these inputs the required pulses for controlling writing and reading in the core stacks. Detailed discussion of the memory timing circuits is reserved for the troubleshooting information in section IV (paragraph 4-156). However, before referring to this part of the manual, the reader must be familiar with the theory of the memory section presented later in section III.

3-138. One point which must be noted is that the MWL pulse, produced by the memory timing circuits, remains permanently true if neither of the following cards is installed: card A15 (Parity Error Option) and card A16 (Memory Protect Option). As with the T6 pulse, pulldown resistors on the optional cards are required for generation of the MWL pulse.

3-139. CONTROL SECTION REGISTERS.

3-140. The registers in the control section are the transfer register (T-register), memory address register (M-register), program address register (P-register), and instruction register (I-register). The following paragraphs explain in general terms the function of each of these registers. A detailed analysis is not provided since the circuits are simple flip-flop registers of conventional design. No carry circuits are used; the arithmetic gates provide this facility when required.

3-141. T-REGISTER. The T-register receives 16-bit words which will be stored in, or which have been read from, the memory section (see figure 3-1). The various stages of the T-register are on four arithmetic logic cards, with reference designations A102, A103, A104, and A105.

3-142. M-REGISTER. The M-register specifies the core memory address in which a word will be stored, or from which a word will be retrieved (see figure 3-1). The various stages of the M-register are on arithmetic logic cards A102, A103, A104, and A105.

3-143. P-REGISTER. The P-register specifies the core memory address from which the next instruction word will be read (see figure 3-1). When the P-register contents are used, they are gated onto the R bus, passed through the arithmetic gates, and gated into the M-register. From here, the address is forwarded to the memory section. The various stages of the P-register are on arithmetic logic cards A102, A103, A104, and A105.

3-144. I-REGISTER. The I-register is a 6-bit register which receives bits 15 through 10 of each instruction word read from the memory section (see figure 3-1). The I-register holds these bits while they are decoded by the instruction decoder. The register is on instruction decoder card A107.

3-145. INSTRUCTION DECODER.

3-146. The instruction decoder examines each instruction word read from the memory section, and produces control pulses in accordance with the type of instruction indicated. These pulses activate flip-flops, gates and registers in the memory, arithmetic, control, and I/O sections to bring about the functions required by the instruction.

3-147. When an instruction word is read from the memory section, it is placed in the T-register (see figure 3-1). Bits 15 through 10 are forwarded to the 6-bit I-register, and from there to the instruction decoder. Bits 9 through 0 of the T-register are furnished directly to the instruction decoder.

3-148. During the course of most instructions, the instruction decoder brings about performance of the following operations (refer to figure 3-1):

a. Gates the contents of the T-, P-, M-, A-, or B-register onto the R bus or S bus.

b. Activates the arithmetic gates to bring about changes in R bus or S bus data as it passes through the gates.

c. Loads the T-, P-, M-, A-, or B-register from the T bus.

3-149. Further information on the operations brought about by the instruction decoder is presented in section IV, where explanatory test and a troubleshooting diagram are provided for each computer instruction.

3-150. The instruction decoder is on instruction decoder card A107.

3-151. PHASE GENERATOR.

3-152. Details on operation of the phase generator are provided in paragraph 4-164.

3-153. SWITCHES AND INDICATORS.

3-154. Details on the functioning of switches and indicators are provided in paragraph 4-65.

3-155. RUN AND HALT CIRCUITS.

3-156. Information on the functioning of the run and halt circuits is furnished in paragraphs 4-71 and 4-76.

3-157. CARRY FLIP-FLOP.

3-158. The purpose of the Carry Flip-Flop is to bring about a program skip. All skip-type instructions set the flip-flop if a skip is to take place. These instructions are: RSS, SZA/B, SSA/B, SLA/B, SEZ, CPA/B, ISZ, SFC, and SFS. When one of these instructions sets the Carry Flip-Flop, the flip-flop furnishes logic 1 to the carry input of adder 0 during T6 and T7 of the instruction. As a result, the P-register and M-register are incremented by 2 instead of by 1.

3-159. The gates which set the Carry Flip-Flop are listed in table 3-3. Figure 3-14 shows the circuits immediately involved; these circuits and the flip-flop itself are situated on shift logic card A108. The C0 (Carry Bit 0) signal shown in the illustration is the carry input to adder 0. A skip occurs when C0 is true.

3-160. The following paragraphs describe the operation of the Carry Flip-Flop for each of the instructions which affect the flip-flop. For further information on these instructions, refer to the troubleshooting information for the instruction concerned. The location of this troubleshooting information is given in table 4-6.

3-161. RSS INSTRUCTION. When not combined with other alter-skip instructions, the RSS instruction causes an unconditional skip. When the instruction is performed, gate MC24A provides a true output during T5. All inputs to gate MC54C are then true. When the TS clock-pulse applied to the Carry Flip-Flop becomes true, the input rank of the flip-flop is set; the output rank is set when the TS pulse falls at the end of T5. During T6T7 the C0 signal is true, and a program skip takes place. The Carry Flip-Flop is cleared at the end of the following T0.

3-162. The eight gates shown below MC24A are employed by the instructions for which RSS can reverse the skip sense. These instructions are all in the alter-skip group, and they are SZA/B, SSA/B, SLA/B, and SEZ. The bottom four gates in the group of eight are used for normal skip sense. For reverse skip sense, all eight gates are used.

3-163. SZA/B, SSA/B, SLA/B, AND SEZ INSTRUCTIONS. If reverse skip sense is not used, gates MC25C, MC15C, MC96C, and MC77C determine the existence of a skip condition for the seven conditional skip instructions in the alter-skip group. These gates function as follows:

a. Gate MC25C, used by the SZA/B instructions, furnishes a true output during T5 if the A- or B-register contains 16 zeroes. The TR1 input to this gate, together with the ASG input to gate MC54B, identifies the SZA/B instruction. (See figure 4-1 for instruction formats.) The output from gate MC87B, if true, indicates the existence of 16 zeroes on the 16 T bus lines, onto which the contents of the A- or B-register are gated.

b. Gate MC15C, used by the SSA/B instructions, furnishes a true output during T4 if R bus 15 carries logic

Table 3-3. Operation of Carry Flip-Flop

SKIP INSTRUCTION	ACTIVE GATES	
	WITHOUT RSS	WITH RSS
Alter-Skip Instructions		
RSS (Reverse Skip Sense), not combined with other instructions.	— — — — — — —	MC124B MC124A MC14A MC24A* MC94A MC54C MC54B
SZA/B (Skip if Zero in A- or B-Register)	MC87B MC113B MC25C* MC127B MC54B	MC113B MC25A* MC94A MC54C MC54B
SSA/B (Skip if Sign Bit of A- or B-Register is Zero)	MC124A MC15C* MC127B MC54B	MC124A MC25B* MC94A MC54C MC54B
SLA/B (Skip if Least Significant Bit of A- or B-Register is Zero)	MC74A MC96C* MC127B MC54B	MC74A MC15A* MC94A MC54C MC54B
SEZ (Skip if E-Register Contains Zero)	MC124B MC77C* MC127B MC54B	MC124B MC15B* MC94A MC54C MC54B
Memory Reference Instructions		
CPA/B (Compare [M] with the Contents of the A- or B-Register; Skip if Unequal)	MC87B MC14B MC86B*	— — —
ISZ (Increment [M]; Skip if Zero)	MC86A*	—
Input/Output Instructions		
SFC (Skip if Flag Clear)	MC84A*	—
SFS (Skip if Flag Set)	MC84A*	—
Shift-Rotate Instructions		
SLA/B (Skip if Least Significant Bit of A- or B-Register is Zero)	MC87A*	—

NOTES:

*An asterisk identifies the principal gate for the instruction.

0. At that time, R bus 15 indicates the content of A- or B-register position 15.

c. Gate MC96C, used by the SLA/B instructions, furnishes a true output at T4 if bit position 0 of the A- or B-register contains logic 0.

d. Gate MC77C, used by the SEZ instruction, furnishes a true output during T3 if the Extend Flip-Flop is clear.

3-164. When reverse skip sense is not combined with SZA/B, SSA/B, SLA/B, or SEZ, bit 0 of the T-register contains logic 0. When one of the instructions is performed, gate MC127B furnishes a true output when MC25C, MC15C, MC96C, or MC77C experiences coincidence. The Carry Flip-Flop is set at the end of T3, T4, or T5, depending on the gate that detected the skip condition. If a skip condition is not detected, the Carry Flip-Flop remains in the clear condition in which it is placed at the end of each T0, and no skip takes place.

3-165. If reverse skip sense is programmed with an SZA/B, SSA/B, SLA/B, or SEZ instruction, position 0 of the T-register contains logic 1. Consequently, gate MC127B is disabled, and MC54C is enabled. If gate MC25C, MC15C, MC96C, or MC77C does not experience coincidence, the output of MC74B is true during the entire machine cycle. Gate MC25A, MC25B, MC15A, or MC15B furnishes a T3, T4, or T5 pulse, depending on the type of skip instruction.

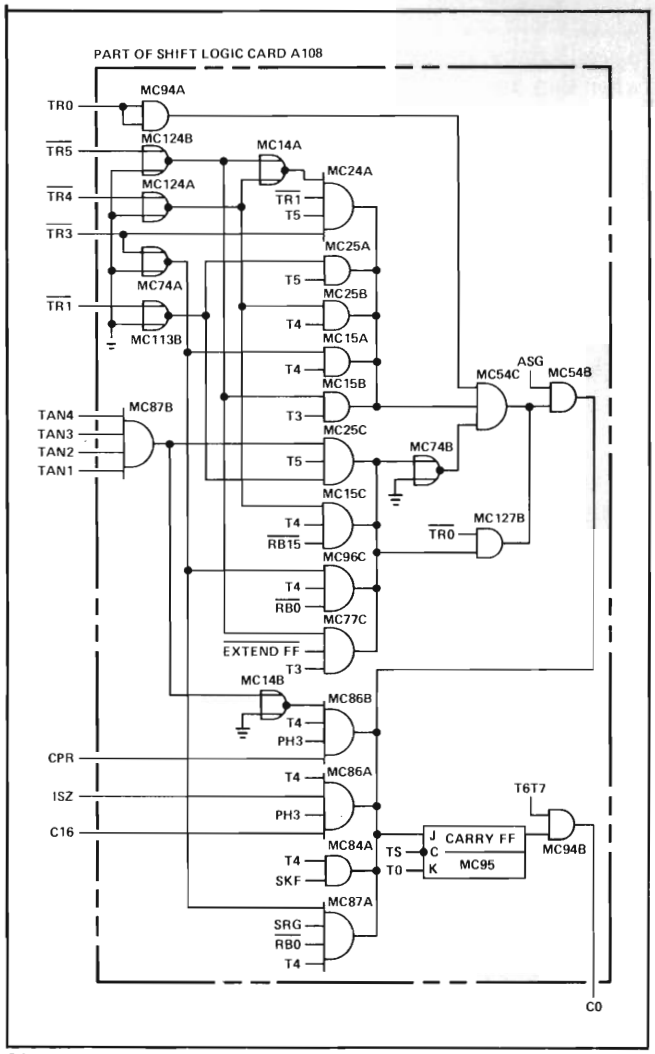

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Figure 3-14. Carry Flip-Flop Circuits

The Carry Flip-Flop is then set and a skip occurs. However, if gate MC25C, MC15C, MC96C, or MC77C experiences coincidence, MC54C is disabled by MC74B, and the Carry Flip-Flop is not set.

3-166. When alter-skip instructions are combined, operation is the same as with separate instructions. If any skip condition is met, the Carry Flip-Flop is set and a skip takes place. As an exception, when SSA/B, SLA/B, and RSS are combined, the sign and the least-significant-bit of the A- or B-register must both be logic 1 for a skip to occur. This results from the fact that MC15C (for SSA/B) and MC96C (for SLA/B) must both furnish a false output to allow MC74B to provide an enable to MC54C. Gates MC25C (for SZA/B) and MC77C (for SEZ) furnish their outputs at T5 and T3 respectively; they thus operate independently of each other and independently of the gates for SSA/B and SLA/B.

3-167. In addition to being in the alter-skip group, the SLA/B instructions can be programmed as shift-rotate instructions if an alternative instruction-word format is used. This feature permits the instructions to be combined either with alter-skip instructions or shift-rotate instructions. When programmed as a shift-rotate instruction, SLA/B brings about coincidence in gate MC87A if a skip is to take place. Reverse skip sense cannot be employed with SLA/B when they are coded as shift-rotate instructions.

3-168. CPA/B INSTRUCTIONS. CPA/B are memory reference instructions which compare the contents of the specified memory location with the A- or B-register. If the 16-bit numbers are unequal, a program skip takes place.

3-169. Gate MC86B furnishes a true output during T4 of phase 3 if a skip is to take place. The output of gate MC87B, inverted by MC14B, is an enable for MC86B when the skip condition exists.

3-170. ISZ INSTRUCTION. ISZ is a memory reference instruction which increments by 1 the contents of the specified memory location. If this operation advances the contents of the memory location to zero, a program skip takes place.

3-171. Gate MC86A furnishes a true output during T4 of phase 3 if a skip is to take place. The C16 (Carry Bit 16) input to the gate is true if the contents of the memory location advance to zero.

3-172. SFC AND SFS INSTRUCTIONS. SFC and SFS are input/output instructions which check the status of the Flag Flip-Flop on the interface card indicated by the select code of the instruction. If the select code is 00 (octal), the Interrupt System Enable Flip-Flop on card A201 is checked. A program skip takes place if the addressed flip-flop is clear (in the case of SFC) or if it is set (for SFS).

3-173. Gate MC84A monitors the SKF signal, which becomes true if a skip condition exists.

3-174. EXTEND FLIP-FLOP

3-175. The Extend Flip-Flop, also known as the E-register, is employed for a number of purposes. The Extend Flip-Flop operates in conjunction with the A- or B-register in rotate operations brought about by the ELA/B instructions. When an ELA/B instruction is performed, the entire contents of the A- or B-register are shifted one position to the left, and the bit originally in the Extend Flip-Flop is moved into position 0 of the accumulator register. The bit in position 15 of the A- or B-register is rotated into the Extend Flip-Flop, where it can be checked by the SEZ instruction. The ERA/B instructions perform similar operations, except that rotation is to the right; position 0 of the accumulator is shifted into the Extend Flip-Flop, and the bit originally in the Extend Flip-Flop is shifted into position 15 of the accumulator.

3-176. The Extend Flip-Flop is also used to move a bit between the A- and B-registers. To accomplish this, the bit is rotated into the Extend Flip-Flop by an ELA/B or ERA/B instruction; then another rotate instruction shifts the bit into the other accumulator.

3-177. An additional function of the Extend Flip-Flop is to record the occurrence of a carry from position 15 of the A- or B-register when an ADA/B or INA/B instruction is performed. The flip-flop is not affeeted by subsequent carriers until it has been cleared. The program determines the occurrence of the carry by an SEZ instruction. Before the ADA/B or INA/B instruction is performed, the Extend Flip-Flop must be cleared by a CLE instruction. The ISZ instruction does not affect this flip-flop.

3-178. The Extend Flip-Flop is further used as a 1-bit storage cell. The contents of the cell can be changed by any of the methods described above, using the ELA/B, ERA/B, ADA/B, INA/B, or CLE instructions. The contents can also be changed by the CCE or CME instructions. The SEZ instruction is used to determine the contents of the cell.

3-179. The state of the Extend Flip-Flop is shown by the EXTEND indicator, situated on display board A501. The indicator lights when the flip-flop is set.

3-180. The paragraphs which follow describe the operation of the Extend Flip-Flop for each of the instructions which affect it. Figure 3-15 shows the flip-flop and associated gates, while table 3-4 lists the gates used by each instruction. For further information on these instructions, refer to the troubleshooting information for the instruction concerned. The location of this troubleshooting information is given in table 4-6.

3-181. ELA/B INSTRUCTIONS. The ELA/B instructions rotate the contents of the Extend Flip-Flop left one position with the contents of the A- or B-register. The bit in position 15 of the A- or B-register is moved into the Extend Flip-Flop, and the bit in the Extend Flip-Flop is moved into position 0 of the A- or B-register.

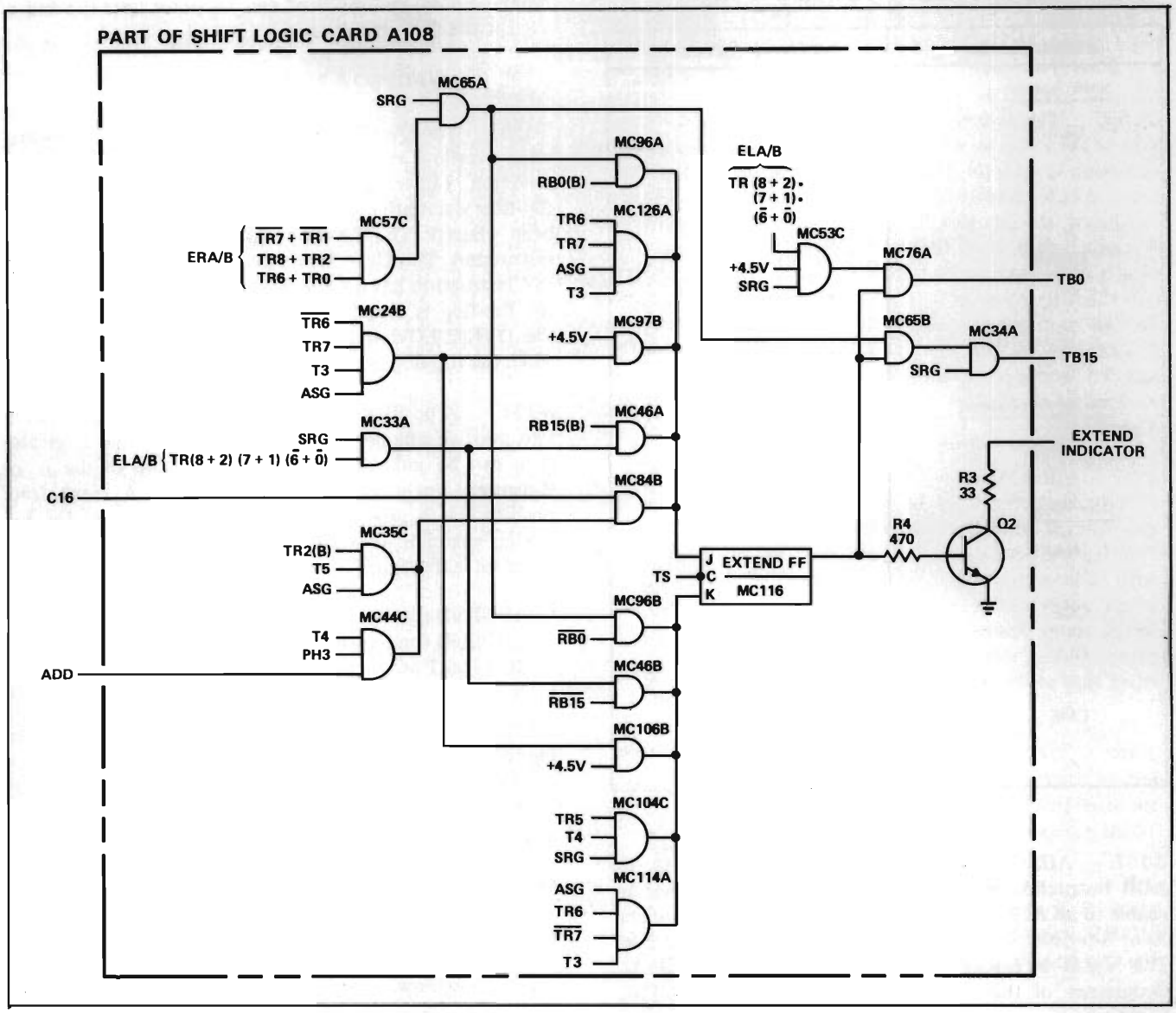

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Figure 3-15. Extend Flip-Flop Circuits

3-182. Gate MC33A provides an enable for gates MC46A and MC46B. The bit in position 15 of the A- or B-register is gated onto R bus, and MC46A or MC46B sets or clears the Extend Flip-Flop when the flip-flop receives a clock pulse.

3-183. One input to MC33A is the SRG (Shift Rotate Group) signal, which becomes true when a shift-rotate instruction is decoded. The other input to MC33A is TR (8+2) (7+1) ($\bar{6}$+$\bar{0}$). This signal is true when T-register positions 8 and 7 contain logic 1, and position 6 contains logic 0. The signal is also true when T-register positions 2 and 1 contain logic 1, and position 0 contains logic 0. Figure 4-1 shows that the T-register contains the first set of bits when an ELA/B instruction is indicated by bits 8, 7, and 6 of the instruction word. The T-register contains the second set of bits when an ELA/B instruction is indicated by bits 2, 1, and 0 of the instruction word.

3-184. Gates MC53C and MC76A shift the bit originally in the Extend Flip-Flop onto T bus 0, from where the bit is gated into position 0 of the A- or B-register.

3-185. The SRG signal, which enables the principal gates used by the ELA/B instructions, becomes true at the beginning of T3. During T3TS, the STBA (Store T Bus in A-register) or STBB (Store T Bus in B-Register) signal is true (figure 7-14). The bit in the Extend Flip-Flop, gated onto T bus 0, is then placed in position 0 of the A- or B-register. Furthermore, at the start of T3TS, the bit on R bus 15 is placed in the input rank of the Extend Flip-Flop; at the end of T3TS, the bit is transferred to the output rank of the flip-flop, and determines the final contents of the Extend Flip-Flop.

3-186. ERA/B INSTRUCTIONS. The ERA/B instructions are similar to the ELA/B instructions, and require no further discussion. Table 3-4 lists the gates used.

Table 3-4. Operation of Extend Flip-Flop

INSTRUCTION	ACTIVE GATES
Shift-Rotate	
ELA/B	MC33A MC46A MC46B MC53C MC76A
ERA/B	MC57C MC65A MC96A MC96B MC65B MC34A
Memory Reference	
ADA/B	MC44C MC84B
Alter-Skip	
INA/B	MC35C MC84B
CCE	MC126A
CLE	MC104C MC114A
CME	MC24B MC97B MC106B

3-187. ADA/B INSTRUCTIONS. When the ADA or ADB instruction is performed, gate MC44C furnishes an enable to MC84B. If there is a carry from position 15 of the A- or B-register, the C16 (Carry Bit 16) signal becomes true. This signal is furnished by arithmetic logic card A102. Occurrence of the carry results in the Extend Flip-Flop being set.

3-188. INA/B INSTRUCTIONS. The INA/B instructions are similar to the ADA/B instructions insofar as the Extend Flip-Flop is concerned. Table 3-4 lists the gates used.

3-189. CCE INSTRUCTION. The CCE instruction sets the Extend Flip-Flop by means of gate MC126A. If the flip-flop is already set, it remains set.

3-190. CLE INSTRUCTION. The CLE instruction can be coded either as a shift-rotate instruction or as an alter-skip instruction, allowing it to be combined with instructions in either group (see figure 4-1). As a shift-rotate instruction, CLE clears the Extend Flip-Flop by means of gate MC104C. When the instruction is coded as an alter-skip instruction, gate MC114A accomplishes the same purpose.

3-191. CME INSTRUCTION. When the CME instruction is performed, gate MC24B provides an input to gates MC97B and MC106B during T3. Both the set and the clear inputs to the Extend Flip-Flop therefore receive true inputs. Upon occurrence of the TS pulse near the end of T3, the flip-flop changes state.

3-192. OVERFLOW FLIP-FLOP.

3-193. The Overflow Flip-Flop records a positive or negative overflow occurring during an ADA/B or INA/B instruction. Either type of overflow sets the flip-flop. The flip-flop is not affected by subsequent overflows until it has been cleared. The flip-flop can also be set by an STO instruction. The CLO instruction clears the flip-flop. The ISZ instruction has no affect on the flip-flop. The state of the flip-flop is tested by an SOS or SOC instruction, and the OVERFLOW indicator on display board A501 lights when the flip-flop is set.

3-194. A positive overflow indicates that the addition of two positive numbers has produced a sum that is greater than can be indicated by the 15 positions of the A- or B-register (excluding the sign position). A carry from position 14 to position 15 indicates an overflow. The following example illustrates a positive overflow (the high-order bit is the sign bit):

AUGEND (on R bus)	0 000 100 000 000 000
ADDEND (on S bus)	0 111 111 111 111 111
SUM (on T bus)	1 000 011 111 111 111

3-195. The high-order bit of the sum is logic 1, appearing to indicate a negative number. In actuality the result is positive, and its magnitude is too large to be indicated by 15 bits.

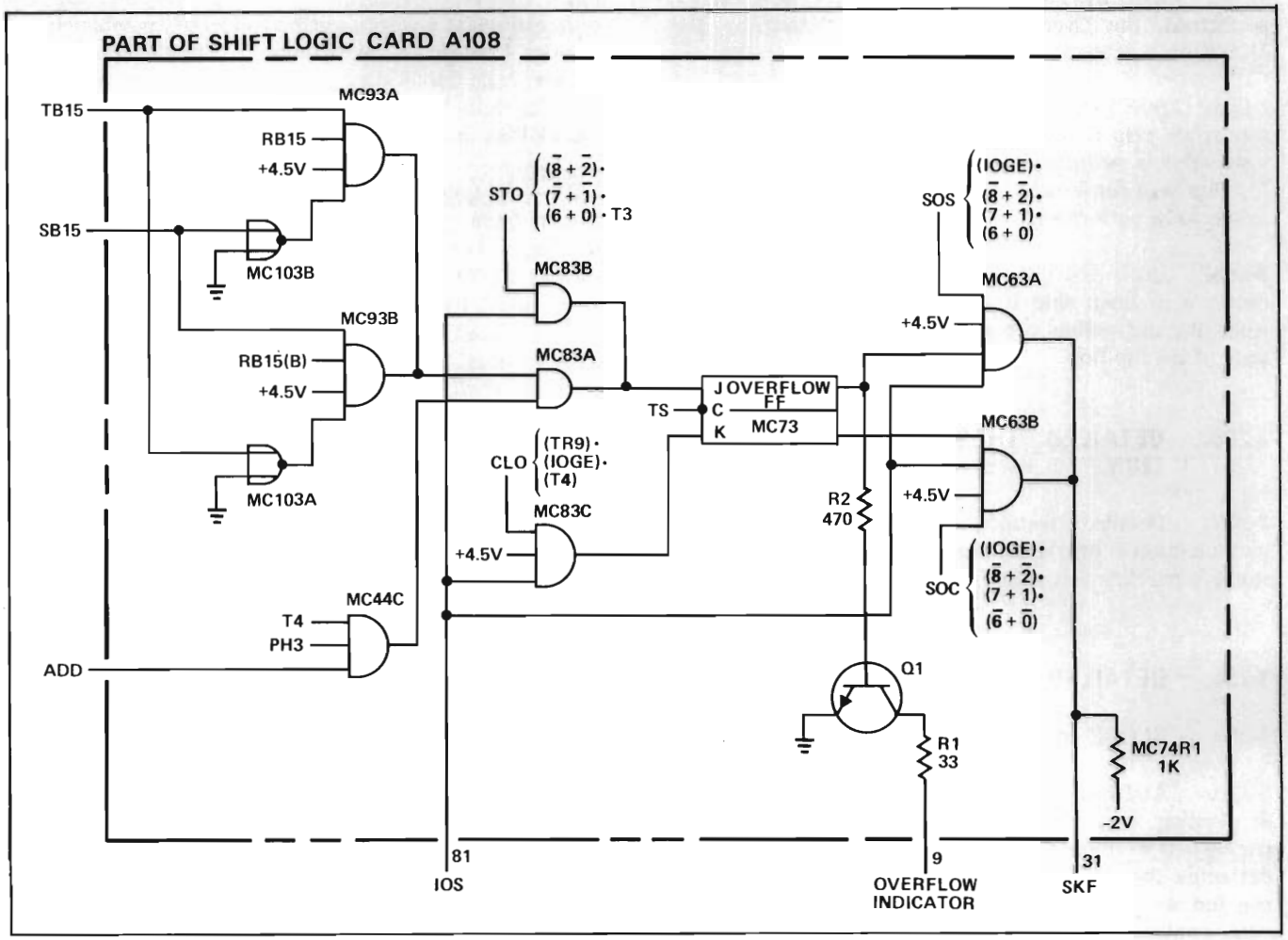
3-196. A negative overflow indicates that the addition of two negative numbers has resulted in a negative number with a magnitude to great to be contained in a 16-bit register. The lack of a carry from position 14 to position 15 indicates an overflow. The following example illustrates a negative overflow:

AUGEND (on R bus)	1 000 000 000 000 001
ADDEND (on S bus)	1 000 000 000 000 001
SUM (on T bus)	0 000 000 000 000 010

3-197. The high-order bit of the sum is logic 0, appearing to indicate a positive number. In actuality, the result is negative, and its magnitude is too great to be indicated by 15 bits.

3-198. The following paragraphs desribe the operation of the Overflow Flip-Flop for each of the instructions which affect it. Figure 3-16 shows the flip-flop and associated gates, while table 3-5 lists the gates used by each instruction. For further information on the instructions, refer to the troubleshooting information for the instruction concerned. The location of this troubleshooting information is given in table 4-6.

3-199. ADA/B INSTRUCTIONS. Gate MC93A is the positive overflow enabling gate. When R bus 15 and S bus 15 are both logic 0 (indicating positive numbers), and



2107-155

Figure 3-16. Overflow Flip-Flop Circuits

Table 3-5. Operation of Overflow Flip-Flop

INSTRUCTION	ACTIVE GATES
ADA/B	MC44C MC83A MC93A MC103B MC93B MC103A
CLO	MC83C
INA/B	MC35C MC83A MC93A MC103B MC93B MC103A
SOC	MC63A
SOS	MC63B
STO	MC83B

when T bus 15 is logic 1 and an add operation has just been performed, positive overflow has occurred. When this is the case, the Overflow Flip-Flop is set.

3-200. Gate MC93B detects negative overflows. When R bus 15 and S bus 15 are both logic 1 (indicating negative numbers), and when T bus 15 is logic 0 and an add operation has been performed, negative overflow has occurred.

3-201. INA/B INSTRUCTIONS. Operation of the Overflow Flip-Flop during the INA/B instructions is similar to operation for the ADA/B instructions, and further discussion is not required.

3-202. STO INSTRUCTION. When an STO instruction is performed, gate MC83B sets the Overflow Flip-Flop. As figure 4-1 shows, when this instruction word is in the T-register, bits 8 and 7 of the T-register are logic 0 and bit 6 is logic 1. This condition results in one true input to MC83B. The other input to MC83B is the IOS (Input/Output Switch Address) signal. Although the STO instruction does not involve the S-register, this signal becomes true during an STO instruction, and the Overflow Flip-Flop is set.

3-203. CLO INSTRUCTION. When a CLO instruction is performed, the Overflow Flip-Flop is cleared by gate MC83C.

3-204. SOS INSTRUCTION. The SOS instruction causes a program skip if the Overflow Flip-Flop is set when the instruction is performed. Gate MC63A tests the state of the flip-flop, and furnishes a true SKF (Skip on Flag) signal if a skip is to be performed.

3-205. SOC INSTRUCTION. The SOC instruction causes a program skip if the Overflow Flip-Flop is clear when the instruction is performed. Gate MC63B tests the state of the flip-flop.

3-206. DETAILED THEORY, ARITHMETIC SECTION.

3-207. Detailed treatment of operations in the arithmetic section is provided in section IV, where each instruction is separately delt with.

3-208. DETAILED THEORY, MEMORY SECTION.

3-209. BLOCK DIAGRAM ANALYSIS.

3-210. ADDRESS SELECTION. When memory reading or writing is performed, the address decoding gates (figure 3-1) examine bits 11 through 0 of the M-register to determine the word-location to be referenced. These 12 bits can indicate any octal address from 0000 through 7777, corresponding to the 4,096 locations in the lower or upper module of a core stack assembly.

3-211. Bits 11 through 6 of the M-register indicate the Y drive-line to be used (see figure 3-17). These bits are decoded to yield their octal equivalent, in the form of two octal digits. Bits 11, 10, and 9 give the most-significant-digit (MSD), and bits 8, 7, and 6 give the least-significant-digit (LSD). Together, these two digits identify one of the 64 Y drive-lines in the core stack assembly.

3-212. Bits 5 through 0 of the M-register are decoded in a manner similar to that used for bits 11 through 6, to yield a 2-digit octal number identifying the X drive-line.

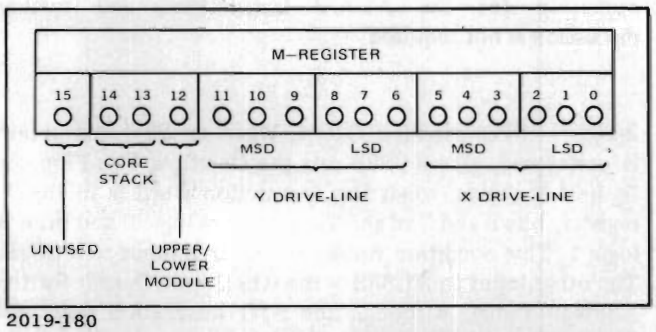


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Figure 3-17. Significance of M-Register Contents

3-213. Bits 14 through 12 of the M-register are also examined in the memory section to identify completely the memory location to be referenced. Bit 12 identifies the module, logic 0 indicating the lower module and logic 1 the upper module. Bits 13 and 14 designate the 8K core stack, if more than one is installed.

3-214. Y-Line Selection. Figure 3-18 illustrates in block diagram form the selection of Y-lines in core stack A20A1, the basic core stack containing octal addresses 00002 through 17777. The decoders, drivers, and switches shown in the illustration are on circuit card A21, and the core stack is on card A20. For other core stacks, different circuit cards are used for the Y-line selection circuits and for the core stack itself.

3-215. The "not" MOD0/1 signal in figure 3-18 results from decoding bits 14 and 13 of the M-register (figure 3-17). If the two bits are both logic 0, indicating the basic core stack, the "not" MOD0/1 signal becomes false. This signal is furnished to X-Y driver/switch card A21, covering addresses 00002-17777 (table 7-18). If bits 14 and 13 of the M-register are 01, 10, or 11 respectively, the "not" MOD2/3, 4/5, or 6/7 signal becomes false, and X-Y driver/switch card A18, A11, or A8 is selected. The "not" MOD signal, when false, serves as an enable for the binary-to-octal decoders on the card which receives the signal.

3-216. When Y-line current is required, the MRT1 signal becomes true (for readout), or the MWT1 signal becomes true (for writing). Upon occurrence of one of these signals, bits 11 through 9 of the M-register are decoded to furnish an octal equivalent, referred to as the Y most-significant-digit (MSD). (See figure 3-18.) As a result, one of the signals YD7 through YD0 becomes true (for readout), or one of the signals YC7 through YC0 becomes true (for writing). M-register bits 8 through 6 are similarly decoded to determine the Y least-significant-digit (LSD), resulting in one true signal in the group YB7 through YB0 (for readout), or one true signal in the group YA7 through YA0 (for writing).

3-217. As a result of the decoding process, a pulse is furnished to one of the eight drivers, and another pulse to one of the eight switches. A total of 64 combinations is possible. The selected driver furnishes a negative signal for readout, or a positive signal for writing. The selected switch provides a path to ground.

3-218. When the selected driver and selected switch receive an input pulse, electron current flows from the driver to the switch (when reading), or from the switch to the driver (when writing). This current flows through the addressed Y-line, which is identified by a 2-digit octal number corresponding to the Y MSD and Y LSD. Current does not flow through other Y-lines because the remaining switches do not furnish a path to ground and the drivers do not furnish a voltage.

3-219. The Y-lines pass through the ring-shaped ferrite cores shown in figure 3-18. Each core in the illustration

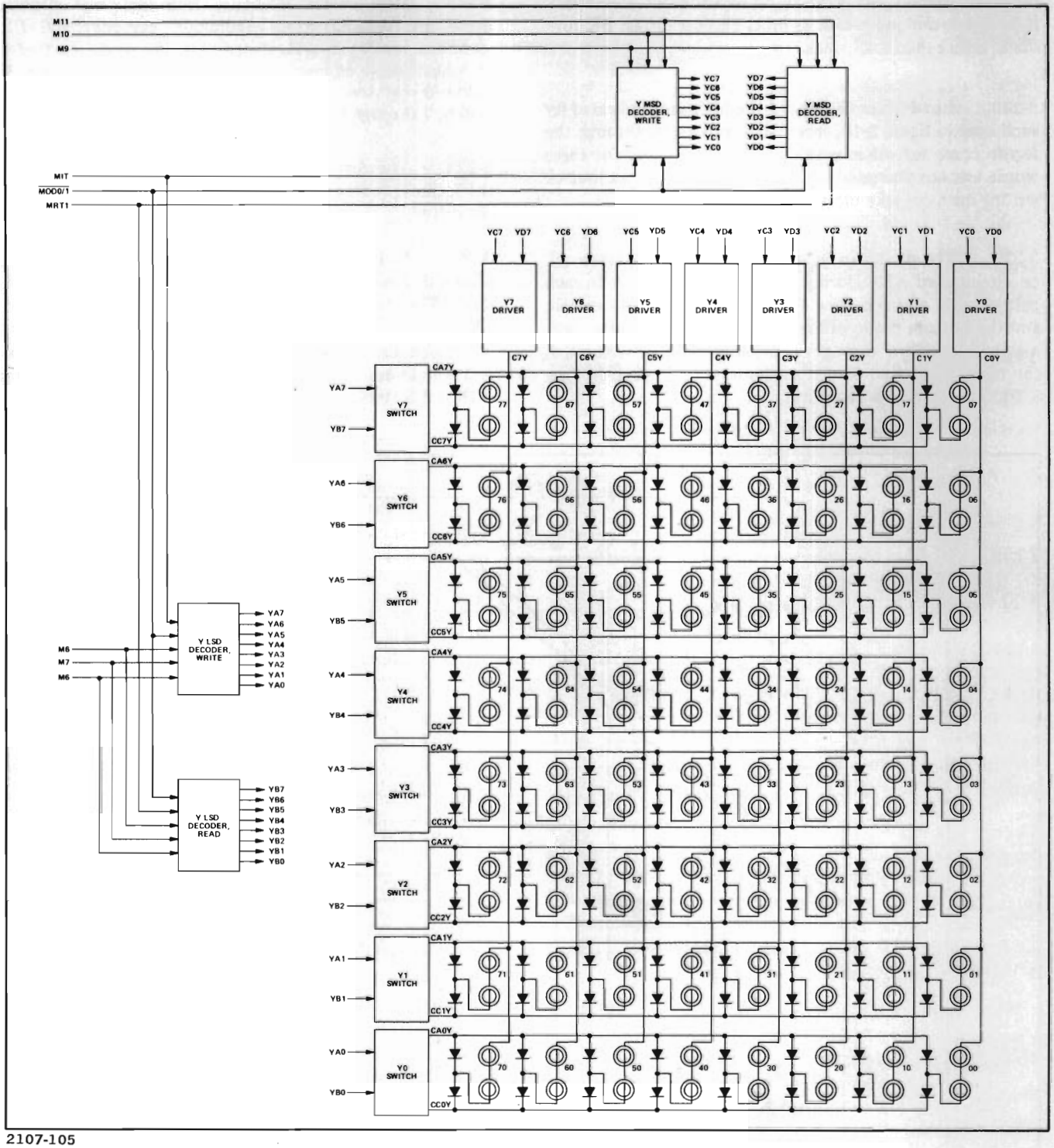

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Figure 3-18. Y-Line Selection Circuits, Core Stack A20A1, Block Diagram

represents the 16 cores of a word location in the core stack. (Physically, each location contains 17 cores. The 17th core is used when the Parity Error option is installed; however, the present discussion does not deal with this optional feature.) It will be noted that every Y-line in figure 3-18 is shown passing through two cores, representing two 16-bit storage locations. One of these locations is in the upper module of the core stack, and the other is in the lower module. An X-line (described later) passes through the same cores, and determines which of the two locations will be used. For one of the locations the X-line current aids the Y-line current. For the second location, the X-line current opposes the Y-line current. The storage location used is the one in which the currents aid. By reversing the direction of

the X-line current, the other 16-bit location can be selected. It is this technique which permits the use of an 8K core stack, rather than a 4K stack.

3-220. In addition to the two 16-bit words indicated by each core in figure 3-18, each Y-line also passes through the ferrite cores for other words. Because the cores for these words are not traversed by the selected X-line, readout or writing does not take place.

3-221. The diodes in figure 3-18 are near the core stack on circuit card A20. During readout, the top diode in each pair permits electron flow from the driver to the switch, and the bottom diode offers a high-resistance path to minimize current flow through it. When writing is performed, the roles of the two diodes are reversed, and electron flow is from the switch to the driver.

3-222. Each switch in figure 3-18 has two outputs. These are designated CC (common cathode) and CA (common anode) in accordance with the diode electrodes to which they connect. Each CC or CA designation is followed by the identifying number of the associated switch, 7 through 0.

3-223. The drivers each have one output, identified by the letter C (core), followed by the identifying number of the driver.

3-224. It is important to note that the diode matrix shown in figure 3-18 does not represent a plane of the core stack. The matrix in figure 3-18 has an 8 x 8 configuration, while the core-plane matrix is 64 x 64. Figure 3-19 shows a core-plane matrix, and indicates the manner in which the Y- and X-lines are connected. The numbered Y-lines in figures 3-18 and 3-19 correspond.

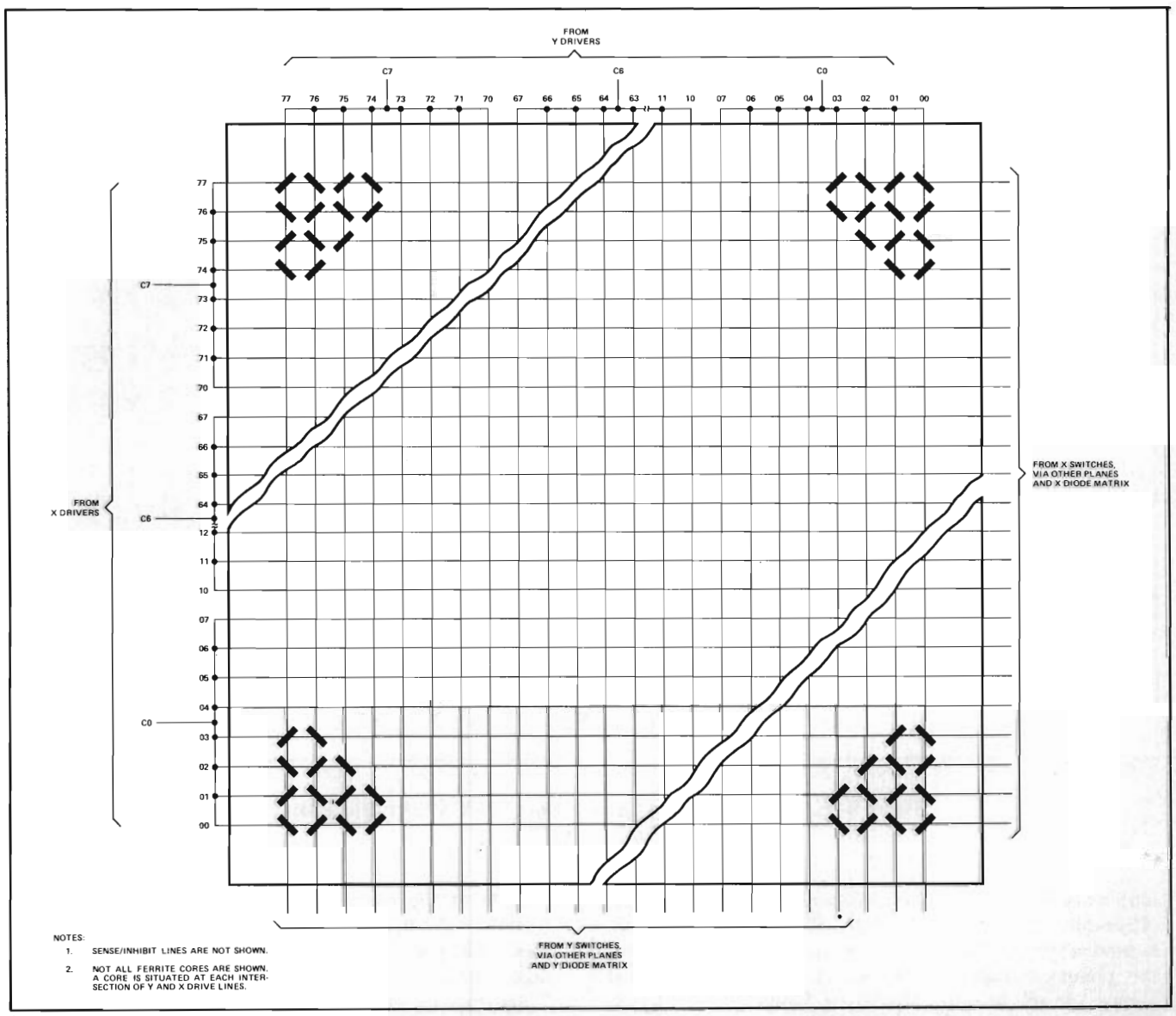

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Figure 3-19. Core Plane

3-225. X-Line Selection. The X-line circuits for core stack A20A1 are shown in figure 3-20. They differ from the Y-line circuits in the following respects:

a. The binary-to-octal decoders receive bit 5 through 3, or 2 through 0, of the M-register.

b. Instead of the MRT1 or MWT1 strobe pulse, either an XT1 or an XT2 pulse is furnished to each decoder.

c. For the cores in the upper module, X-line read or write current is in the reverse direction from that in the lower module. For the Y-lines, read or write current is the same in both modules.

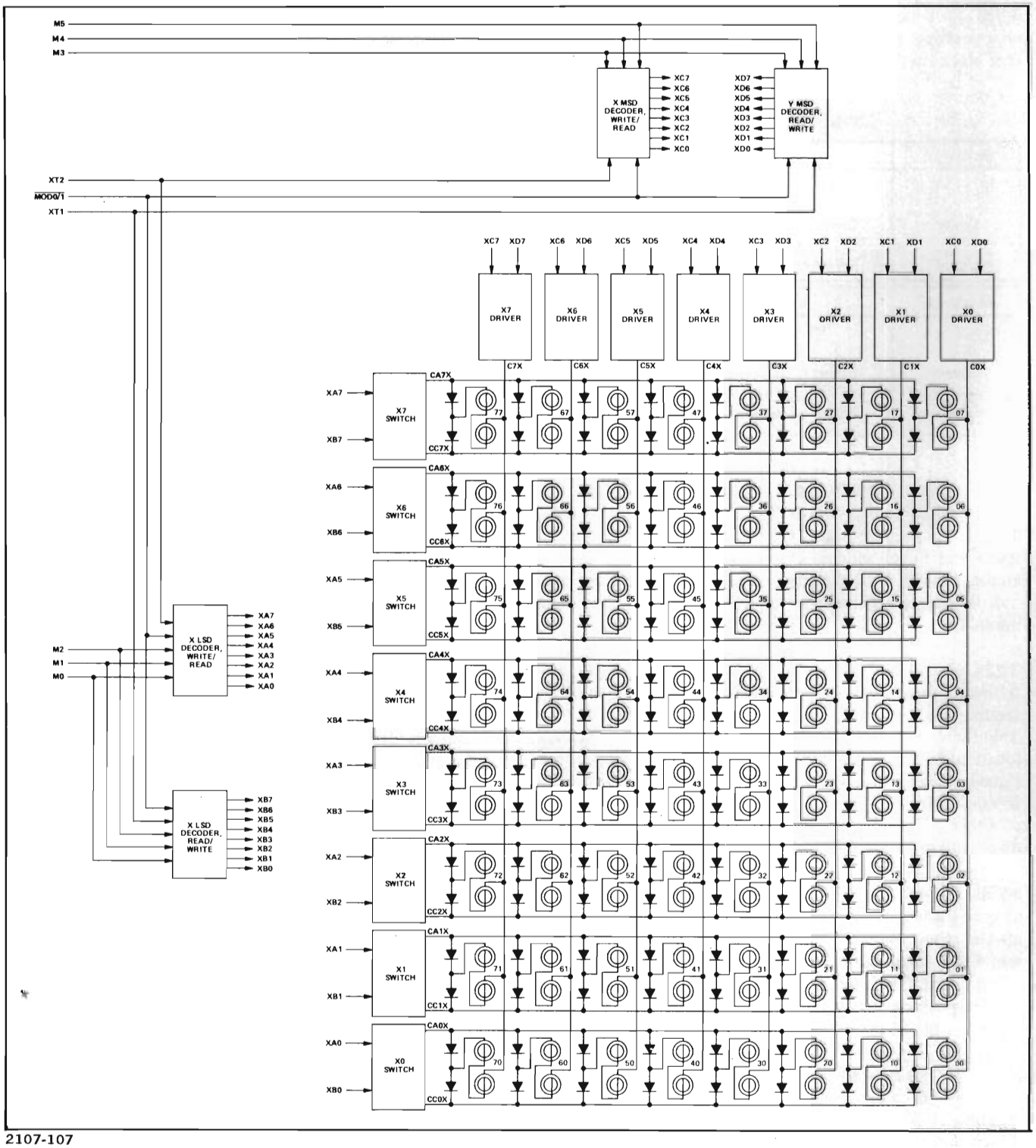

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Figure 3-20. X-Line Selection Circuits, Core Stack A20A1, Block Diagram

3-226. As pointed out earlier, a reversed-current technique with the X-lines permits the selection of a word in either the lower or upper module, using only a single pair of X and Y drive lines. The current reversal is brought about by the XT1 and XT2 pulses. If bit 12 of the M-register is logic 0, indicating the lower module, current flow for readout or writing is the same as for the Y-lines. If bit 12 is logic 1, indicating the upper module, X-line current flow is reversed.

3-227. Table 3-6 shows the direction of current flow for all operating combinations. The table is applicable to all core stacks in the computer.

Table 3-6. Electron Flow

MODULE	Y-LINE ELECTRON FLOW	
	READ	WRITE
Lower	Driver to switch	Switch to driver
Upper	Driver to switch	Switch to Driver
MODULE	**X-LINE ELECTRON FLOW**	
	READ	WRITE
Lower	Driver to switch	Switch to driver
Upper	Switch to driver	Driver to Switch

3-228. The X MSD and X LSD decoders in figure 3-20 are identified by the words "read/write" or "write/read". This terminology indicates the function of the decoders for lower and upper module operations, respectively. For example, the "X MSD decoder, read/write" is used for readout in the lower module, or for writing in the upper module.

3-229. OPERATION OF MEMORY SECTION. The following paragraphs explain the operation of the memory section, making use of the block diagram in figure 3-21. The discussion describes reading and writing in core storage location 05270, with general comments regarding operations in other storage locations. Of the 16-bit word read or written, only bit 0 is dealt with here. Reading and writing of other bits is identical, except that a separate inhibit driver and sense amplifier is used for each bit.

3-230. Core Stack. The core stack is made up of two sets of core planes, each set consisting of 17 planes and making up the lower or upper module. The core planes each contain 4,096 ferrite cores, and each plane stores one bit of a 17-bit word. The planes are numbered in accordance with the bit position in the word, with bit 15 being the high-order bit. Bit 16 is the parity bit.

3-231. The core stack utilizes a folded construction, and has eight or nine core planes in each physical plane. Figure 3-21 illustrates this construction, with the core stack shown partly unfolded to reveal internal wiring in the core stack.

3-232. Lower Module Read Operations. The following paragraphs describe a typical memory read operation, using address 05270 (octal). Figure 3-21 illustrates the operation, and figure 3-22 shows the timing relationships.

3-233. The core stack and module to be used, and the Y-line and X-line employed, are identified by positions 14 through 0 of the M-register (figure 3-23). The number in this portion of the register is one of the following:

a. The address of the next instruction (if the current instruction is a single-phase instruction).

b. The address of an address word (if the next phase is indirect phase).

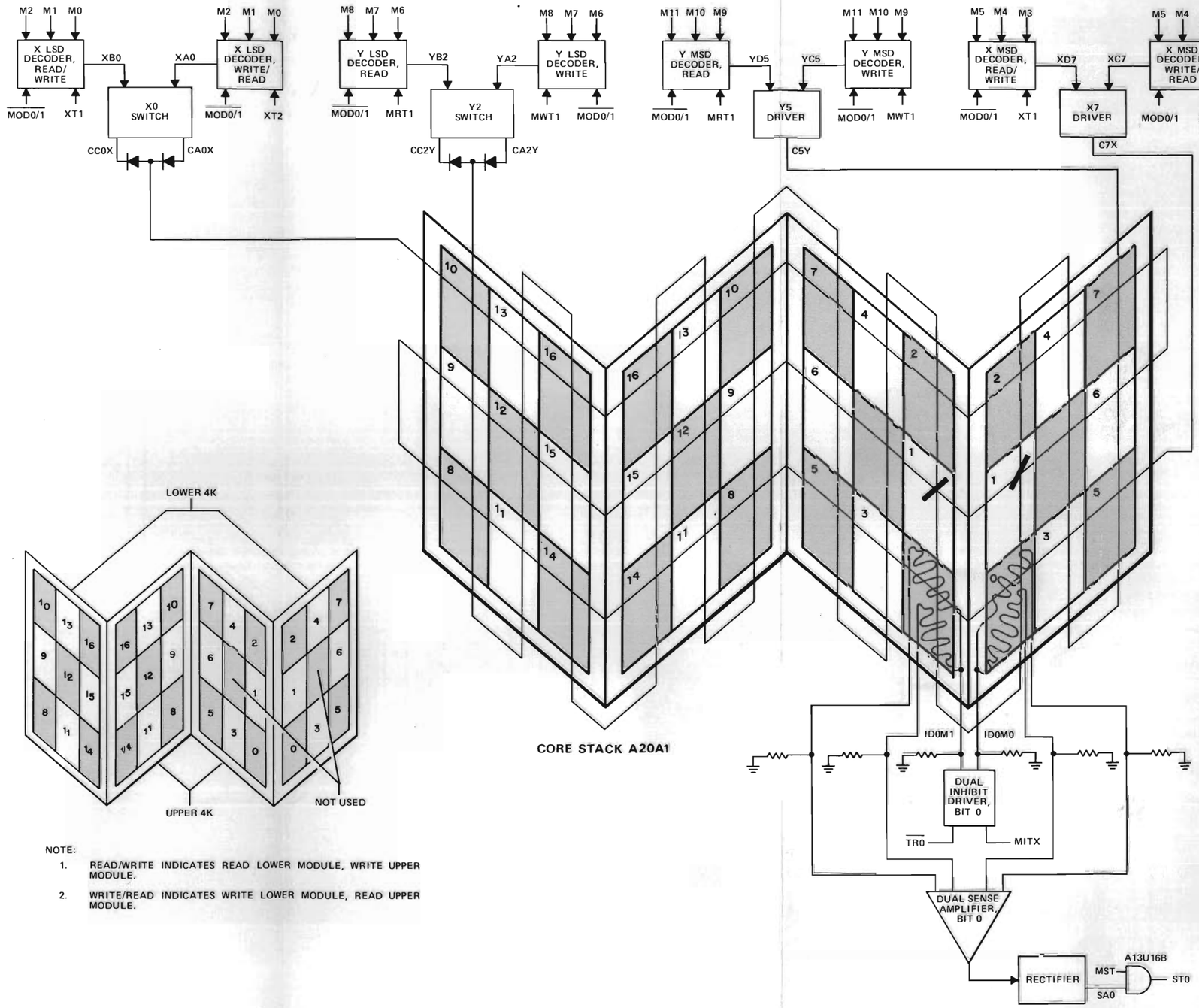
c. The address of an operand (if the next phase is execute phase).

3-234. As figure 3-23 indicates, the address within each page consists of part of the Y-line designation, and the entirety of the X-line designation. As explained earlier, this arrangement permits a memory reference instruction to specify an address in the current page or in page 0, using bits 9 through 0 of the instruction word. These bits, initially in the T-register, are transferred to the M-register (figure 3-1). The remainder of the M-register either remains unchanged (to obtain an operand from the current page), or is cleared (for page 0).

3-235. Bits 14, 13, and 12 of the M-register are examined to determine the stack and module to be used. This operation is dealt with in a later paragraph. Bits 12 through 0 are gated by "not" phase 5, and forwarded as bits M12 through M0 to the X and Y decoders (figure 3-21).

3-236. As table 3-2 shows, address 05270 is in the lower module of the core stack on circuit card A20, and is therefore in module 0. (For all addresses, the applicable module is indicated by the high-order digit of the 5-digit octal address. The modules in the four core stacks thus are numbered from 0 through 7.) Since the address being referred to is in module 0, the "not" module 0/1 signal becomes false, and the X and Y decoders on X-Y driver/switch card A21 are enabled. The Y most-significant-digit (MSD) is 5 and the Y least-significant-digit (LSD) is 2. Therefore, the Y MSD and Y LSD read decoders furnish a YD5 and YB2 pulse upon occurrence of the MRT1 pulse (figure 3-21). As table 3-6 indicates, electron current flows through the Y-line from the Y5 driver to the Y2 switch. Approximately 150 nanoseconds later the XT1 signal becomes true, and X-line current flows from the X7 driver to the X0 switch. At this time the ferrite cores in the addressed location change magnetic state if they are storing logic. As a result, the sense/inhibit winding passing through each of these cores generates a pulse, indicating readout of logic 1. After readout, all cores at the addressed location are in the logic 0 state.

3-237. Two sense/inhibit windings are shown in figure 3-21. One is for bit-plane 0 in the upper module, and the



NOTE:

1. READ/WRITE INDICATES READ LOWER MODULE, WRITE UPPER MODULE.
2. WRITE/READ INDICATES WRITE LOWER MODULE, READ UPPER MODULE.

Figure 3-21. Memory Section, Partial Block Diagram

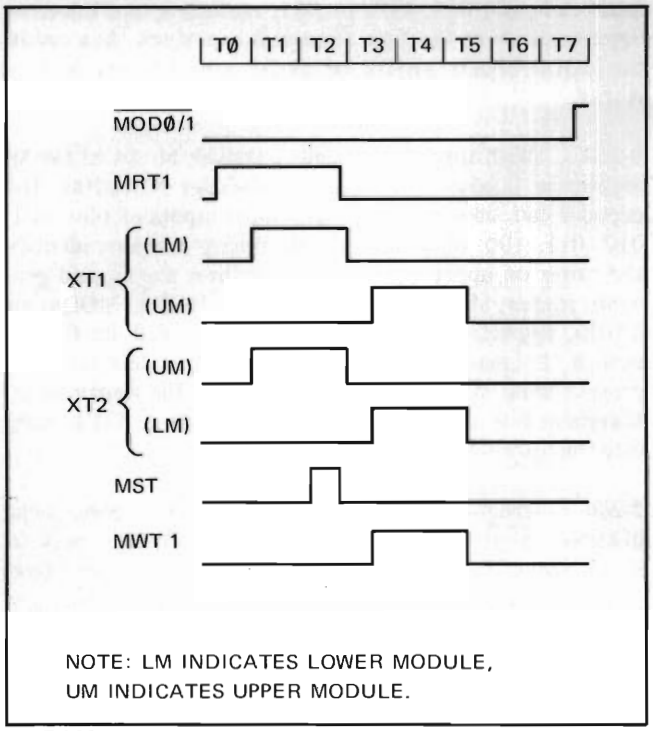


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Figure 3-22. Y-Line and X-Line Current, Timing Diagram

other for bit-plane 0 in the lower module. For clarity, the sense/inhibit windings for other bit planes have been omitted from the illustration. It will be noted that each sense winding consists of two halves; this serves to minimize electrical noise induced in the winding by half-selected cores. A dual inhibit driver is connected to the junction of the two half windings. During readout this connection to the inhibit driver is essentially an open circuit, and therefore plays no part in the operation.

3-238. The two ends of the sense/inhibit winding for bit 0 in module 0 connect to the dual sense amplifier for bit 0. This amplifier consists of two differential amplifiers, one for the lower module and the other for the upper module. When logic 1 is read from either module, at least 20 millivolts appears across the two ends of the applicable sense/inhibit winding. This voltage is applied to the two inputs to the differential amplifier for the lower or upper module. For logic 0, the voltage is under 10 millivolts. The differential amplifier for the module not in use receives only a slight noise potential.

3-239. The outputs of the differential amplifiers for the lower and upper module "or" together, and the resulting signal is rectified and furnished as the SA0 signal. Rectification is required because the sense/inhibit winding passes alternately across the bit plane in two directions, and therefore can traverse the selected ferrite core in either direction. As a result, the pulse induced in the sense/inhibit winding for logic 1 can be of either electrical polarity. The rectification process ensures that regardless of the polarity of the signal furnished to the differential amplifier, the SA0 signal is positive when a logic 1 is read. Essentially, the rectifier inverts the signal if it is of the wrong polarity.

3-240. Each core stack has its own dual sense amplifiers and bit rectifiers. The SA0 signal from each stack "ors" with the corresponding signal from the other stacks.

3-241. The MST signal gates the SA0 output into position 0 of the T-register. Figure 3-22 shows that the entire read operation is completed by the end of T2.

3-242. Lower Module Write Operations. Memory section writing is similar to reading. Address selection is the same, except that the Y-line is activated by the MWT1 signal rather than the MRT1 signal (see figure 3-21). As a result, current flows in the opposite direction through the Y-line. Similarly, the X-line is activated by XT2 instead of XT1, and again the direction of current flow is reversed. The Y-line and X-line currents attempt to place each ferrite core at the addressed location to logic 1. However, the sense/inhibit winding prevents this for each bit position in which there is a logic 0 in the T-register. In figure 3-21 the "not" TR0 input to the inhibit driver controls this function for bit position 0. The center-tapped connection of the inhibit driver permits current flow in the correct direction through the two halves of the sense/inhibit winding, allowing cancellation of the X-line and Y-line currents if logic 0 is required.

3-243. The abbreviations ID0M0 and ID0M1 in figure 3-21 stand for inhibit driver bit 0, module 0 or 1 respectively. Inhibit current flows only in the module being addressed, and its duration is the same as that of the MITX pulse (figure 3-22). The MITX pulse has the same timing as the MWT1 pulse, which controls Y-line current.

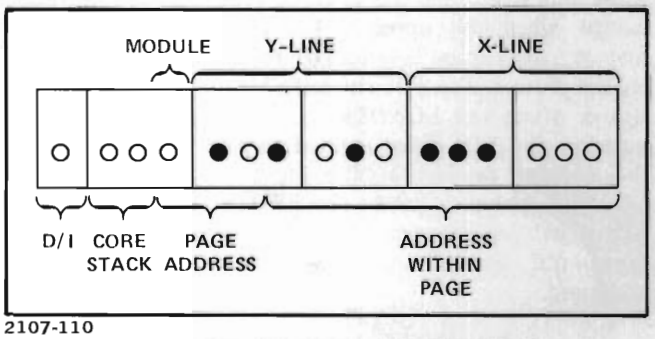

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Figure 3-23. M-Register Contents 05270

3-244. Upper Module Read Operations. Upper module read operations are the same as for the lower module, except that the X-line current is reversed and a different sense amplifier is used. In figure 3-21 it can be seen that the XT2 signal activates the X MSD and X LSD decoders for reading. This results in current flow through the X-line in the direction used for writing in the lower module. Figure 3-22 shows that the timing of the XT2 is changed during upper module read operations, resulting in readout during the first part of the machine cycle. This leaves the remainder of the machine cycle for writing.

3-245. Upper Module Write Operations. As with upper module reading, upper module writing employs reverse current in the X-line. The XT1 pulse activates the X MSD and LSD decoder. and the timing of this pulse is delayed as shown in figure 3-22. Inhibit current is in the same direction as for the lower module.

3-246. LOGIC DIAGRAM ANALYSIS.

3-247. The following discussion makes use of the logic diagrams in section VII to explain the operation of the memory section. Readout and store operations are described, using address 05270 (octal). Operations for other addresses are also described in general terms. As table 3-2 shows, the example address is situated in the lower module of the core stack on sense amplifier card A20.

3-248. ADDRESSING CIRCUITS. The address to be referenced is indicated by bits 14 through 0 of the M-register, which is situated on the four arithmetic logic cards (figure 7-12). The output of this register is forwarded to memory address decoder card A14 (figure 7-10). From there, if the computer is not in phase 5, bits 11 through 0 are forwarded to each of the four X-Y driver/switch cards (figure 7-7).

3-249. Memory address decoder card A14 selects the X-Y driver/switch card corresponding to the required core stack. Binary-to-octal decoder A14U106 performs this function. The decoder furnishes one true output, 0 through 7 octal, corresponding to the binary input received. This output identifies the module to be referenced. Modules 0 and 1 are in the first core stack, 2 and 3 in the second stack, and so on.

3-250. To provide an output, binary-to-octal decoder A14U106 requires a true enable at pin 4 and a false enable at pin 3. Pin 4 is connected to a permanently true source, while pin 3 receives the required false input at all times except when the upper 64 (decimal) addresses in the memory section are referenced. These upper 64 addresses are the protected area in which the binary loader program is stored. When the LOADER switch is at the ENABLED position, the LPS signal applied to card A14 is false, and the decoder receives a false input at pin 3. When the LOADER switch is set to the PROTECTED position the LPS signal becomes true, but pin 3 of A14U106 remains false until one of the upper 64 storage locations is addressed.

3-251. Decoder A14U106 furnishes the octal equivalent of the three binary digits applied to pins 8, 7, and 6 of the decoder. If the computer has only a single 8K core stack, pins 7 and 6 connect to an open circuit; the decoder interprets these open inputs as logic zeros. In this situation the decoder can receive only 000 or 001 (binary), the low order bit being derived from position 12 of the M-register. It has been seen that bit 12 indicates the lower or upper module (figure 3-23). Thus, the decoder indicates either module 0 or 1 in the basic 8K core stack, and the MOD0 or MOD1 output from card A14 is true. If a second stack is installed, the MMD13 signal is applied to the decoder, indicating the content of M-register position 13. If this bit is logic 0, the basic core stack on card A20 is designated. If the bit is logic 1, the second 8K stack, on card A19, is indicated.

3-252. With two core stacks installed, pin 6 of decoder A14U106 is open. Thus, the decoder can receive binary inputs of 000, 001, 010, or 011, indicating the lower or upper module of the first or second core stack. As a result, the MOD0, MOD1, MOD2, or MOD3 output from card A14 is true.

3-253. With three core stacks installed, bit 14 of the M-register is furnished to pin 6 of decoder A14U106. The decoder can then receive programmed inputs of 000, 001, 010, 011, 100, or 101. These six binary numbers identify the lower or upper modules of the three stacks, and generate signals MOD0, MOD1, MOD2, MOD3, MOD4, or MOD5, respectively. With four stacks installed, no further change is made to the input to the decoder, but programming may now make reference to the fourth stack. M-register bits 14, 13, and 12 are then 110 or 111 to indicate the lower or upper module of the fourth stack.

3-254. Program Foldover. With one or two core stacks installed, decoder A14U106 can make reference only to these stacks. The open input to pin 6 of the decoder (and to pin 7 as well, when only one stack is installed), results in the decoder treating the high-order bit or bits as logic 0 when a reference is made to an address beyond the installed storage capacity. A memory reference still takes place, but it is within the installed storage capacity (table 3-7). This effect is referred to as program foldover. With three stacks installed, reference to the third stack requires that pin 6 of the decoder receive logic 1 and pin 7 receive logic 0. The

Table 3-7. Program Foldover

NO. OF STACKS INSTALLED	NONEXISTENT MODULE ADDRESSED*	MODULE REFERENCED
1 (8K)	2	0
1 (8K)	3	1
1 (8K)	4	0
1 (8K)	5	1
1 (8K)	6	0
1 (8K)	7	1
2 (16K)	4	0
2 (16K)	5	1
2 (16K)	6	2
2 (16K)	7	3
3 (24K)	6	0
3 (24K)	7	1

*Designated by bits M14, M13, and M12.

MMD14 and MMD13 signals are therefore applied to these pins. However, if the program should make reference to the nonexistent fourth stack, pin 10 or 9 of the decoder will furnish a true output, although only the MOD0 through MOD5 signals can bring about memory operations in the three stacks installed. To maintain the program foldover effect with three stacks installed, gates MC33A and MC43A are provided. These gates receive the MPT3 signal at one input. With only one or two stacks installed, these gate inputs are open, and the gates interpret an open as logic 0. Thus, the gates are essentially nonexistent when one or two stacks are installed. When a third stack is used, the MPT3 signal is constantly true, and the gates are enabled. If pin 10 or 9 of decoder A14U106 should now furnish a true output, indicating reference to a fourth core stack, gate A14U33A or A14U43A makes the MOD0 or MOD1 signal true. As a result, reference is made to module 0 or 1 in the basic core stack.

3-255. When a fourth core stack is installed, the MPT4 signal becomes true and the MPT3 signal is constantly false. The MOD6 or MOD7 signal now becomes true when the fourth stack is addressed, and reference is made to the fourth stack. (With four stacks installed, the MPT3 signal is false as a result of card A8, the X-Y driver/switch card for the fourth stack, which shorts the MPT3 signal to ground where the signal enters the card at pin 28.)

3-256. Y-Line and X-Line Decoders. The preceding paragraphs explained how one of the signals MOD0 through MOD7 becomes true to indicate the required memory module. The module decoder on card A14 brings this about by examining bits 14, 13, and 12 of the M-register. The remainder of the address, indicated by M-register bits 11 through 0, is decoded by an X-Y driver/switch card. One of these circuit cards is installed for each core stack, and the module decoder determines the card to be used.

3-257. In figure 7-7 it can be seen that the "not" MOD0/1, MOD2/3, MOD4/5, or MOD6/7 signal is furnished to the X-Y driver-switch cards. When one of these signals becomes false it activates the card to which it is furnished; the other X-Y driver/switch cards remain inoperative. The false input to the selected circuit card serves as an enable to the Y-line and X-line decoders, U17 through U24.

3-258. The eight drive-line decoders on the selected card require, in addition to a false signal at the E2 input, a true signal at E1 in order to become operative. The E1 input is used to control the timing of the Y-line and X-line currents (figure 3-22), and to select the decoders required. For each memory read or write operation, two Y-line decoders and two X-line decoders are used. These decode the Y and X MSD and LSD. That is, they furnish the octal equivalent of a 3-bit binary input. Table 3-8 identifies the decoders for each core-stack module. The two MSD decoders in use each select a driver, and the two LSD decoders each select a switch.

3-259. In the representative read and write operation being discussed, the address is 05270 (octal). The first digit

Table 3-8. Y-Line and X-Line Decoders

MODULE ADDRESSED	Y MSD DECODER		Y LSD DECODER		X MSD DECODER		X LSD DECODER	
	READOUT	WRITE	READOUT	WRITE	READOUT	WRITE	READOUT	WRITE
0	A21U24	A21U23	A21U22	A21U21	A21U18	A21U17	A21U20	A21U19
1	A21U24	A21U23	A21U22	A21U21	A21U17	A21U18	A21U19	A21U20
2	A18U24	A18U23	A18U22	A18U21	A18U18	A18U17	A18U20	A18U19
3	A18U24	A18U23	A18U22	A18U21	A18U17	A18U18	A18U19	A18U20
4	A11U24	A11U23	A11U22	A11U21	A11U18	A11U17	A11U20	A11U19
5	A11U24	A11U23	A11U22	A11U21	A11U17	A11U18	A11U19	A11U20
6	A8U24	A8U23	A8U22	A8U21	A8U18	A8U17	A8U20	A8U19
7	A8U24	A8U23	A8U22	A8U21	A8U17	A8U18	A8U19	A8U20

NOTES:
1. The module addressed is indicated by bits M14, M13, and M12
2. The Y MSD is indicated by bits M11, M10, and M9.
3. The Y LSD is indicated by bits M8, M7, and M6.
4. The X MSD is indicated by bits M5, M4, and M3.
5. The X LSD is indicated by bits M2, M1, and M0.

in this address, 0, indicates that the addressed location is in module 0. From table 3-5 it is seen that the Y decoders for readout are integrated circuits U24 and U22 on circuit card A21. The next octal digits in the address, 5 and 2, are the Y MSD and Y LSD. Figure 7-7 indicates that for these inputs the YD5 and YB2 signals are furnished by U24 and U22 on card A21 when readout is performed. The YD5 and YB2 signals are true for the duration of the MRT1 pulse. When writing is conducted, the MWT1 signal is produced rather than the MRT1 signal. As a result, decoders U23 and U21 furnish signals YC5 and YA2.

3-260. The X-line decoders function in a manner similar to that of the Y-line decoders. However, for the lower module of a core stack the XT1 signal selects the two X decoders used for reading, and the XT2 signal selects the two X decoders for writing. In the upper module, the role of these two signals is reversed, as also is their timing. In the example lower-module address, 05270, the decoders produce signals XD7 and XB0 for readout, and XC7 and XA0 for writing. In the upper module of a core stack, the signals are XC7 and XA0 for readout, and XD7 and XB0 for writing.

3-261. Drivers and Switches. The decoder outputs are applied to the drivers and switches. In figure 7-7, the Y-line drivers and switches are in the lower part of the diagram; the X-line drivers and switches are in the upper portion. The decoder output signals received by these circuits are in alphanumeric sequence proceeding from left to right.

3-262. In the typical address under consideration, the YD5 signal is generated in a readout operation, and furnished to pulse transformer T13B. As a result, transistor U13D is driven from the cutoff condition into saturation. The C5Y output from the circuit card then becomes negative, and electron current can flow from U13D through a Y-line to a CC or CA terminal. Transformer T13B, transistor U13D, and their associated components, are a Y-line driver. Also part of the driver, but unused at this time, are T13A, U13C, and associated components. Each driver thus consists of two halves, of which one half is used at a time. The required direction of current determines the half to be utilized.

3-263. The Y LSD in the present example is 2. Therefore, as noted earlier, the YB2 signal on circuit card A21 becomes true when readout is performed. The YB2 signal is furnished pulse transformer T14C through current limiting resistor R90. As a result, the transformer secondary furnishes a pulse, bringing transistor U14B into conduction. This transformer and transistor constitute part of the Y2 switch. The remaining portion of the switch, consisting principally of T14D and U14A, is not used at this time.

3-264. In the present example, electron current flows from C5Y through Y-line 52 to CA2Y, then through U14B to ground. This current, amounting to about 400 milliamps, is the Y-line current. It flows through current-limiting resistor R160 on card A21, bringing a change in voltage at test point TP4 from -20 volts to about -4 volts. Capacitor C3 bypasses the resistor until the capacitor charges; this serves to steepen the leading edge of the Y-line current pulse.

3-265. Diode CR22, in the Y2 switch, protects transistor U14B. When pulse transformer T14C ceases to furnish an output to the base of transistor U14B, the transistor returns to the cutoff condition. However, the collapsing magnetic field around the Y-line attempts to maintain current flow. Diode CR22 shunts this current back to the -20 volt supply, to which the other end of the Y-line is connected by U13D in the Y5 driver. Transistor U13D cuts off at about the same time as transistor U14B, but resistor R46 in the Y5 switch furnishes a path for continued current flow in the Y-line until the magnetic field is entirely collapsed.

3-266. The distributed inductance, distributed capacitance, and lumped inductance of ferrite cores, give the Y-line the characteristics of a "lossy" transmission line. The Y-line thus exhibits the usual transmission line properties, including a characteristic impedance and propagation velocity. Resistor R22 in the Y2 switch provides termination resistance for the transmission line. Resistor R46, in the Y5 driver, serves a similar function at the other end of the Y-line. (Because current can flow either way through the Y-line, a termination resistor is needed at both ends. Their values differ because of the differing conditions of operation for the two cases.) The termination resistors furnish only an approximate match for the characteristic impedance of the Y-line because the number of ferrite cores to be set or cleared varies in accordance with the particular word being read or written. There is also a change in the characteristic impedance of the Y-line as cores change state. The use of termination resistors, even though only approximating the correct value, serves to minimize distortion of the square wave current pulse, to absorb energy from the core stack, and to assist in rapid recovery to a low noise condition.

3-267. As well as serving as a termination resistor for the Y-line, resistor R22 back-biases diode CR22 during the Y-line current pulse. While U14B is conducting, current flow through R22 and U14B provides the back-biasing voltage. Diode CR22 is then effectively out of the circuit. When U14B cuts off, the diode performs its designated function, described earlier, of furnishing a path for current induced by the collapsing magnetic field around the Y-line.

3-268. To generate the X-line current for lower-module readout, the XT1 signal becomes true shortly after the MRT1 signal initiates Y-line current (figure 3-22). For the address under consideration (05270), this results in X-line decoders A21U18 and A21U20 furnishing true XD7 and XB0 signals for the duration of the XT1 pulse. Consequently, current flows from C7X to CA0X. This current, amounting to about 400 milliamps, is the X-line current. The X-line driver and switch circuits are identical with those used by the Y-line; hence no further discussion is required for the X-line circuits.

3-269. Turning now to a write operation at address 05270, the Y decoders furnish signals YC5 and YA2, as noted earlier. The X decoders produce signals XC7 and XA0. The half of the selected driver and switch which remained unused during readout now comes into operation, and current flow in the Y-line and X-line is in the opposite direction from that used for readout. The cores at the selected address are therefore set to the logic 1 condition, unless inhibit current flows in the sense/inhibit line for the particular bit plane.

3-270. For addresses other than 05270, readout and write operations are similar to those described, except that the outputs of the MSD and LSD decoders for Y and X select different Y-lines and X-lines. For addresses not in module 0 or 1, a different X-Y driver/switch card is used, and readout or writing takes place in the core stack to which the outputs from the driver/switch card are connected.

3-271. Protective circuits are included on the X-Y driver/switch cards to prevent Y-line and X-line current from flowing during power turn-on and shut-down. This protection feature prevents destruction of data in core storage resulting from the uncontrolled transient conditions that occur as supply voltages rise or fall. The protective circuits also prevent abnormal memory references, possibly a result of component failure, at times when the MRT1, MWT1, XT1 or XT2 pulse is not furnished. Transistors Q5, Q6, Q7, and Q8, together with their associated passive components, provide this protection for the Y-lines. The corresponding components in the X-line circuits prevent undesired X-line current. Transistors Q9 and Q10 and their related components are used by both protection circuits.

3-272. In the Y-line protection circuits, the PON signal is applied by transistors Q9 and Q10 to diodes CR103 and CR104. These diodes, together with resistors R125 and R126, form an encoding gate. Paragraph A-27 describes the function of this type of gate. Because logic symbols are used in this manual only for integrated-circuit logic elements, figure 7-7 does not use the logic symbol presented in paragraph A-27 for this type of gate. If a logic symbol were used, in this instance it would have an inverting dot at the input.

3-273. The PON signal applied to the encoding gate becomes true after all operating voltages are furnished to the computer circuits; the signal remains true until power shut-down. Before PON becomes true, transistor Q9 is held in the cut-off condition as -2 and +4.5 volts rise to their operating levels. As a result, -2 volts is applied to the base of Q10. If the MRT1 or MWT1 signal should now become true, the base of Q10 is negative with respect to its emitter, and Q10 conducts. Diode CR104 or CR103 also conducts, and because of the low forward-voltage drop across Q10 and the diode, the base of Q5 or Q7 is clamped at a voltage between -2 volts and 0 volts. The base of Q5 or Q7 is then negative with respect to its emitter, and the transistor conducts. As a result, transistor Q6 or Q8 also conducts. Assuming Q6 conducts, diode CR99 is forward biased, and approximately -1.2 volts is applied to diodes CR68, CR66, and the corresponding diodes in the other Y-line drivers and switches. If YD0, YB0, or any of the other outputs from the Y-line decoders now attempt to become true, forward current flows through Q6, CR99, R115, and the remaining diode in the circuit. As a result, the top end of the primary of the pulse transformer is clamped at about ground potential, and the secondary is unable to bring a driver or switch into conduction.

3-274. Diode CR68, CR66, and the other diodes whose cathodes connect to resistor R115 constitute, with the resistor, an encoding gate. The function of this gate is to permit application of the clamp voltage to the pulse transformers during power turn-on or shut-down, while allowing isolation of the various pulse transformer inputs during normal operation.

3-275. The remaining power turn-on and shut-down protection circuits on the X-Y driver switch card function in the same manner as the typical portions of the protection circuits described above.

3-276. When the PON signal becomes true, the input encoding gate is shut off (diodes CR101, CR102, CR103, and CR104 become reverse-biased). The input to Q1, Q4, Q5, and Q7 is then free to follow the applied XT2, XT1, MRT1, or MWT1 signal. When one of these signals is true, the associated pulse transformers function in the normal manner. When the signal is false, operation is the same as that described for the power turn-on period. Thus, protection is also furnished at times other than power turn-on.

3-277. SENSE AMPLIFIERS. The sense amplifiers, situated on sense amplifier cards A20, A19, A10, and A9, amplify the output from the sense/inhibit lines, and produce a logic 1 or logic 0 signal of standard voltage level. Seventeen dual sense amplifiers are situated on each sense amplifier card. One portion of each dual amplifier senses the output from the sense/inhibit line in the lower module, and the other portion of the dual amplifier senses the output from the upper module. The outputs from the two portions of the sense amplifier "or" together. The seventeen output bits from each sense amplifier card "or" with the corresponding outputs from the other cards.

3-278. Figure 3-24 shows the sense amplifier circuit for bit 0 read from any address in the lower module of core stack A20A1. It will be noted that only half of the dual sense amplifier is shown. The half not shown is used for bit 0 in the upper module. Also not shown are the dual sense amplifiers for other bits. However, included in the illustration are control circuits which are common to all seventeen lower-module sense amplifiers on the circuit card.

3-279. For the representative address 05270 under consideration, the MOD0 signal becomes true, indicating the module to be used. After the Y-line and X-line current is initiated, the MSG signal becomes true. This signal, timed for the best signal-to-noise ratio, turns on the sense amplifiers for the lower module. When this occurs, the true output of U17B makes the base of transistor Q17 negative

with respect to the emitter, bringing the transistor into conduction. Current flows through R27, R26, Q17, and R25 to the +4.5 volt Vcc source for U17B. Diode CR1 clamps the collector voltage of Q17 at +0.6V (the forward voltage drop across the diode). As a result, the voltage at the junction of R26 and R27 maintains a level of approximately -7.5 volts. This voltage is applied to the base of transistor U15B through resistor R28, the resistor serving to suppress parasitic oscillation. The emitter of U15B is at approximately -8.6 volts; U15B therefore is able to conduct, with the collector current passing through transistors U15F and U15A and resistors R21 and R24, to the +12 volt supply. Transistor U15B thus serves to turn the sense amplifier on or off.

3-280. Transistors U15F and U15A, together with the components in their emitter and collector circuits, constitute a differential amplifier. This type of amplifier furnishes an output voltage determined by the potential differences between the two inputs to the amplifier. In the present instance, these inputs are the two extreme ends of the center-tapped sense/inhibit line. The IDOM0 input applied to the center tap is essentially an open circuit during readout. Resistor R84G establishes a ground-oriented reference point at the center tap; the two extreme ends of the sense/inhibit line therefore exhibit opposite changes in polarity when a voltage is induced in the line by readout of one of the 4,096 ferrite cores in the bit plane. One end of the sense/inhibit line therefore becomes negative with respect to ground, and the other becomes positive. The peak of the voltage pulse is at least 20 millivolts if logic 1 is read, or less than 10 millivolts for logic 0.

3-281. Transformer T1 and diodes CR1 and CR2 in the balun module serve a purpose during the inhibit function, described later. These components are paralleled by resistors R1 and R2, and have no significant effect during readout because current in the sense/inhibit line is relatively small.

3-282. If logic 0 is read out, the bases of U15F and U15A experience only a slight change in potential. The voltage at the collectors of these two transistors remains almost unchanged, and transistors Q16 and Q15 maintain the cut-off condition resulting from the identical potential at the base and emitter of each transistor. Emitter follower Q19 experiences no appreciable change in input, and the bottom input to gate U16B is logic 0. The MST pulse therefore does not cause coincidence in this gate, and bit position 0 of the T-register remains in the clear condition in which the entire register is placed shortly before readout.

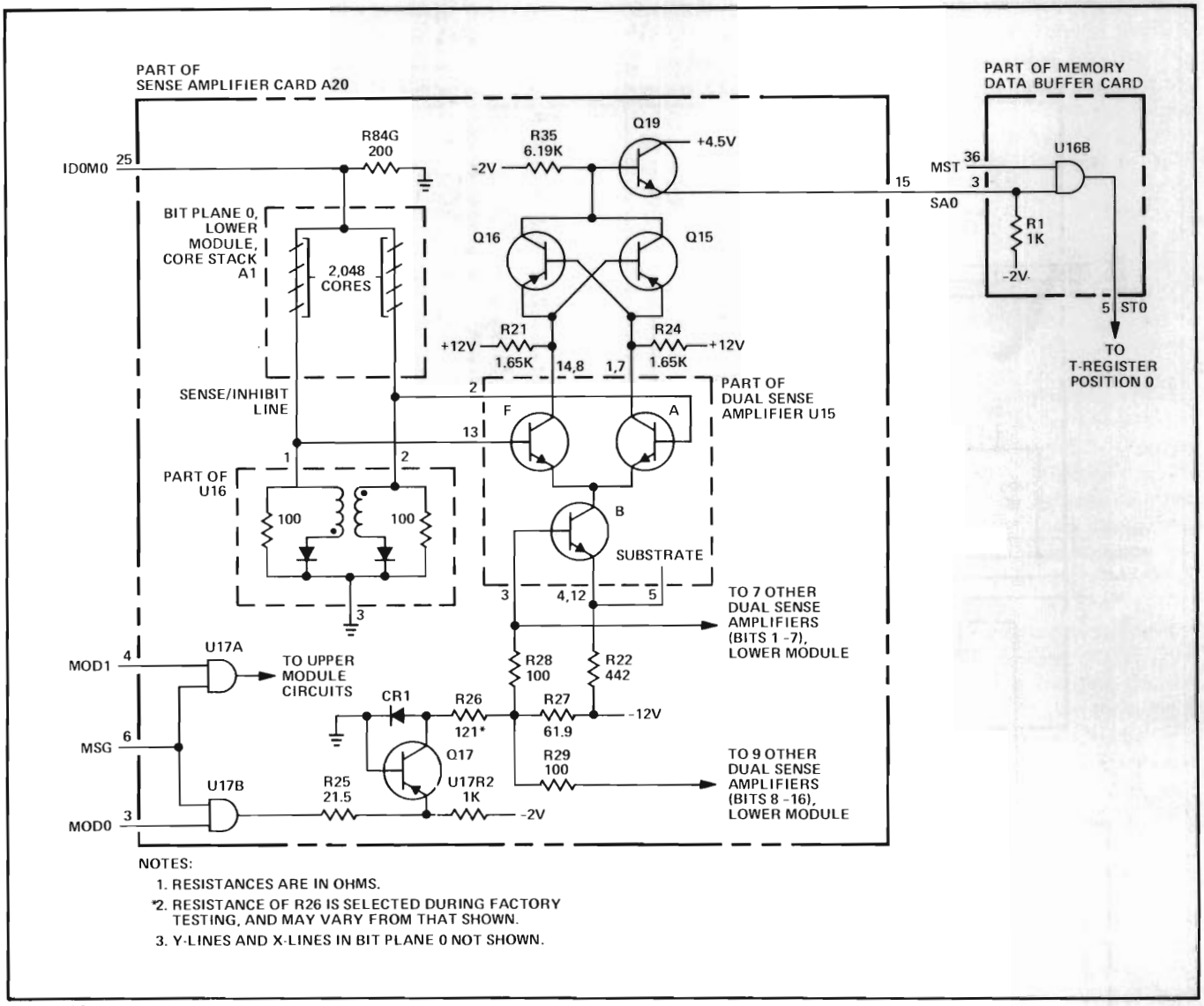
3-283. If logic 1 is read from the bit plane, transistors U15F and U15A experience a relatively large difference in potential between their bases. One transistor increases conduction and the other decreases conduction, and the collectors of these transistors change potential. Depending on the direction in which the sense/inhibit line traverses the selected core in the bit plane, either U15F or U15A could conduct more heavily than the other transistor of the pair. It is the function of Q16 and Q15 to act as a rectifier to ensure that when logic 1 is read, the input to transistor Q19 becomes more positive. Assuming U15F increases conduction during readout, the collector of U15F becomes less positive. As a result, the base of Q15 becomes less positive. Also, the emitter of Q15 becomes more positive as a result of decreased conduction through U15A and R24. Transistor Q15 conducts and a positive voltage is applied to the base of Q19. On the other hand, if the bit plane output voltage is the reverse of that described, transistor Q16 conducts, again applying a positive potential to Q19. In either case, emitter follower Q19 applies a true signal to gate U16B, and upon occurrence of the MST signal logic 1 is placed in bit position 0 of the T-register.

3-284. In figure 3-24 it will be noted that the substrate of integrated circuit U15 is connected to the emitter of U15B. This conforms with a requirement that the substrate be negative with respect to all collector terminals in this type of integrated circuit.

3-285. INHIBIT DRIVERS. As noted earlier, the inhibit drivers prevent the writing of logic 1 in designated bit positions of a core storage location. In doing this, the inhibit driver causes a 400-milliamp current to flow through the sense/inhibit line of the appropriate bit plane; this takes place when Y-line and X-line current flows. The Y-line and X-line currents, each 400 milliamps, flow through the addressed ferrite core in the opposite direction from that of the inhibit current. Thus the effective current through the core is 400 milliamps, and since this is sufficient only to half select the ferrite core, the core remains in the logic 0 state in which it is placed during readout.

3-286. Figure 3-25 shows the dual inhibit driver for bit position 0 in the lower and upper modules of core stack A20A1. The representative storage location under consideration, 05270, is in the lower module of this stack. Included in the illustration is a portion of sense amplifier card A20. The principal components of the dual inhibit driver in the illustration are transistors Q1, U11B, Q2, and U11C. Transistors Q1 and U11B, and their associated components, are the inhibit driver for bit plane 0 in the lower module, while Q2, U11C, and associated components, are the inhibit driver for bit plane 0 in the upper module.

3-287. Gates U2B and U2A select the lower- or upper-module inhibit driver under control of the MOD0 and MOD1 signals. In the present example, a lower module operation is under consideration. Therefore, bit 12 of the M-register is logic 0, and as a result the MOD0 signal is true. With the occurrence of the MITX pulse, gate U2B furnishes a true output. If position 0 of the T-register contains logic 0, the "not" TR0 signal is true, and gate U1C furnishes a pulse to the base of transistor Q1 for the duration of the MITX pulse. Current flows from ground through current limiting resistor R19, through Q1, and the primary of pulse transformer T1A to +4.5 volts. Transformer T1A couples the pulse to the base of transistor U11B, while isolating from each other the differing dc voltage levels in the primary and secondary circuits of the transformer. The pulse transformer also prevents the coupling of common



NOTES:

1. RESISTANCES ARE IN OHMS.
2. *RESISTANCE OF R26 IS SELECTED DURING FACTORY TESTING, AND MAY VARY FROM THAT SHOWN.
3. Y-LINES AND X-LINES IN BIT PLANE 0 NOT SHOWN.

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Figure 3-24. Sense Amplifier Circuits, Partial Logic Diagram

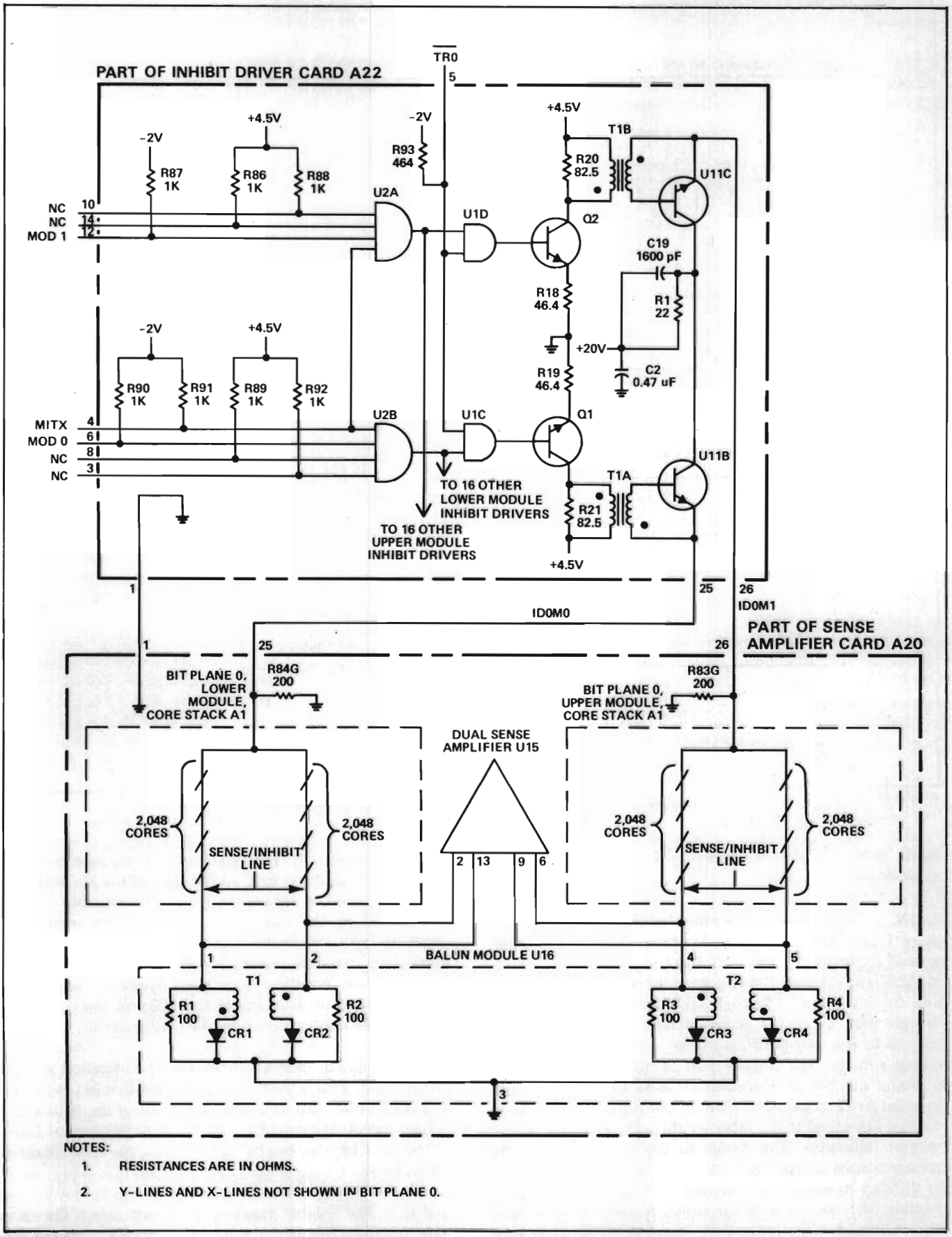
mode noise to the secondary, with the exception of capacitive-coupled noise.

3-288. The output of the pulse transformer brings transistor U11B into conduction. Electron current flows from ground through CR1 and CR2 and the two portions of T1 in A20U16, through the two portions of the sense/inhibit line for bit plane 0, through Q11 and R1, to +20 volts. Transformer T1 in the balun module serves to equalize current in the two portions of the sense/inhibit line. The currents in the two circuits tend to differ because of the differing number of half-selected cores in each path. An increase or decrease of current in one winding of T1 produces a like effect in the other winding, thereby minimizing current imbalance. The diodes in the balun module clip voltage spikes, preventing damage to the balun transformer or differential amplifier. Resistors R1 and R2 in the balun module decrease the Q of the circuit to prevent oscillation and to furnish surge protection. Resistor R84G serves as a termination resistor for the sense/inhibit line, which has transmission-line characteristics.

3-289. Resistor R21, on the inhibit driver card, serves to limit current in the circuit. At the start of the inhibit pulse, R21 is bypassed by capacitor C19; this allows rapid buildup of current in the circuit to overcome the inductance resulting from the ferrite cores. Capacitor C2 performs a decoupling function, minimizing change in potential on the +20 volt line resulting from the increased voltage drop along the +20 volt line, and in the +20 volt source, due to the increased current drawn by the inhibit circuit.

3-290. Inhibit current flows for the duration of the MITX pulse. This pulse has the same duration as the MWT1 and XT2 pulses, which respectively control the Y-line and X-line currents (figure 3-22). Thus, the inhibit current flows at the same time as, but in opposition to, the X and Y drive line currents.

3-291. The inhibit function does not affect the dual sense amplifier because the amplifier does not receive the signal, derived from MSG, required to turn the amplifier on. Also, during writing the inputs to the amplifier are essen-



NOTES:

1. RESISTANCES ARE IN OHMS.
2. Y-LINES AND X-LINES NOT SHOWN IN BIT PLANE 0.

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Figure 3-25. Inhibit Driver Circuits, Partial Logic Diagram

tially open circuits as far as loading the sense/inhibit line is concerned.

3-292. At the termination of the inhibit current pulse, transistor Q1 on the inhibit driver card cuts off. Resistor R21 provides a path for the collapsing magnetic field in the primary of T1A.

3-293. If bit position 0 of the T-register contains logic 1 when writing takes place, gate U1C on the inhibit driver card does not experience coincidence, and no inhibit current is furnished.

3-294. For other positions of the 16-bit word, operation is identical with the functioning for bit 0.

3-295. For inhibit operations in module 1, gate U2A on the inhibit driver card is activated. The inhibit drivers connected to the upper-module sense/inhibit line are then brought into use.

3-296. For modules other than 0 or 1, other inhibit driver cards are used. One card is installed for each core stack.

3-297. DETAILED THEORY, INPUT/OUTPUT SECTION.

3-298. The technical theory of the input/output section is covered in general terms in Volume III. The following paragraphs provide detailed treatment of this portion of the computer. The discussion first covers I/O control card A201, then deals with I/O address card A202 and resistance load card A218. For detailed theory discussions of the related I/O interface cards and I/O devices, refer to the manual for the applicable interface card or I/O device.

3-299. I/O CONTROL CARD.

3-300. The main function of the I/O control card is to control the interrupt system. The various output signals from the card which bring about these operations are furnished to the interface cards and the control section. In addition to controlling the interrupt system, the I/O control card also provides certain reset and clock signals, and controls selection of the switch register and the Overflow Flip-Flop.

3-301. A logic diagram of the I/O control card is furnished in figure 7-19. Unless otherwise stated, all circuit elements mentioned in the following discussion are situated on this circuit card. During the course of the discussion, reference should be made to the logic diagram as required.

3-302. POWER TURN-ON. At power turn-on, the I/O control card furnishes signals which establish predetermined conditions in the I/O system. This prevents undesired operation of I/O devices which could result from random flip-flop states, and prepares the I/O system for operation in the normal manner.

3-303. When power is initially applied, the computer is set to the halt condition, and is placed in phase 1. As this is done, the POPIO signal is received by the I/O control card. This signal consists of a series of T5 pulses, lasting for about 40 milliseconds. The POPIO signal can also be produced any time after power turn-on by pressing the PRESET push-switch when the computer is not running. In this instance the POPIO signal continues for as long as the switch is pressed, and produces the same effect as at power turn-on.

3-304. The functions performed by the POPIO signal are listed below, and described in the paragraphs that follow:

a. Disable the interrupt system.

b. Furnish a false ESR signal to the I/O address card.

c. Place the Flag Buffer, Flag, and IRQ Flip-Flops in a predetermined state (on each I/O interface card that has these flip-flops).

d. Reset the Control Flip-Flop on all interface cards that have this flip-flop.

3-305. Disabling of Interrupt System. The POPIO signal resets the Interrupt System Enable Flip-Flop (MC66) through diode CR1, thereby disabling the interrupt system. (The flip-flop consists of two "nor" gates which are connected so the flip-flop can be reset by a true signal to either the reset-side input or the reset-side output of the flip-flop.)

3-306. False ESR Signal. When the Interrupt System Enable Flip-Flop has been reset by the POPIO signal, the true reset-side output of the flip-flop is applied to gate MC27A through diode CR3. The output of MC27A is then false. This false ESR signal is forwarded to the I/O address card, where it prevents an interrupt signal from being furnished to the computer control section. If an interrupt signal could be furnished, it would place the computer in the interrupt phase (phase 4); this could occur any time between power turn-on and the starting of the computer if the false ESR signal did not prevent such an occurrence.

3-307. Diode CR1 allows application of the true POPIO signal to the Interrupt System Enable Flip-Flop, while preventing the reset-side output of the flip-flop from affecting the level of the POPIO line when POPIO is false. Diode CR3 similarly allows application of the true reset output of the Interrupt System Enable Flip-Flop to MC27A, while preventing application of the HIS signal to gate MC97B.

3-308. Flag Buffer, Flag, and IRQ Flip-Flops. The output of gate MC86A is the POPIO(B) signal. When true, this signal sets the Flag Buffer Flip-Flop on all interface cards having such a flip-flop. To reset the IRQ Flip-Flop on each interface card, the ENF signal is furnished. This signal is true during T2, regardless of whether the computer is running or halted. When the Flag Buffer Flip-Flop is set and the IRQ Flip-Flop is reset, the Flag Flip-Flop is placed in the set state. On some types of interface card, however, the Flag Flip-Flop is reset by the POPIO signal.

3-309. Control Flip-Flop. The POPIO signal passes through driver gate MC87A, and is furnished to all interface cards as the CRS signal. This signal resets the Control Flip-Flop or Control Bit Flip-Flop on each interface card having such a flip-flop. The CRS signal also resets the Interrupt Control Flip-Flop on the I/O control card.

3-310. Resetting the Control Flip-Flops on the interface cards prevents an interrupt from occurring immediately when the interrupt system is enabled. (The system is enabled by setting the Interrupt System Enable Flip-Flop on the I/O control card.) The Interrupt Control Flip-Flop on the I/O control card is reset by the CRS signal to ensure that the ESR signal remains false when the POPIO signal ends. As a result, an interrupt cannot be furnished by the I/O address card until the interrupt system is enabled.

3-311. As explained in detail in a later paragraph, the CRS signal can be produced by a CLC instruction that has a select code of 00 (octal). This produces the same results as the CRS signal produced from the POPIO signal.

3-312. SIR SIGNAL. At each T5 clock time, the T5 signal is sent to the I/O control card. After being applied to gate MC57B, this signal is forwarded to all interface cards as the SIR (Service Interrupt Request) signal. This signal enables the setting of the IRQ (Interrupt Request) Flip-Flop on all interface cards in order to provide Flag and IRQ signals to the I/O address card during an interrupt request. This signal is also applied to the set input of the PH4/5 SYNC 2 Flip-Flop on the I/O control card, causing the flip-flop to apply a true output signal to pin 6 of gate MC47B. A detailed description of the PH4/5 SYNC 2 Flip-Flop is provided in a later paragraph.

3-313. PRIORITY-AFFECTING INSTRUCTIONS. Four instructions, STC, CLC, STF, and CLF, affect the priority structure of the input/output devices. Whether a device can request an interrupt depends on whether its interface card Control Flip-Flop is set or reset (STC,CLC) or its Flag Flip-Flop is set or reset (STF,CLF).

3-314. If an I/O device cannot request an interrupt, it is not recognized as part of the interrupt priority structure. In this case, all succeeding I/O devices are effectively moved up in priority.

3-315. The four instructions also inhibit all interrupts during the machine cycle in which they occur, plus one machine cycle. This is done by removing the true ESR (Enable Service Request) signal from the I/O address card. This prevents interrupts during JMP,I and JSB,I instructions during entry and exit from subroutines. Also, a combination of two of the four instructions are normally the next-to-last instruction in a service subroutine processing an interrupt (the last being a JMP,I instruction to cause return to the main program or to an address in another service subroutine). If another input/output device could interrupt immediately after execution of these instructions (and before the JMP,I instruction), the possibility would exist that the first device may interrupt a second time before the JMP,I instruction is performed. In this event, the first main-program address (or the other service-subroutine address) stored in the beginning of the service subroutine would be destroyed, preventing a return to the main program or to the other service subroutine.

3-316. When any of the four instructions are programmed, the STC, CLC, STF, and CLF signals are received by the I/O control card and applied to one of the MC77A through MC77D isolator gates. The applicable gate output then supplies a true input to gate MC37C. The MC37C output becomes true during time T3 receipt of clock signal TS and the IOGE signal from gate MC57A.

3-317. The IOGE signal is sent to the I/O control card at T3 of each machine cycle in which an I/O Group instruction is performed. The other input to gate MC57A is the IOGE signal which has been delayed by about 70 nanoseconds to eliminate any noise which may have been generated during its formation. (The delay is caused by gates MC55A and MC55B, resistor R3, and capacitor C3.) At the end of the delay, gate MC57A provides a true output to gate MC37C, and a buffered IOGE signal to all interface cards. The IOGE(B) signal is an enabling signal for the I/O instruction and the select code transferred to the selected interface card.

3-318. The true output of gate MC37C is applied to gate MC36B. When not in phase 5, the other input to MC36B is true due to the inversion of the false PH5 signal by gate MC37B. The true output of gate MC36B resets the Interrupt Control Flip-Flop. The true reset-side output of the Interrupt Control Flip-flop is applied to gate MC27A, removing the true ESR signal from the I/O address card. Interrupt signals are now effectively blocked from the control section for the remainder of the current machine cycle.

3-319. At time T7 of the current machine cycle, the STM signal sets Interrupt Timing Flip-Flop MC16. At time T0, TS of the next machine cycle, the true output of MC36A resets the Interrupt Timing Flip-Flop. The set-side output of the Interrupt Timing Flip-Flop is applied to the Interrupt Control Flip-Flop. The Interrupt Control Flip-Flop is set at time T0, TS by the trailing (negative-going) edge of the Interrupt Timing Flip-Flop output. The false reset-side output of the Interrupt Control Flip-Flop is inverted by gate MC27A, providing a true ESR signal input to the I/O address card, and allowing interrupt signals to be furnished to the control section.

3-320. RESETTING CONTROL FLIP-FLOPS. The Control Flip-Flop on all interface cards can be reset by the CLC instruction with a select code of 00. The CLC signal is applied to gate MC76B. The other input to MC76B is from the output of gate MC67C. This gate output is true when select code 00 (octal) is received at pins 36 and 38, and the output of the gate MC57A is true. The true output of gate MC76B then applies a CRS signal to all interface cards. The CRS signal resets the Control Flip-Flop on the interface cards to prevent an interrupt request from any input/output device.

3-321. PHASE OPERATION. Operations controlled by phase signals PH4, PH1, and PH5 are described below.

3-322. Phase 4. During phase 4 (interrupt phase), the PH4 signal and the T3 clock signal are received by the I/O control card. The T3 signal, after passing through gate MC35A, is applied to gates MC37A and MC36C as the T3(B) (buffered T3) signal. It is also sent out of the I/O control card to all I/O interface cards. The PH4 input signal is also applied to gates MC37A and MC36C. When the PH4 signal and the T3(B) signal are simultaneously applied to gate MC37A as input signals, (during time T3 of a phase 4), a true output signal from MC37A is applied to the Interrupt Control Flip-Flop as a reset pulse. The resulting true reset-side output signal of the flip-flop is inverted by gate MC27A and sent to the I/O address card as a false ESR (Enable Service Request) signal. This action inhibits the INT (Interrupt) signal to the control section until after the program counter steps (time T7 of fetch phase). The PH4 and T3(B) signals are also simultaneously applied to gate MC36C at time T3 of Phase 4. This causes gate MC36C to apply a true output signal to the direct set input of the PH4/5 SYNC 1 Flip-Flop, which then applies its set-side true output signal to gate MC47B. This signal, when true, remains in a true state as an input to gate MC47B until the PH4/5 SYNC 1 Flip-Flop is directly reset by the POPIO pulse or is clocked by the IAK (Interrupt Acknowledge) signal at time T1 of fetch phase.

3-323. Phase 1. At time T2 of phase 1 (fetch phase), directly following the interrupt phase, the PH1 signal and signal T1 are applied as inputs to gate MC37B. The true output of gate MC37B supplies one input of gate MC35B. The other input to MC35B is the true reset-side output of the Interrupt Control Flip-Flop. When both these inputs are true, gate MC35B sends the IAK signal to all interface cards. This signal causes the Flag Buffer Flip-Flop on the interface card which initiated the interrupt to be reset. The IAK signal is also applied to the PH4/5 SYNC 1 Flip-Flop (MC46), on the I/O control card, as a clock pulse.

3-324. The ESR signal is inhibited between phase 4 and time T7 of the fetch phase of the instruction in the interrupt location, unless further disabled by a JMP-I or JSB-I instruction in the interrupt location. This ensures full execution of at least one instruction before the interrupt system is again enabled. At time T7 of the fetch phase, the STM signal sets the Interrupt Timing Flip-Flop. The flip-flop is reset at time T0,TS of the next machine cycle by the true output of gate MC36A. The trailing-edge output of the Interrupt Timing Flip-Flop sets the Interrupt Control Flip-Flop at time T0,TS. The false reset-side output of the Interrupt Control Flip-Flop is inverted by gate MC27A, providing a true ESR signal to the I/O address card, and again enabling the interrupt system.

3-325. Phase 5. Phase 5 is a one-cycle suspension of normal computer operation caused by the DMA (Direct Memory Access) computer option. Phase 5 is generated by the DMA option when the option is ready to operate. When Phase 5 is generated (always at time T6 of the machine cycle immediately preceding phase 5 operation), the HIS (Hold Interrupt System) signal is received by the I/O control card. This signal is then applied to gate MC27A where it is inverted and sent to the I/O address card as a false ESR signal. When phase 5 begins (T0 of the phase 5 machine cycle), the PH5 signal is received by the I/O control card and is applied to gate MC27B and gate MC45B. The resulting false output of MC27B is sent to the I/O address card as the false PH5 signal. The output of gate MC45B during phase 5 is dependent upon the state of the output signal from the set-side of the PH4/5 SYNC 1 Flip-Flop. If phase 5 was not immediately preceded by a phase 4, the input signal to pin 8 of gate MC45B will be false throughout the entire phase 5 machine cycle. In this case MC45B will apply a false signal to the PH4 line during phase 5.

3-326. If phase 5 has been immediately preceded by a phase 4, pin 3 of gate MC47B receives a true input signal during all of phase 5 from the PH4/5 SYNC 1 Flip-Flop. At time T5 of phase 5, the SIR signal from gate MC57B is applied as a true signal to the set input of the PH4/5 SYNC 2 Flip-Flop. The resulting true output signal from the set-side of the flip-flop is then applied to pin 6 of MC47B. Gate MC47B then applies a true output signal to gate MC45B. With the PH5 signal at pin 6 and the true output signal from gate MC47B at pin 8, gate MC45B experiences coincidence (at the end of time T5 of Phase 5). When this occurs, MC45B applies a true output signal to the PH4 line allowing the contents of the M-register to be updated to the current highest priority interrupt location.

3-327. SWITCH REGISTER AND OVERFLOW REGISTER SELECTION. Select code 01 must be used to enter the switch register setting into the A- or B-register when using instructions LIA/B and MIA/B. Select code 01 must also be used with input/output instructions STO, CLO, SOC, and SOS to perform operations using the 1-bit Overflow Register. Select code 01 causes the SCM0 and SCL1 signals to be applied to gate MC47C. The third input to MC47C is the IOGE(B) signal, which becomes true during time T3. The output of MC47C causes gate MC76A to furnish the IOS signal. The IOS signal enables the applicable Switch Register or Overflow Register operations.

3-328. INTERRUPT SYSTEM CONTROL. The programmed set or reset condition of the Interrupt System Enable Flip-Flop determines whether the interrupt system is on or off. If the flip-flop is set, the IEN signals to the interface cards permit interrupt requests; if the flip-flop is reset, the IEN signals are false and interrupt requests will not be recognized. Initially, the interrupt system is disabled by the POPIO signal.

3-329. Interrupt System Enable. If the interrupt system is to function, the Interrupt System Enable Flip-Flop must be set by an STF instruction with a select code of 00. When this is programmed, the SCM0 and SLC0 signals are received by the I/O control card and applied to gate MC67C. The remaining input to gate MC67C is the true IOGE(B) signal. The true output of MC67C is "anded" with the STF signal at time T3. The true output of gate MC67A sets the Interrupt System Enable Flip-Flop.

3-330. The ESR signal is produced when there is a false input to pin 1 or pin 2 of gate MC27A. The input to pin 1 is supplied either by the HIS signal, the reset output signal from the Interrupt System Enable Flip-Flop, or the POPIO signal. The input to pin 2 of MC27A is the reset output signal from the Interrupt Control Flip-Flop. The true ESR signal is applied to the I/O Address card.

3-331. Refer to figures 3-26 and 7-19. The true set-side output signal of the Interrupt System Enable Flip-Flop is applied to gate MC86B and also to pin 10 of the I/O control card as the IEN6 (Interrupt Enable, Select Code 06) signal. Pin 10 sends this signal to the interface cards which have select codes 05 and 06, and back into the I/O control card at pin 5, where it is applied to gate MC17B.

3-332. The power fail interrupt card uses select code 04, which has the highest priority in the interrupt system. The power fail card generates the PRH5/PRL4 (Priority High Select Code 5/Priority Low Select Code 4) signal when the ac line voltage fails or becomes abnormally low. This signal is applied to the two interface card slots using select code 05. These two slots are reserved for the Memory Protect and Parity Error options. If neither of these options is installed, jumper W3 is in place and the PRH5/PRL4 signal bypasses nonexistent circuit cards A15 and A16. Regardless of whether these options are installed, the PRL6 signal is applied to DMA control card A4. The output of card A4, PRH10/PRL7, is forwarded to I/O interface card A203 and to gates A201MC47A and A201MC86B. If DMA control card A4 is not installed, it is bypassed by jumper W2.

3-333. When the Interrupt System Enable Flip-Flop is set, the IEN10 signal is true provided no priority 4, 5, 6, or 7 interrupt is in progress. The true IEN10 signal allows I/O interface cards A203 through A210 to initiate an interrupt. When a card in this group does produce an interrupt, its PRH/PRL output becomes false and all cards of lower priority are temporarily disabled. That is, they cannot produce an interrupt. The PRH/PRL output of each disabled card is false.

3-334. When no interrupt with priority 4 through 17 is in progress, and the Interrupt System Enable Flip-Flop is set, the PRH20/PRL17 signal is true. As a result, gate A201MC17B furnishes a true IEN20 signal. This signal permits I/O interface cards A211 through A218 to initiate an interrupt. When a card in this group produces an interrupt, its PRH/PRL output becomes false and all cards of lower priority are disabled. The PRH/PRL output of each disabled card is false.

3-335. The interrupt control system is extended to include I/O interface cards in the I/O extender, if used. Cards in the extender can produce an interrupt only when no interrupt is in progress in the main frame.

3-336. Interrupt System Disable. To disable the interrupt system, the Interrupt System Enable Flip-Flop is reset by a CLF instruction having a select code of 00. When the instruction is performed, the SCM0 and SCL0 signals are applied to gate MC67C. Since the CLF instruction is an I/O instruction, IOGE becomes true, and about 70 nanoseconds later the output of gate MC57A (signal IOGE(B)) is true. All inputs to MC67C are then true, and the true output of this gate is applied to gate MC67B. This gate resets the Interrupt System Enable Flip-Flop. The IEN6, IEN10, and IEN20 signals then become false, and the only circuit cards which can produce a program interrupt are power fail interrupt card A6, parity error card A15, and memory protect card A16. No I/O device, including the DMA system, can produce an interrupt.

3-337. FLAG SKIP INSTRUCTIONS. Through the use of the SFS (Skip if Flag Set) and SFC (Skip if Flag Clear) instructions, a program skip is produced when the Interrupt System Enable Flip-Flop is set (SFS) or clear (SFC). When an SFS instruction with a select code of 00 is performed and the flip-flop is set all inputs to gate MC97A are true. A true SKF signal is then sent to the control section, resulting in a program skip. If the Interrupt System Enable Flip-Flop is in the clear state when the instruction is performed, no skip takes place.

3-338. When an SFC instruction with select code 00 is performed, and the flip-flop is clear, all inputs to gate MC97B are again true. The SKF signal is again true, and a skip takes place. If the flip-flop is set, SKF remains false and no skip occurs.

3-339. I/O ADDRESS CARD.

3-340. The I/O address card has three functions. First, it decodes the 6-bit select code of instructions of the input/output group. Secondly, the I/O address card encodes the Flag and IRQ signals from the various I/O interface cards to provide a 6-bit I/O address and an Interrupt signal. The third function of the circuit card is to store the I/O address of the last I/O device that interrupted the computer program; this address can be utilized by certain program instructions.

3-341. A logic diagram of the I/O address card is furnished in figure 7-20. Unless otherwise stated, all circuit elements in the following discussion are situated on this circuit card. During the course of the discussion, reference should be made to the logic diagram as required.

3-342. DECODING FUNCTION. When an instruction is read from the memory section, the instruction word is placed in the T-register. If the instruction is of the I/O type, T-register bits 5 through 0 contain the select code portion of the instruction. These six bits, and the "not" equivalent of each, are furnished to the I/O address card, where they are decoded. In instructions which are not of the I/O type the same six bits are decoded, but no use is made of the decoded output.

3-343. The decoding gates on the I/O address card are in two groups. One group decodes the three most significant bits of the select code to furnish one true signal in the

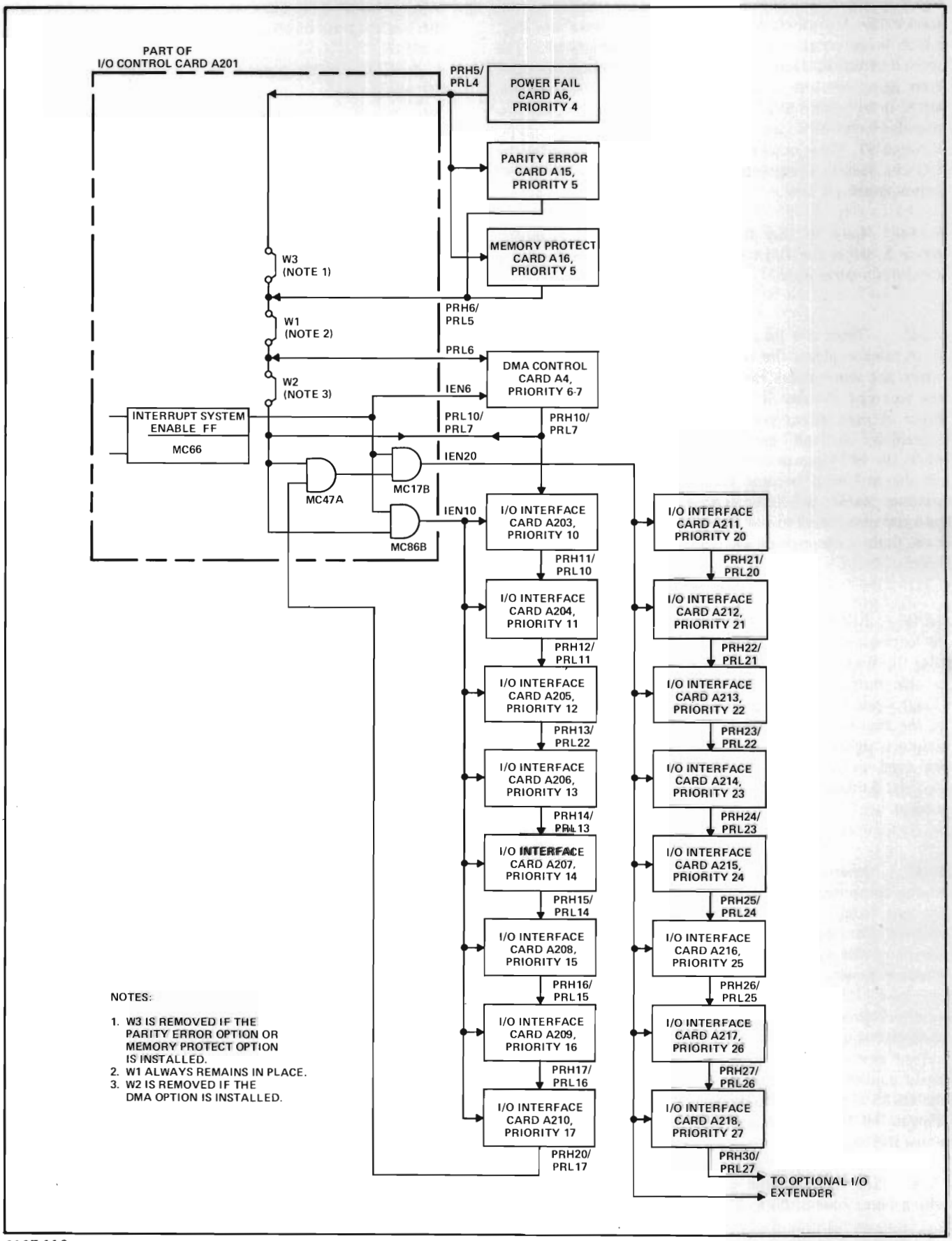

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Figure 3-26. Interrupt Priority Circuits

signal group SCM6 through SCM0. (Signal SCM7 is not used.) The fourth character in the signal name is a digit which is the octal equivalent of the three binary bits. The second group of decoding gates similarly decode the three least significant bits of the select code, to provide one true signal in the group SCL7 through SCL0. Together, the two decoded octal digits form an octal number ranging from 00 through 67. These octal numbers provide addressing for the I/O channels in the computer, as well as those in an I/O extender unit, if used.

3-344. Gate MC16A disables the decoding gates during phase 5, when the DMA system rather than the T-register furnishes a select code.

3-345. Table 3-9 lists the various select codes in octal form, and explains the functions of all instructions with which the select codes can be used. Included in the table is the name of the circuit card which decodes the two octal digits of each select code. This decoding process is performed by an "and" gate, which experiences coincidence when the SCM signal and the SCL signal furnished to the circuit card both become true. In the case of some I/O interface cards, two select codes can be decoded by the card, corresponding to the high and low select codes for the card. Certain other cards also can recognize more than one select code.

3-346. ENCODING FUNCTION. When an input/output device requests an interrupt of the computer program, the IRQ flip-flop on the interface card for the device is set. The set-side output of the IRQ flip-flop applies a true FLG (Flag) signal to the I/O Address card; the reset-side output of the flip-flop is inverted to apply a true IRQ (Interrupt Request) signal to the I/O Address card. These two signals are used to form the Interrupt signal and the Service Request Address to be transferred to the computer control section.

3-347. Interrupt Signal. An Interrupt (INT) signal is sent to the computer at time T5 when a Flag (FLG) signal is received from an interface card and if the ESR signal is received from the I/O control card. The INT signal causes the computer to enter phase 4 at the end of the current machine phase.

3-348. Four Flag signals (FLG 0 through FLG 3) can be received from the interface cards. These signals are described in steps "a" through "d" below. Receipt of a Flag signal applies a true input to gate MC16B through one of the CR33 through CR36 diodes. If the ESR signal is true, the gate MC16B output is applied to the control section as a true INT signal.

a. FLG 0. This input is true when an interface card with a select code of 05 to 17 is requesting an interrupt.

b. FLG 1. This input is true when an interface card with a select code of 20 to 37 is requesting an interrupt.

c. FLG 2. This input is true when an interface card with a select code of 40 to 57 is requesting an interrupt.

d. FLG 3. This input is true when an interface card with a select code of 60 to 67 is requesting an interrupt.

3-349. Service-Request Address. The 6-bit service-request address is the select code of the interface card requesting an interrupt. It is sent to the M-register via the T-bus and specifies the interrupt location for that device in memory. (The interrupt location contains the instruction to be executed after the interrupt occurs.) While the Interrupt signal is sent to the control section at time T5 of the current machine phase, the service request address is not furnished to the computer until time T7 of Phase 4.

3-350. The service-request address is formed by encoding the combination of Flag and IRQ signals from the interface card requesting an interrupt. The FLG 0 signal is used to generate the INT signal when select codes 05 through 17 request an interrupt. The FLG 1 through FLG 3 signals generate the INT signal for select codes 20 through 70 and determine the two most significant bits (bits 4 and 5) of the address. These signals are applied to diodes CR37 through CR40 and then to gates MC17A and MC17B. The IRQ signals determine the four least significant bits (bits 0 through 3) of the address and are applied to diodes CR1 through CR32 and then to gates MC26A, MC26B, MC27A, and MC27B. The remaining input to the service-request address gates is applied to time T7 of Phase 4 by the RSM 6-9 signal. The Flag and IRQ signals received from various interface cards and their select codes are indicated by table 3-10. This table also indicates the I/O address card components these signals are applied to in obtaining the 6-bit service-request address.

3-351. Run Signal. The "not" RF2 (Run Flip-Flop 2) signal is applied to gate MC67A. When the computer is running the "not" RF2 signal is false. When the computer is in a HALT condition the "not" RF2 signal is true. MC67A inverts the "not" RF2 signal and applies it to gate MC57A. Since the two input pins (pin 2 and 14) of MC57A are tied together, it produces a true output signal whenever it receives a true input from gate MC67A (whenever the computer is in the RUN mode). This signal is sent out of the I/O address card as the RUN signal and is applied to pin 50 of all I/O interface-card slots (select codes 10 through 27). If an I/O extender is used, the RUN signal is also applied to pin 50 of all interface card slots in the extender.

3-352. CENTRAL INTERRUPT REGISTER. The central interrupt register (Flip-Flops CIF0 through CIF5 and gates MC15A, MC15B, MC36A, MC36B, MC46A, and MC46B) stores the Service Request Address. This information, or address, is always available during a Phase 4 I/O operation and is strobed into the Central Interrupt Flip-Flops, CIF0 through CIF5, at T7 of Phase 4. To utilize this address, the computer must execute an I/O load or merge

Table 3-9. Select Code Functions

SELECT CODE	INSTRUCTION	CIRCUIT CARD ON WHICH SELECT CODE IS DECODED	FUNCTION
00	CLF, STF	I/O control card A201	Turn the interrupt system off (CLF) or on (STF). The power failure interrupt circuits are not affected. The parity error or memory protect interrupt circuits are likewise not affected if these options are installed.
00	SFC, SFS	I/O control card A201	Skip the next instruction if the interrupt system is off (SFC) or on (SFS).
01	LIA/B	I/O control card A201	Load the contents of the switch register into the A-register or B-register.
01	MIA/B	I/O control card A201	Merge (combine by inclusive "or") the contents of the switch register with the contents of the A-register or B-register.
01	CLO, STO	I/O control card A201	Clear (CLO) or set (STO) the Overflow Flip-Flop.
01	SOC, SOS	I/O control card A201	Skip the next instruction if the Overflow Flip Flop is clear (SOC) or set (SOS). Also, clear the Overflow Flip-Flop if the hold/clear bit (bit 9) of the instruction word is logic 1.
02	CLC	DMA register card A1	Prepare the DMA channel 1 memory address register to receive a DMA type 2 control word.
02	STC	DMA register card A1	Prepare the DMA channel 1 word-count register to receive a DMA type 3 control word.
02	OTA/B	DMA register card A1	Transfer a DMA type 2 or type 3 control word from the A-register or B-register to the DMA channel 1 system.
03	CLC	DMA register card A2	Prepare the DMA channel 2 memory address register to receive a DMA type 2 control word.
03	STC	DMA register card A2	Prepare the DMA channel 2 word-count register to receive a DMA type 3 control word.
03	OTA/B	DMA register card A2	Transfer a DMA type 2 or type 3 control word from the A-register or B-register to the DMA channel 2 system.
04	SFC	Power-failure auto-restart card A6*	If the Restart Control Flip-Flop on card A6 is clear, this instruction and select code cause a program skip when performed after a power failure interrupt. A skip does not take place when this instruction is performed after a power-on interrupt.
04	CLC	Power-failure auto-restart card A6*	This instruction and select code are used to set the Restart Control Flip-Flop on card A6 after power fails. As a result, if the power failure is only momentary a return is made to the main program. The maximum duration of the momentary failure depends on the amount of time before the POFP pulse is furnished to indicate the start of dc shut-down. The delay between the power fail interrupt and the POFP pulse is 1 to 12 milliseconds, depending on the amount of loading imposed on the dc power supplies by optional devices.
04	STC	Power-failure auto-restart card A6*	Clear the Flag Flip-Flop on card A6. A power failure can then initiate an interrupt by setting the flip-flop. The instruction also clears the Restart Control Flip-Flop on card A6 if the hold/clear bit (bit 9) of the instruction word is logic 1.
04	CLF	Power-failure auto-restart card A6*	This instruction and select code are used to clear the Restart Control Flip-Flop on card A6 after restoration of ac power. As a result, an SFC instruction with select code 04 causes a program skip when performed after a subsequent power fail interrupt. This instruction does not affect the Flag Flip-Flop on card A6.
04	HLT	Power-failure auto-restart card A6*	When the hold/clear bit (bit 9) of the instruction word is logic 1, this instruction and select code clears the Restart Control Flip-Flop on card A6. The program is also stopped. The Flag Flip-Flop on card A6 is not affected.
05	CLF, STF	Parity error card A15	Turn the parity error detection system off (CLF) or on (STF).
05	CLC	Parity error card A15	Turn the parity error detection system off if the hold/clear bit (bit 9) of the instruction word is logic 1.

Table 3-9. Select Code Functions (Continued)

SELECT CODE	INSTRUCTION	CIRCUIT CARD ON WHICH SELECT CODE IS DECODED	FUNCTION
05	STC	Memory protect card A16 Parity error card A15	Turn on the memory protect system. The system is turned off each time an interrupt occurs. It is also turned off when the PRESET push-switch is pressed (provided the computer is not running), and during power turn-on. If the hold/clear bit (bit 9) of the STC instruction is logic 1, the parity error system detection system is turned off.
05	OTA/B	Memory protect card A16	Load the Fence register with the contents of the A-register or B-register, specifying the lowest unprotected address.
05	LIA/B	Memory protect card A16	Load the contents of the Violation register into the A-register or B-register. The Violation register contains an address that has been illegally referenced.
06	CLC,STC	DMA control card A4	Clear (CLC) or set (STC) the Control Flip-Flop for DMA channel 1. Also, if the hold/clear bit (bit 9) of the instruction word is logic 1, the DMA channel 1 Flag Flip-Flop is cleared.
06	CLF,STF	DMA control card A4	Clear (CLF) or set (STF) the DMA channel 1 Flag Flip-Flop.
06	SFC,SFS	DMA control card A4	This instruction and select code cause a program skip if DMA channel 1 Flag Flip-Flop is clear (SFC) or set (SFS).
06	OTA/B	DMA control card A4	Transfer the contents of the A-register or B-register to DMA channel 1 system. The A-register or B-register contains a type 1 DMA control word.
07	CLC,STC	DMA control card A4	Clear (CLC) or set (STC) the Control Flip-Flop for DMA channel 2. Also, if the hold/clear bit (bit 9) of the instruction word is logic 1, the DMA channel 1 Flag Flip-Flop is cleared.
07	CLF,STF	DMA control card A4	Clear (CLF) or set (STF) the DMA channel 2 Flag Flip-Flop.
07	SFC,SFS	DMA control card A4	This instruction and select code cause a program skip if DMA channel 2 Flag Flip-Flop is clear (SFC) or set (SFS).
07	OTA/B	DMA control card A4	Transfer the contents of the A-register or B-register to DMA channel 2 system. The A-register or B-register contains a type 1 DMA control word.
10 through 67 (octal)	STC,CLC	I/O interface card**	Set (STC) or clear (CLC) the Control Flip-Flop on the designated I/O interface card. Also, if the hold/clear bit (bit 9) of either instruction word is logic 1, clear the Flag Flip-Flop on the I/O interface card.
10 through 67 (octal)	STF,CLF	I/O interface card**	Set (STF) or clear (CLF) the Flag Flip-Flop on the designated I/O interface card.
10 through 67 (octal)	SFS,SFC	I/O interface card**	Skip if the Flag Flip-Flop on the designated interface card is set (SFS) or clear (SFC).
10 through 67 (octal)	OTA/B	I/O interface card**	Transfer the contents of the A-register or B-register to the designated I/O interface card. Also, if the hold/clear bit (bit 9) of the instruction word is logic 1, clear the Flag Flip-Flop on the I/O interface card.
10 through 67 (octal)	LIA/B	I/O interface card**	Transfer a 16-bit word from the designated I/O interface card to the A-register or B-register. Also, if the hold/clear bit (bit 9) of the instruction word is logic 1, clear the Flag Flip-Flop on the I/O interface card.
10 through 67 (octal)	MIA/B	I/O interface card**	Merge (combine by exclusive "or") a 16-bit word from the designated I/O interface card with the contents of the A-register or B-register. Also, if the hold/clear bit (bit 9) of the instruction word is logic 1, clear the Flag Flip-Flop on the I/O interface card.
10 through 67 (octal)	HLT	I/O interface card**	Halt the program and, if the hold/clear bit (bit 9) of the instruction word is logic 1, clear the Flag Flip-Flop on the designated I/O interface card.

NOTES:

*If the power-failure auto-restart option is not installed, these instructions produce no effect.

**The particular I/O interface card is designated by the select code (see figure 7-2, card slots 203 through 218). If the select code is greater than 27/30, the I/O interface card is in the optional I/O extender.

Table 3-10. I/O Address Card Encoding Examples

INTERFACE CARD SELECT CODE (OCTAL)	FLAG SIGNAL IS APPLIED			IRQ SIGNAL IS APPLIED			FOR A SERVICE REQ. ADDRESS OF (BINARY)
	FLAG SIGNAL	TO DIODE(S)	THEN TO GATE(S)	IRQ SIGNAL	TO DIODE(S)	TO GATE(S)	
07	0	–	–	7	CR28,CR20,CR12	MC27B,MC27A, MC26B	000 111
10	0	–	–	10	CR1	MC26A	001 000
21	1	CR38	MC17B	1	CR25	MC27B	010 001
32	1	CR38	MC17B	12	CR21,CR3	MC27A,MC26A	011 010
43	2	CR39	MC17A	3	CR26,CR18	MC27B,MC27A	100 011
54	2	CR39	MC17A	14	CR13,CR5	MC26B,MC26A	101 100
65	3	CR37,CR40	MC17B,MC17A	5	CR27,CR10	MC27B,MC26B	110 101
76	3	CR37,CR40	MC17B,MC17A	16	CR23,CR15,CR7	MC27A,MC26B, MC26A	111 110

instruction containing select code 04. These instructions would be LIA/B and MIA/B used with select code 04. Select code 04, the Power Fail Interrupt Select Code, is not required for any power fail interrupt function during a load instruction so has been used here. On the I/O address card, the Phase 4, T7 signal enables gate MC37A which then applies its true output to all flip-flops of the register (CIF0 through CIF5). This action causes the address to be written into the register flip-flops. In order to then apply this address to the computer central processor, the IOGE(B) signal and both select code signals (representing select code 04) must be applied to gate MC37C. The output of gate MC37C is then applied to gate MC37B simultaneously with the IOI signal. When all of these signals are presented, (having been generated by a computer program instruction of the type mentioned above) the output of gate MC37B is applied to all of the central interrupt register output gates (MC15A, MC15B, MC36A, MC36B, MC46A, and MC46B). This action enables all output gates of the register and the address that it contains is applied to the IOBI bus of the computer central processor.

3-353. RESISTANCE LOAD CARD.

3-354. The resistance load card (figure 7-21) contains pull-down resistors for certain signals (furnished to the I/O interface card slots. The resistors serve to increase the fall-time of the signals and to reduce electrical noise. If all I/O interface card slots contain I/O interface cards, the loading effect of the cards eliminates the need for the resistance load card.

3-355. The resistance load card does not contain interrupt priority circuits or jumpers. Therefore, it cannot be inserted in a card slot with a number lower than that of a slot containing an I/O interface card. If it is, the interrupt system will not function properly.

3-356. DETAILED THEORY, POWER SUPPLY SECTION.

3-357. The following paragraphs explain the circuit theory of the various power supplies in the computer. The discussion is followed by an explanation of the power supply turn-on and shut-down sequence.

3-358. POWER SUPPLY CIRCUIT THEORY.

3-359. +4.5 VOLT AND -2 VOLT POWER SUPPLIES. The +4.5 and -2 volt supplies provide operating voltages for the logic circuits. Descriptions are given below.

3-360. +4.5 and -2 Volt Power Sources. Figure 3-27 is a schematic diagram of the +4.5 volt and -2 volt power sources. Included in the diagram is a portion of the regulator for each of these two voltages.

3-361. Both power sources use a single tapped secondary winding of transformer A311T1. The +4.5 volt power source consists of the center portion of the winding, diodes CR1 and CR2, capacitors C5, C6, A303C14, A303C15, and A303C16, and resistors A303R26 and A310R23. Fuses F12 and F13 provide overload protection.

3-362. Silicon diodes CR1 and CR2 form a full-wave rectifier, providing approximately 7.9 volts dc which is filtered by A303C14 and A303C15. Additional filtering is provided by A303C16. Capacitors C5 and C6 bypass rf noise spikes produced each ac cycle when diode conduction stops. Resistor A303R26 discharges the filter capacitors when power is removed from the computer. Resistor A310R23 provides a minimum load for the +4.5 volt power supply, and discharges bypass capacitor A310C16.

3-363. The -2 volt power source uses the entirety of each half of the secondary winding shown in figure 3-27. Silicon diodes CR3 and CR4 form a full-wave rectifier, with capacitors C4 and C7 serving to bypass voltage spikes. Capacitors A303C17 and A303C18 are filter capacitors, and resistor A303R27 discharges these two capacitors when power is removed. Additional filtering is provided by capacitor A303C8. Fuses F11 and F14 provide overload protection.

3-364. The remaining components in figure 3-27 are part of the +4.5 and -2 volt regulators, explained below.

3-365. Schematic Diagram Analysis of +4.5 Volt Voltage Regulator. The +4.5 volt regulator consists of portions of large heat sink assembly A304, a portion of logic supply regulator card A301, resistors A310R8 through A310R11, and resistors A307R45 and A308R17. The circuit is shown in figure 3-28. Included in the diagram are the circuits for +4.5 volt current limiting.

3-366. The voltage regulator is of the series type. By varying the voltage drop across transistors Q1, Q2, Q3, and Q4, the regulator maintains a fixed voltage across the +4.5 volt computer load. When fully loaded, the +4.5 volt regulator and filter capacitors maintain a regulated +4.5 volt output for at least one millisecond after instantaneous removal of the ac line voltage.

3-367. The +4.5 volt sense input to the regulator is applied to the base of transistor Q30. This transistor and Q31 form a differential amplifier, with resistor R66 providing the means for adjusting the level of the regulated +4.5 volts to the required voltage. Resistors R67 and R65 keep the adjustment of the base voltage of Q31 within normal range, and provide for a vernier action in the adjustment of R66.

3-368. If the +4.5 sense voltage rises above normal, conduction through Q30 decreases, conduction through Q31 increases, and the voltage applied to the base of transistor Q32 becomes less negative. As a result, conduction in Q32 decreases, and the voltage at the base of Q10 becomes less negative. The voltage applied to the bases of Q1, Q2, Q3, and Q4 moves in the positive direction, and these transistors conduct less heavily. As a result, the voltage drop across Q1, Q2, Q3, and Q4 increases, and the regulated +4.5 volts returns toward normal.

3-369. If the regulated +4.5 volts decreases in value, the opposite action to that described above takes place.

3-370. Resistors A310R8 through A310R11 serve to equalize the current through the four series regulator transistors. Because of minor differences in these transistors, one will conduct more than the others. If countermeasures are not taken, this transistor will heat up slightly more than the others, conduct more as a result, and thermal runaway will take place, destroying the transistor. Then the transistor which conducts next-most-heavily will destroy itself, and so on. Resistors A310R8 through A310R11 prevent this current hogging. If a transistor conducts more than the others, the increased voltage drop across its emitter transistor opposes the increase in bias current, preventing runaway. Each transistor establishes its own state of balance.

3-371. The regulator circuit requires the following operating voltages: +20, -20, +23.3, +9, and -8 volts. These voltages, used only within the power supply itself, are produced by simple full-wave rectifiers and Zener-diode circuits which require no discussion.

3-372. Schematic Diagram Analysis of +4.5 Volt Current Limiter. Transistor Q33 (figure 3-28) is used to control current limiting. The current limiting circuit also uses some of the components employed for voltage regulation. If an excessive load is imposed on the +4.5 volt power supply, Q33 reduces current flow through Q1, Q2, Q3, and Q4, preventing overheating and damage to components. The reduced current through the load reduces the voltage across the load. The voltage regulating circuits oppose this tendency, but the current limiter over-rides the voltage regulator, and the +4.5 volt supply breaks out of regulation in the downward direction. As a result, dc shut-down takes place.

3-373. Resistor A310R11 is in the ground side of the +4.5 volt circuit. The voltage drop across the resistor is applied to transistor Q33, and if excessive current is drawn from the +4.5 volt source, Q33 conducts heavily. Voltage at the base of Q32 becomes less negative, causing decreased conduction through Q32. The base of Q10 becomes less negative, moving the bases of Q1, Q2, Q3, and Q4 in the positive direction. This results in decreased conduction by Q1, Q2, Q3, and Q4.

3-374. Transistor Q33 functions as an analog circuit, rather than a switching circuit.

3-375. Resistor R69 is the current-limiting adjustment (CLA) resistor. It is set to cause current-limiting at the proper point. If components in the current-limiting circuit are changed, readjustment of R69 may be necessary; however, this adjustment requires special loading and test equipment, and must not be performed in the field. If adjustment is needed, logic supply regulator card A301 must be returned to the factory, where suitable equipment for making the adjustment is available.

3-376. +4.5 Volt Shut-Down. The +4.5 volt power supply is shut down as a result of any of the following:

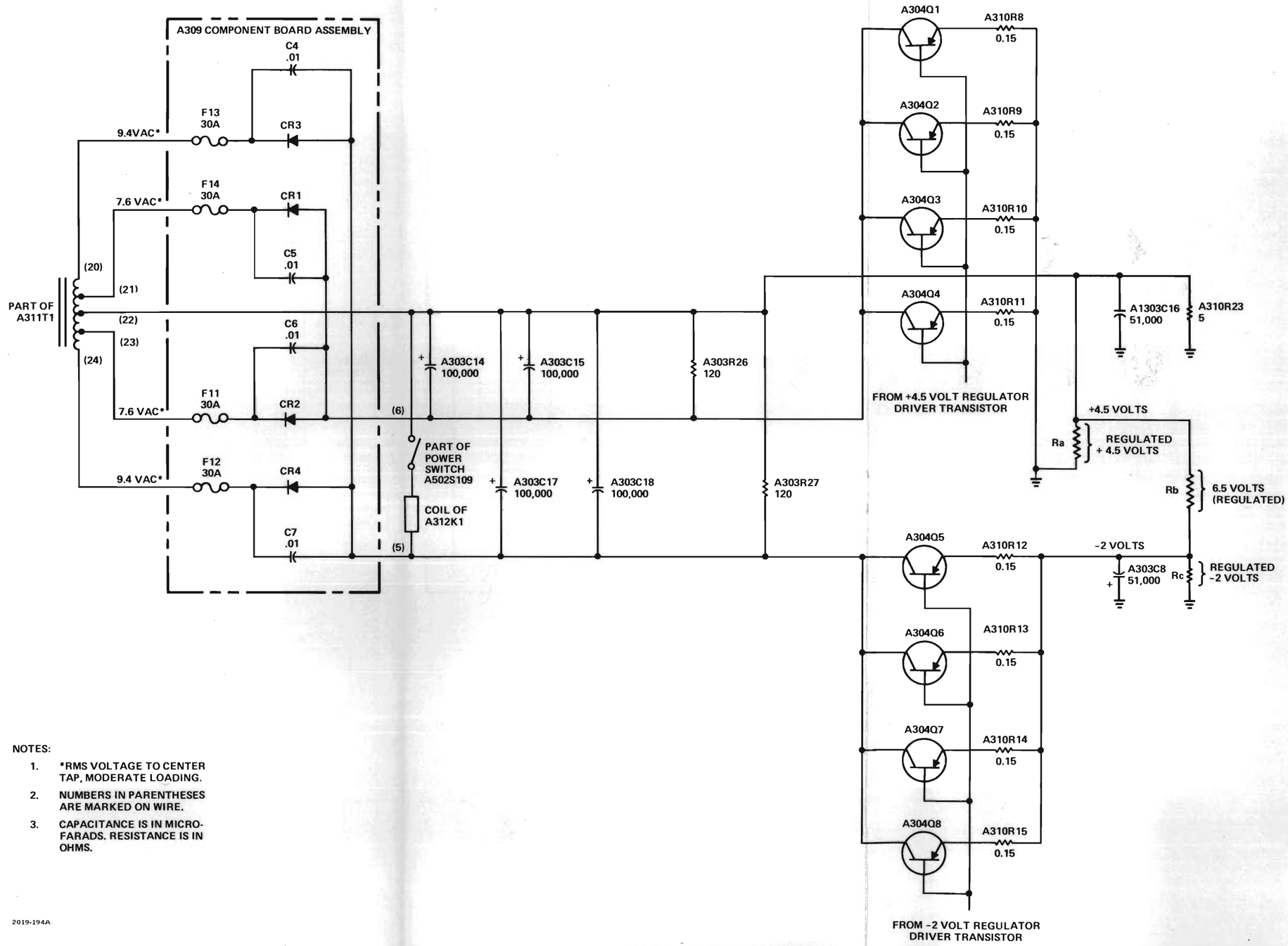
a. The computer has been turned off by means of the POWER switch.

b. Overheating in the computer cabinet or in the 2160A Power Supply Extender (if used) has caused a thermal switch to open.

c. AC line voltage has become zero volts.

d. AC line voltage has become abnormally low.

e. The output of the -2 volt power supply has dropped below normal or become zero volts.



NOTES:

1. *RMS VOLTAGE TO CENTER TAP, MODERATE LOADING.
2. NUMBERS IN PARENTHESES ARE MARKED ON WIRE.
3. CAPACITANCE IS IN MICROFARADS. RESISTANCE IS IN OHMS.

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Figure 3-27. +4.5 Volt and -2 Volt Power Sources, Schematic Diagram

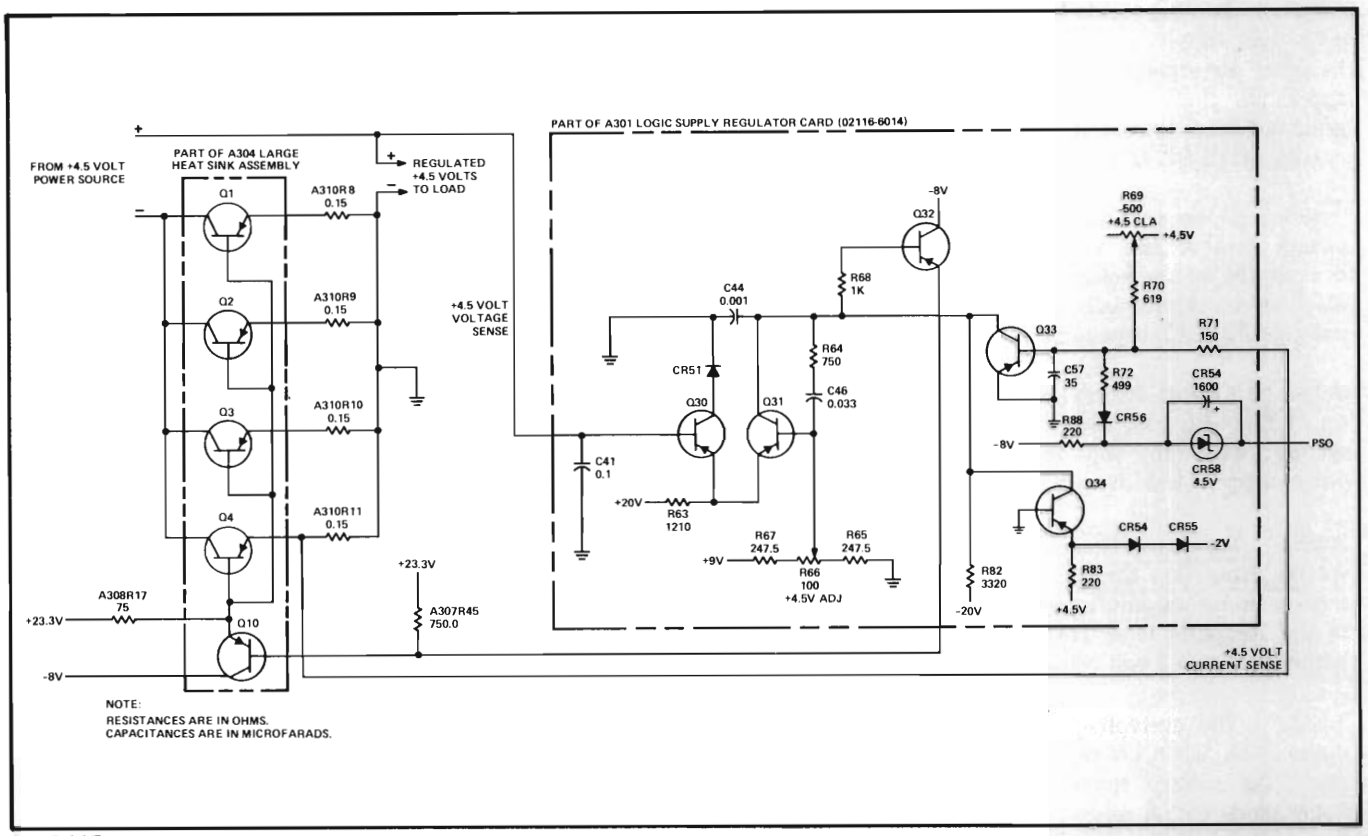

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Figure 3-28. +4.5 Volt Voltage Regulator, Current Limiter, and Shut-Down Circuits, Schematic Diagram

3-377. When shut-down of the +4.5 volt supply occurs, the flow of current through the computer load is stopped by the +4.5 volt current limiter. If the computer has been turned off, or if ac line voltage has lowered or become zero, the +4.5 volt current is cut off before the +4.5 volt filter capacitors have appreciably discharged, after which the capacitors begin to discharge. If shut-down occurs because of reason "b" or "e" above, the +4.5 volt power source continues to function, and the +4.5 volt filter capacitors remain fully charged.

3-378. After dc shut-down resulting from any cause, bypass capacitors on cards in the card cage must discharge before +4.5 volts is completely removed from the computer circuits. About 70 ms is required to discharge these bypass capacitors. (In the case of the +12 volt power supply, several seconds is required if this circuit is only lightly loaded by optional devices.)

3-379. When shut-down occurs because of a fault condition (that is, for any reason other than operation of the POWER switch), the +4.5 volt power is automatically restored if the fault clears. However, a POFP pulse is generated during dc power turn-on. As a result, the program does not restart, and the computer will be in the same state as when power is applied by operating the POWER switch.

3-380. Examining in detail the first two methods of bringing about dc shut-down, if the computer is turned off or if a thermal switch opens the PSO signal becomes false (see figures 3-7 and 3-28). The voltage at the base of transistor Q33 moves in the negative direction, bringing about heavy conduction in Q33. As a result, transistors Q1, Q2, Q3, and Q4 are cut off. When the PSO signal becomes false, power fail interrupt card A6 produces a power fail interrupt, and if programmed to do so the computer stores the contents of registers and performs other functions in preparation for later start-up. (If the computer is in the halt mode when the power fail occurs, the power fail interrupt program will not be performed.)

3-381. The third type of shut-down for the +4.5 volt supply occurs when the ac line voltage drops to zero or becomes abnormally low. First, a power fail interrupt takes place when the line voltage drops below a point which is between 100 and 102 volts rms. (In a 230-volt computer this point is between 200 and 204 volts rms.) The interrupt is produced by power fail interrupt card A6. If the line voltage continues to drop, or if it has become zero volts almost instantly, the various power supply regulators endeavor to maintain their output voltage levels, drawing upon the energy stored in the filter capacitors. A point will be reached when one of the regulators will be unable to maintain its output voltage. The regulator in which this first occurs depends on the loading imposed on each power supply by the various optional devices installed in the computer. If line voltage is still being furnished when a dc voltage drops out of regulation, rectifier ripple will appear on the output of the dc voltage. After the first dc voltage has dropped below its regulated value, other dc voltages are shut down in the manner described later in this section.

3-382. Turning to the last method of shutting down the +4.5 volt supply, if the -2 volt power supply output becomes abnormally low or fails completely, the voltage applied to diode CR55 becomes less negative. As a result, grounded-base transistor Q34 conducts, leading to the cutting off of Q1, Q2, Q3, and Q4.

3-383. When shut-down of the +4.5 volt power supply occurs because the computer has been turned off or because the ac line voltage has become zero, relay A312K1 de-energizes. Abnormally low ac line voltage may also de-energize A312K1, depending on the ac level reached.

3-384. Further information on the shut-down and turn-on of the +4.5 volt power supply is provided later in this section, when the shut-down and turn-on sequence of power supplies is dealt with.

3-385. Schematic Diagram Analysis of +4.5 Volt Overvoltage Protection Circuit. The +4.5 volt overvoltage protection circuit prevents excessive voltage from being applied to the computer load. This high voltage could result from failure of the +4.5 volt voltage regulator.

3-386. The overvoltage protection circuit is shown in figure 3-29. When the regulated +4.5 volts is at its normal value, the voltage across the series circuit consisting of Zener diode CR13, resistor R21, and resistor R22, is insufficient to cause avalanche breakdown in the diode. However, if the voltage rises to between +5 and +8 volts, CR13 enters the breakdown region. The resistance of CR13 decreases, and the voltage drop across R22 increases. As a result, silicon-controlled rectifier Q6 conducts at saturation, placing a low resistance across the computer load and making the voltage across the load about 0.9 volts. The heavy current drawn from the +4.5 volt power supply causes current limiting of the power supply output. (Since the voltage regulator may be defective, the current limiter may also be inoperative. If this is the case, the heavy current will result in a blown fuse.) The loss of +4.5 volts across the computer load leads to shut-down of the other dc voltages.

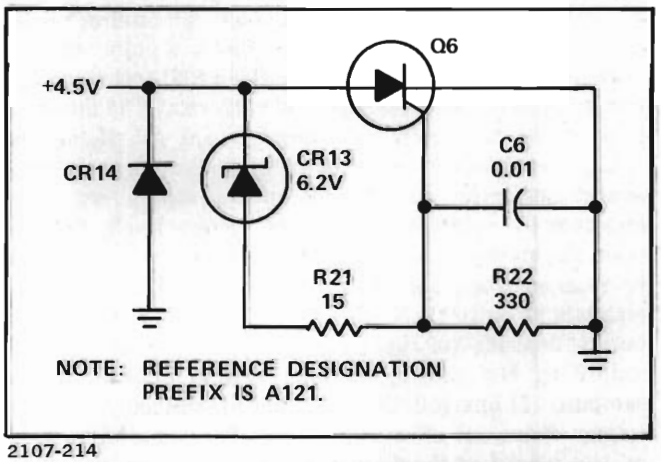

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Figure 3-29. +4.5 Volt Overvoltage Protection Circuit, Schematic Diagram

3-387. Diode CR14 prevents current from flowing in the reverse direction through the +4.5 volt power supply. This might occur when another dc voltage is shorted to +4.5 volts. One of the supplies will force current in the reverse direction through the other supply, the power supply receiving the reverse current depending on the voltage and internal impedance of the two supplies concerned. Diode CR14 provides a low resistance path to protect the +4.5 volt power supply from damage due to this cause.

3-388. Overvoltage protection is provided for all regulated voltages furnished to the computer, with the exception of +32 volts. Table 3-11 lists the voltage required to activate each protection circuit.

Table 3-11. Overvoltage Limits

NOMINAL REGULATED VOLTAGE	VOLTAGES THAT ACTIVATE THE OVERVOLTAGE PROTECTION CIRCUITS
+4.5	+5.0 To +8.0
-2.0	-2.5 To -8.0
+12.0	+13.0 To +18.0
-12.0	-13.0 To -18.0
+20.0	+25.6 To +31.4
-20.0	-25.6 To -31.4

3-389. Schematic Diagram Analysis of Voltage Regulator, Current Limiter, and Overvoltage Protection Circuit for -2 Volts. The voltage regulator, current limiter, and overvoltage protection circuit for the -2 volt power supply are similar to those used for +4.5 volts, and therefore require no additional circuit theory discussion. When fully loaded, the -2 volt regulator and filter capacitors maintain a regulated -2 volt output for at least one millisecond after instantaneous drop of the ac line voltage to zero volts.

3-390. +12, -12, +20, AND -20 VOLT POWER SUPPLIES. The +12, -12, +20, and -20 volt power supplies closely resemble the +4.5 and -2 volt supplies. Therefore, no circuit-theory discussion is furnished for these supplies. It must be pointed out, however, that the +20 and -20 volt outputs vary in accordance with the air temperature near the core stack circuit cards. The change in voltage counteracts the change in core stack operation which results from the temperature variation. The circuits for bringing about the voltage change are shown in figures 7-34 and 7-38. Resistor A100R220 in figure 7-38 is a thermal sensing resistor situated at the top of the card cage. Its resistance varies in accordance with the air temperature at that point; as a result the voltage furnished to the base of transistor A302Q54A changes as the air temperature changes. This leads to a variation in the output voltage of +20 volt regulator. One destination of this voltage is resistor A302R158, which is in the -20 volt regulator circuit. The changes in

+20 volts bring about like changes in the -20 volt output. The variation in these voltages affects the operation of the X-Y driver switch cards and the inhibit driver cards to reduce the effects of temperature change on core stack operation.

3-391. Table 5-4 shows the variation in the +20 and -20 volt outputs as temperature changes.

3-392. As with the +4.5 volt and -2 volt supplies, the +12, -12, +20 and -20 volt power supplies maintain a normal regulated output voltage for at least one millisecond after instantaneous removal of ac line voltage.

3-393. +35 VOLT SUPPLY. The +35 volt power supply (figure 7-34) furnishes filtered unregulated dc to the I/O interface cards. The rectifiers are CR15 and CR16. Another power supply, using the bridge rectifier composed of CR23, CR24, CR25 and CR26, furnishes +50 volts which is connected in series with the +35 volt supply to furnish +85 volts for use within the power supply.

3-394. +32 VOLT SUPPLY. A Zener diode circuit on memory supply regulator card A302 produces regulated +32 volts. This voltage is used by logic supply regulator card A301 and by power-failure auto-restart card A6.

3-395. +7 VOLT SUPPLY. The +7 volt supply uses the bridge rectifier comprised of diodes CR31, CR32, CR33, and CR34 (figure 7-34). The resulting unfiltered voltage is used for lighting lamps on the door assembly. The lamps are turned on and off by driver transistors in series with the lamp filaments.

3-396. POWER TURN-ON AND SHUT-DOWN.

3-397. The six regulated voltages used by the logic and memory circuits are applied to and removed from the computer load circuits in a controlled sequence. These voltages are -2, +4.5, +12, -12, +20 and -20 volts. Two further outputs are provided by the power supply; these are +7 volts unregulated and +35 volts unregulated. Neither of these voltages enters in the turn-on or shut-down sequence. Additional subsidiary voltages are produced for use within the power supply section itself. Like +7 volts and +35 volts, these do not enter into the controlled turn-on or shut-down sequence.

3-398. When the POWER switch is turned on, the six controlled voltages are applied to their respective loads in a predetermined sequence. Similarly, when the computer is turned off the controlled voltages are shut down in an orderly manner. In the event of failure of some of the controlled voltages, certain other voltages are shut down. If a thermal switch opens, all controlled voltages are removed in the same sequence as when the POWER switch is turned off.

3-399. The turn-on or shut-down of the six controlled voltages is accomplished by making the series regulator transistors for each voltage conduct or cut off. In the case of the +4.5 volt power supply, the series regulator transistors are in the ground return to the power source (figures 3-27 and 3-28, A304Q1 through A304Q4), and it is here that the voltage source is connected to or cut off from the computer load. The series regulator transistors for the remaining five controlled voltages are in the ungrounded (high potential) side of the applicable power supply output.

3-400. TURN-ON SEQUENCE. The power supply turn-on sequence is illustrated by graphs in figures 4-105 through 4-108 in Section IV. When the POWER switch is turned on, the first voltage furnished at full level to the computer load is -2 volts. This voltage is followed by +4.5 volts. Other voltages are furnished in the sequence indicated.

3-401. The waveforms shown in figures 4-106 and 4-107 are for computer turn-on with filter capacitors initially discharged. When power is turned off, the series regulator transistors cut off each power supply from its load, and several minutes is required to fully discharge the filter capacitors. Therefore, if the computer is turned on after being off for only a brief time, the waveforms differ somewhat from those shown, and the time required for each voltage to reach operating level is shorter. Further, the waveforms illustrated are for power supplies which are loaded to their maximum capability. With lighter loading, waveforms and timing will differ from those shown, both for turn-on and shut-down.

3-402. The turn-on sequence is determined by the connections between the control circuits for each power supply. This is illustrated in figure 3-30. Each block in the figure represents the power supply named. Before it can furnish an output, every power supply except that for -2 volts and +32 volts must receive the output voltage furnished by the power supply shown to its left. The +12 volt supply requires an input from both the +32 and -12 volt supplies.

3-403. -2 and +4.5 Volt Turn-On. When the POWER switch is turned on, the various subsidiary voltages in the power supply section become available as soon as their filter capacitors charge. The filter capacitors for -2 and +4.5 volts also start to charge (figure 7-34). The series regulator transistors for -2 volts (A304Q5 through A304Q8) begin to conduct, as do the corresponding transistors for +4.5 volts (A304Q1 through A304Q4).

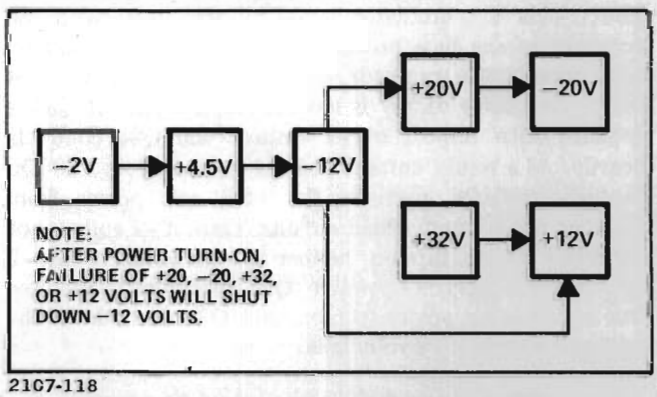


Figure 3-30. Power Supply Interdependence

3-404. The -8 volt power source produces 12.5 volts, from which 4.5 volts normally is subtracted as a result of the series-opposing connection between the +4.5 and -8 volt power supplies. At first, however, while the +4.5 volt bus is near ground potential, the -8 volt output rises toward -12.5 volts as the -8 volt filter capacitor charges. This voltage is applied to resistor R88 on logic supply regulator card A301 (figure 7-34). At this time the PSO signal is not furnished because +4.5 volts is not being supplied to power fail interrupt card A6, which generates PSO. Current flows through resistor R88 and through transistor Q5 on card A6 (figure 7-5), to the +4.5 volt bus, which is near ground potential. The current through resistor R88 begins to charge capacitor C54. As it charges, the capacitor bypasses current around Zener diode CR58, preventing the diode from entering avalanche breakdown.

3-405. The potential at the anode of CR58 is negative as C54 commences to charge from the -8 volt source. This negative voltage is applied to the bases of transistors Q33 and Q38. Diodes CR56 and CR57, together with associated resistors, form an encoding gate (paragraph A-27). This gate allows application of the potential at the anode of CR58 to Q33 and Q38, while preventing shorting together the -2 volt and +4.5 volt current sense voltages.

3-406. As the output from the -8 volt supply increases, the rising negative potential at the bases of Q33 and Q38 causes these transistors to conduct, bringing about current limiting in the series regulator transistors for +4.5 and -2 volts. As a result, the +4.5 and -2 volt outputs are reduced in amplitude after rising for about 20 milliseconds (figure 4-105). Capacitor C54 continues to charge, and a point is reached at which the voltage across C54 is sufficient to permit zener diode CR58 to break into avalanche conduction. The bases of Q33 and Q38 become less negative, current limiting ceases, and the filter and bypass capacitors at the outputs of the +4.5 and -2 volt series regulator transistors begin to charge again. The output filter capacitor for +4.5 volts is A303C16, and that the -2 volts is A303C8. The bypass capacitors for these voltages are situated on various circuit cards in the card cage. When these filter and bypass capacitors are completely charged, the full +4.5 and -2 volts are applied to the computer load circuits.

3-407. The -2 volt output is applied through diodes CR55 and CR54 to the emitter of transistor Q34 on card A301. This is a grounded-base PNP transistor, with the potential of the base positive with respect to the emitter; consequently, the transistor normally is cut off. However, if the 2-volt power supply is inoperative, the base of Q34 is negative with respect to its emitter and Q34 conducts heavily. As a result, current limiting in transistors A304Q5 through A304Q8 prevents the +4.5 volt power from reaching the computer load circuits. Thus, if -2 volts is not furnished during turn-on, neither is +4.5 volts. If the -2 volt power supply is operative, Q34 continues to monitor this source after power turn-on, and Q34 shuts down the +4.5 volt supply if -2 volts fails.

3-408. When +4.5 volts rises to its full potential after turn-on, the PSO signal from card A6 also rises to +4.5 volts. At this time the 4.5 volt drop across CR58 results in a potential at the bases of Q33 and Q38 which keeps these transistors cut off. As a result, current limiting does not take place. However, if a thermal switch is open during power turn-on, the PSO signal is false (figure 3-7). With PSO false, the 4.5 volt drop across CR58 results in a negative potential at the bases of Q33 and Q38 (relative to the emitter of each transistor), and the current limiting which occurs during turn-on remains in effect. Consequently, +4.5 and -2 volts are not applied to the computer load circuits.

3-409. -12, +20, -20, and +12 Volt Turn-On. The controlling elements in the turn-on process for -12, +20, -20, and +12 volts are gates MC1B and MC1A on logic supply regulator card A301 (figure 7-34). Gate MC1A monitors the six controlled voltages during computer operation. If all voltages are normal, and +32 volts also is normal, the gate experiences coincidence and its true output keeps transistor Q43 cut off. If one of the voltages fails, Q43 conducts and brings about shut-down of -12 volts. When -12 volts is shut down, the +20, -20, and +12 volt supplies also are shut down (figure 3-30). Shut-down is brought about by cutting off the series regulator transistor for the voltage concerned.

3-410. During turn-on, a means must be provided for bypassing this voltage monitoring system until all power supplies are operative. Gate MC1B performs this function. When +4.5 volts is available, capacitor C56 starts to charge. While it is charging, the output of MC1B is true and Q43 is cut off. The capacitor becomes substantially charged in about 0.3 second. At this time the output of MC1B becomes false, and MC1A must then furnish a true output in order to prevent shut-down. The output of gate MC1A is true if all six controlled voltages, and +32 volts, are all available.

3-411. The seven voltages monitored by gate MC1A are furnished to the gate in the following manner:

a. +4.5 volts is furnished to one end of resistor R113, the other end of which is connected to the gate.

b. -2 volts affects the gate by shutting down the +4.5 volt supply if -2 volt failure occurs.

c. +12 volts is furnished through two resistors and a Zener dropping diode to pin 1 of the gate, with diode CR63 functioning as a clamp.

d. -12 volts affects the gate by shutting down the +12 volt supply if -12 volt failure occurs.

e. -20 volts affects the gate by keeping transistor Q44 cut off, thereby permitting the application of +4.5 volts through resistor R113 without significant drop in voltage.

f. +20 volts affects the gate by shutting down the -20 volt supply if +20 volts fails.

g. +32 volts is furnished through two resistors and a Zener dropping diode to pin 14 of the gate, with diode CR62 functioning as a clamp.

3-412. When power turn-on takes place, the -12 volt output starts to rise. However, Q43 on card A301 begins to conduct as various filter capacitors charge, and current limiting takes place for -12 volts. As a result, the voltage across the -12 volt load returns toward zero (figure 4-106). Then, when the +4.5 volt output is available, gate MC1B cuts off Q43, and -12 volts again commences to increase. The series regulator transistor for this voltage functions as a constant current source, and the voltage rise is almost linear as filter and bypass capacitors charge from the regulator output. The filter capacitor is A303C10, and the bypass capacitors are installed on various circuit cards in the card cage.

3-413. The -12 volt output is applied to the +20 volt regulator through temperature sensing resistor A100R220. When -12 volts starts to rise, the +20 volt output also commences to rise. Because of the differing loads for the -12 and +20 volt supplies, and the different amounts of capacitance requiring charging, the two voltages rise at different rates. The final level of the +20 volt output is determined by the temperature near the core stacks.

3-414. The output from the -12 and +32 volt supplies are applied to the +12 volt regulator circuit. The +32 volt output becomes positive as the +85 volt filter capacitors charge. As the +32 volt output rises, the +12 volt output also commences to rise. When +12 volts reaches its normal operating level, zener diode CR74 on circuit card A302 establishes the +32 volt level at 20 volts above the +12 volt level.

3-415. The output of the +20 volt power supply is applied to resistor R158 in the -20 volt regulator. As a result, -20 volts increases toward operating level as +20 volts rises and as the -20 volt output filter capacitor and bypass capacitors charge. The ultimate level of the -20 volt output is determined by the final level of the +20 volt output, which in turn is established by the temperature near the core stacks.

3-416. As the interior of the computer cabinet warms up during operation, and as ambient temperature changes, the resistance of A100R220 changes. This brings about a change in the +20 volt output. The shift in the +20 volt level, in turn, causes the -20 volt output to change. The voltages decrease in magnitude with rising temperature.

3-417. SHUT-DOWN SEQUENCE. Power shut-down can be a result of any of the following:

a. Turning the POWER switch off.

b. AC power-line failure (excessively low line voltage or no line voltage).

c. Failure or overloading of one of the six controlled voltages, which may lead to shut-down of some or all of the other controlled voltages.

d. Overheating which causes one of the thermal switches to open.

3-418. If a controlled voltage fails or is overloaded, or when a thermal switch opens, only dc shut-down takes place. When this occurs, the affected voltage or voltages are cut off by their series regulator transistors, but the ac circuits and the dc power sources remain in operation.

3-419. Shut-Down by Power Switch. When the POWER switch is turned off, relays A312K1 and A312K2 de-energize (figures 3-6 and 3-7), and filter capacitors throughout the power supply begin to discharge. At the moment the switch opens, +4.5 volts is removed from pin 52 of power fail interrupt card A6. A power-fail interrupt occurs. The POFP pulse produced during shut-down stops the program (if running). The POFP pulse also turns off the I/O system and interrupt priority system.

3-420. Approximately 8 milliseconds after the contacts of the POWER switch open, the PSO signal becomes false. (The 8-millisecond delay is typical. The time varies from 1 to 12 milliseconds, depending on power supply loading.) The false PSO signal, furnished to pin 11 of logic supply regulator card A301, starts the dc power supply shut-down sequence (figures 4-107 and 4-108).

3-421. The false PSO signal is forwarded through Zener diode CR58 and other components to the base of transistor Q33 on card A301. The 4.5 volt drop across the Zener diode results in the application of a negative voltage to Q33. As a result, series regulator transistors Q1 through Q4 in large heat sink assembly A304 cut off the flow of current from the +4.5 volt supply.

3-422. The false PSO signal is also furnished to the base of transistor Q38, stopping the flow of current from the -2 volt supply by cutting off transistors Q5, Q6, Q7, and Q8 in large heat sink assembly A304.

3-423. To shut down the remaining controlled voltages, the false PSO signal is applied to gate MC1A on logic supply regulator card A6. The gate no longer experiences coincidence, transistor Q43 conducts, and the -12 volt series regulator transistor stops the flow of current from the -12 volt power source. With the loss of -12 volts, the remaining controlled voltages are shut down. (See figure 3-30.)

3-424. When dc shut-down occurs for each controlled voltage, the filter capacitors on the input side of the series regulator transistors discharge through resistors provided for the purpose. The filter capacitor on the output side of each regulator discharges through the computer load circuits.

3-425. When relay A312K2 de-energizes, the power supply subsidiary voltages are turned off. To fully discharge all filter capacitors, approximately 3 minutes is required.

3-426. Shut-Down Due to AC Power-Line Failure. If the ac line-voltage drops below a level between 100 and 102 volts rms (200 to 204 volts for a 230-volt computer), a power-fail program interrupt occurs. If programmed to do so, and if the computer is running, the computer then performs a power-fail program. The dc voltage regulators

and filter capacitors can maintain normal dc voltage for at least 1 millisecond after complete and sudden ac line voltage failure. During this time the computer can perform at least 200 machine cycles. At the end of the power failure program the computer halts if so programmed. If the ac line voltage has dropped below about 80 volts rms (160 volts for a 230-volt computer), or has failed completely, filter capacitors discharge and the power supply regulators can no longer maintain the required voltage levels. The voltage which drops out of regulation first, and the ac line voltage at which this occurs, depends on the loading of the various regulators. This, in turn, depends on the quantity and type of optional devices installed in the computer.

3-427. When the first voltage drops out of regulation, other controlled voltages which depend on the affected voltage are shut down. Figure 3-30 illustrates the requirement of each controlled power supply with respect to outputs from other supplies. If any power supply drops out of regulation, the supplies to the right in the illustration are shut down. Also, if any supply to the right of the -12 volt supply loses regulation, -12 volts is shut down, resulting in all supplies shown to the right of the -12 supply being shut down.

3-428. A condition that could result from a continued abnormally low line voltage is that certain controlled voltages are shut down, while others continue to be furnished to the computer load.

3-429. When +12 volts is shut down, and if +4.5 volts is still available, power fail interrupt card A6 produces a power on/off pulse (POFP). This pulse turns off the I/O system and the interrupt priority system, and stops the computer if it is running.

3-430. If the ac line voltage becomes sufficiently low or if it drops to zero, relays A312K1 and A312K2 de-energize (figure 3-6). When line voltage returns to normal, the computer undergoes the normal power-on sequence and will then be ready for use, but will not be running.

3-431. If the ac line voltage is low enough to cause dc power shut-down, but is not sufficiently low for A312K1 and A312K2 to de-energize, power transformer A311T1 continues to furnish voltage to the rectifiers in the power supply. The series regulator transistors for the controlled voltages maintain the shut-down condition. Upon restoration of normal ac line voltage, the normal power turn-on sequence takes place except that relay A312K1 has remained energized and resistor A300R1 remains shorted out.

3-432. Shut-Down Due to Failure of a Controlled Voltage. If one of the controlled power supplies (+4.5, -2, +12, -12, +20, or -20 volts) experiences failure, other controlled supplies may be shut down. Failure of +32 volts will also cause shut-down of some controlled voltages. Figure 3-30 illustrates the requirement of each controlled power supply with respect to outputs from other supplies. A power fail interrupt occurs when shut-down of this type takes place. However, since a regulated dc voltage has failed, the power fail program may not function correctly.

3-433. When +12 volts is shut down, and if +4.5 volts is still available, power fail interrupt card A6 produces a power on/off pulse (POFP). This pulse turns off the I/O system and the interrupt priority system, and stops the computer if it is running.

3-434. Failure of a voltage regulator might result in a subnormal voltage from one of the supplies. If small, the drop in voltage may not be enough to disable gate MC1A on card A301. If this occurs, all power supplies continue to furnish voltage to the computer. The worst case is for +32 volts. This voltage is applied to MC1A through Zener voltage-dropping diode CR64, rated at 17.8 volts. Subtracting this amount from 32 volts leaves 14.2 volts. Clamp diode CR62 establishes a potential of +4.5 volts at the junction of the two diodes. Therefore, the +32 volt output must drop below 22.3 volts in order to bring about a decrease in potential at the junction of the diodes. The input to MC1A need be only +1.8 volts to be interpreted as true, therefore a further drop from +4.5 to below +1.8 volts can take place before the shut-down sequence is started.

3-435. Another result of voltage regulator failure could be an abnormally high voltage from the power supply. If the voltage becomes sufficiently high, the overvoltage protection circuit imposes a short on the power supply output (see table 3-11). As a result of the short, shut-down takes place for the affected voltage. This, in turn, may shut down other controlled voltages, as illustrated in figure 3-30. As previously noted, if shut-down occurs for any power supply to the right of the -12 volt supply in the illustration, the -12 volt supply itself is shut down, resulting in shut-down of all supplies shown to the right of the -12 volt supply.

3-436. When shut-down takes place because of failure of a controlled voltage, the +7 volt lamp voltage and the subsidiary voltages produced for use within the power supply section continue to be available.

3-437. Shut-Down Due to Open Thermal Switch. When a thermal switch opens, a power-fail interrupt occurs. The PSO signal becomes false (figure 3-7) and as a result, the six controlled voltages are shut down by their series regulator transistors. However, relays A312K1 and A312K2 remain energized and the fans continue to function. The +7 volt lamp voltage and the subsidiary voltages produced for use within the power supply section continue to be available. If there is sufficient cooling to permit the thermal switch to close after dc shut-down, the computer undergoes the normal power turn-on sequence except that A312K1 and A312K2 are already energized. The computer is available for use after this turn-on, but is not running.

3-438. PON SIGNAL. A power-on-normal (PON) signal is furnished by power fail interrupt card A6 when +4.5 and -2 volts are available to the computer. The PON signal becomes true approximately 0.1 second after these voltages are furnished to the computer load, and the signal remains true while both voltages remain available.

3-439. When false, the PON signal protects stored data by preventing memory readout during the transient conditions of power turn-on. The false PON signal also prevents certain operations of I/O devices, such as drum or disc writing, during power turn-on and shut-down.

3-440. The PON signal is furnished to X-Y driver-switch cards A8, A11, A18, and A21. Here the PON signal, when false, prevents activation of core memory X and Y drive lines. Memory readout therefore cannot occur. The PON signal also affects the state of the memory-normal-switch (MNS) signal furnished to timing generator card A106. When PON is false MNS also is false, and control signals used for writing and reading in core memory remain false, providing further protection against destruction of stored data.

3-441. The function of the PON signal on I/O interface cards is described in the operating and service manual for the device concerned.

3-442. As noted, the PON signal becomes true approximately 0.1 second after +4.5 and -2 volts are furnished to card A6 during turn-on. The potential at the base of transistor Q3 on card A6 is then approximately +2.5 volts with respect to ground (figure 7-5). Since the collector connects to +4.5 volts, the base of the transistor is negative with respect to its collector and the transistor conducts. Capacitor C5 commences to charge. After approximately 0.1 second, the capacitor is sufficiently charged to cause the PON signal to become true. The switching action of driver MC17A steepens the leading edge of the PON signal from the exponential charge-curve of capacitor C5.

3-443. POFP PULSE. During dc turn-on and shut-down a power on/off pulse (POFP) is produced by power fail interrupt card A6. The pulse is produced for any power shut-down, regardless of cause, which brings about cutoff of the +12 volt regulator.

3-444. The POFP pulse ensures that the computer is halted, that it is in the fetch phase, and that the I/O system and interrupt priority system are turned off. To bring about these conditions, the POFP pulse sets or clears flip-flops as follows:

a. POFP clears the Run 1 and Run 2 flip-flops on timing generator card A106. This ensures that the computer is halted.

b. POFP sets the Phase 1 Flip-Flop on timing generator card A106. This places the computer in the fetch phase.

c. POFP initiates reset of the Interrupt Control Flip-Flop on I/O control card A201, and reset of the Flag and Control Flip-Flops on each I/O interface card. This turns off the I/O system.

d. POFP resets the Flag Flip-Flop on power fail interrupt card A6. This disables the entire priority system. Before the computer is started, the interrupt priority system is made effective by pressing the PRESET switch, thereby resetting the Flag Flip-Flop on card A6.

3-445. A single POFP pulse is produced each time the computer is turned on or off. The pulse is also produced when +12 volts fails or when +12 volts is shut down by an open thermal switch or by failure of another voltage. The POFP pulse, which is true for about 40 milliseconds, is produced by transistors Q2, Q3, and Q4 and their associated components, on card A6 (figure 7-5). When +4.5 volts and -2 volts become available during power turn-on the base of Q3 is negative with respect to its emitter, and the transistor conducts. Before +12 volts is furnished, the base of Q4 is more positive than its emitter, and the transistor is cut off. Transistor Q2, however, conducts heavily and furnishes nearly +4.5 volts to pin 6 of gate MC57B. As a result, the POFP signal becomes true. The true output of Q2 also resets the Flag Flip-Flop on card A6. Diode CR9 permits the true output of Q2 to be applied to the Flag Flip-Flop, while preventing the output of gate MC57A from being applied to MC57B. When +12 volts is furnished to the cathode of CR7, Q2 cuts off and the POFP pulse becomes false.

3-446. During shut-down, the POFP pulse becomes true when +12 volts is removed from the cathode of diode CR7. The pulse remains true until +4.5 volts is shut down.

3-447. POWER-FAIL INTERRUPT CIRCUITS. If the ac line-voltage drops below a level between 100 and 102 volts rms (200 to 204 volts if the computer is connected for 230-volt operation), a power-fail interrupt occurs. The priority of this interrupt is 4, and it causes a program jump to core-memory address 00004. From that point, operations depend on whether a power-fail interrupt program is stored in memory. The program is written to suit the needs of the particular installation, but in general it stores the contents of registers and performs other actions in preparation for later start-up at the point of program termination.

3-448. The circuits which initiate the power-fail interrupt are on power fail interrupt card A6 (figure 7-5). Pins 79 and 80 of this card receive a voltage furnished by a center-tapped secondary winding on transformer A311T1 in the power supply section. With normal ac line-voltage, pins 79 and 80 each receive about 18 volts ac rms with respect to ground, with the voltage at the two pins being 180 degrees out of phase. This ac voltage is rectified by diodes CR1 and CR2, which together constitute a full-wave rectifier. Resistor R3, with capacitors C2 and C3, filter the rectified voltage.

3-449. The rectified voltage is applied to a voltage divider made up of resistors R6, R7, and R8. Potentiometer R7 is adjusted so that with normal ac line-voltage transistor Q7 conducts and Q8 is cut off. The collector source for Q8 is pin 3 of gate MC97B, which normally is slightly negative.

3-450. If the ac line-voltage becomes excessively low Q7 cuts off, Q8 conducts, and gate MC87B experiences coincidence. As a result, a power-fail interrupt occurs.

3-451. Further discussion of the circuits which produce the interrupt is presented in paragraph 4-180.

3-452. GROUND CIRCUITS.

3-453. AC NEUTRAL.

3-454. In keeping with international safety regulations, the power-line ac neutral input to the computer is not connected to the computer frame.

3-455. FRAME GROUND.

3-456. Schematic diagrams which show frame ground connections are the following:

a. A300 power supply assembly schematic (figure 7-34).

b. A502 control panel assembly schematic (figures 7-36 and 7-37).

c. Overall interconnection diagram (figure 7-38).

3-457. The earth-ground conductor in the ac power cable is connected to the frame of the computer at the base of connector A300J1.

3-458. The power supply dc ground-return circuit is connected to the computer frame at the anode of diode A308CR9. This diode bolts to a metal bracket attached to the computer frame. No insulating washer is used for mounting the diode, and its anode is therefore electrically connected to the mounting bracket.

3-459. The frame of the card cage is connected to the power supply dc ground-return circuit at point E2, where the ground strap from the power supply bolts to the frame of the card cage. DC ground return is also connected to the card cage frame in overvoltage protection assembly A121.

3-460. The door is connected to the dc ground-return circuit at a lug beside POWER switch A502S109.

3-461. CARD GROUND.

3-462. For each etched-circuit card in the card cage, ground connection is made at backplane pins 1, 2, 85, and 86. In most cases, these pins serve for both dc ground-return and signal ground-return. In some instances, additional pins are used for signal ground-return in order to eliminate coupling due to voltage drop in common ground returns. These signal-ground pins are shown on the applicable logic diagrams.

3-463. Cards which have a 48-pin connector on the front use pins 1, A, 24, and BB of the connector for signal ground-return. In some cases additional pins also are employed.

3-464. BUS BARS.

3-465. Three square bus bars are installed on the right side of the power supply section. At the top, they curve over capacitor board assembly A303. At the bottom, flexible metal straps are attached to make connection with the card cage. The front bus bar carries regulated +4.5 volts. The middle bus bar is at ground potential. The rear bus bar carries regulated -2 volts.

3-466. The +4.5 volt, ground, and -2 volt circuits for all cards in the card cage are routed through small vertical bus bars, visible between the backplane connectors when they are viewed from the card side. These attach to heavy horizontal bars, covered with white tape, which make connection with three conducting straps from the power supply at points A100E1, A100E2, and A100E3, respectively (figure 1-5). The far end of each vertical bus bar passes through the backplane and makes attachment to a horizontal bus bar on the wiring side of the backplane connectors. Several vertical bus bars are used for each voltage, one end making attachment to the horizontal bus bar on the card side of the backplane, the other end making connection with the horizontal bus bar on the wiring side of the backplane.

3-467. On the wiring side of the backplane, the horizontal bus bars for +4.5 volts make connection with pins 39 and 40 of each circuit card. The ground horizontal bus bars connect to pins 1, 2, 85, and 86. The -2 volt bus bars make connection with pins 47 and 48.

3-468. Additional ground connections to a circuit card, if any, are made by insulated copper wires.

3-469. Two additional voltage buses are used on the backplane. These apply +12 volts to pins 43 and 44, and -12 volts to pins 69 and 70, of all circuit cards in the bottom row of cards. One end of each bus bar is connected by insulated copper wire to terminal strip A100TB2.

SECTION IV

TROUBLESHOOTING

4-1. INTRODUCTION.

4-2. This section of the manual contains testing and troubleshooting data for the computer's control section, arithmetic section, memory section, input/output section, and power supply section. The test data is used to check the overall performance of the computer. The troubleshooting data is used to check the computer sections at the circuit level.

4-3. TEST DATA.

4-4. Test data for the computer consists of the basic checkout (paragraph 4-9) and the diagnostic checkout (paragraph 4-17). Performing the basic checkout test procedure is the first step of computer testing. This procedure consists of step-by-step instructions for using front panel switches and indicators to make a preliminary check of the computer's performance before more detailed testing is attempted. Trouble symptoms detected in making this check are analyzed to establish which circuit function is most probably causing the trouble indication. If no trouble symptoms are detected in the course of performing the basic checkout procedure, the computer is assumed to be capable of loading, storing, and at least partially executing diagnostic test programs.

4-5. Performing the diagnostic checkout test procedure is the next step of computer testing. Diagnostic test programs are used to dynamically check the operation of the circuits in the control, arithmetic, memory, and input/output sections of the computer. Trouble symptoms are indicated by error halts displayed at the front panel. By carefully analyzing the error halt condition, the cause of the trouble can be traced to one or more instructions in the test program which the computer failed to process. References are provided to detailed troubleshooting data for the circuits suspected of causing the failure. If no error halts are detected in the course of performing the diagnostic checkout procedure, the computer is assumed to be ready to resume normal operation.

4-6. TROUBLESHOOTING DATA.

4-7. Troubleshooting data, used to isolate trouble symptoms that are found while performing the basic checkout or the diagnostic checkout, is given in this manual as follows: troubleshooting procedures in section IV; maintenance procedures in section V; replaceable parts information in section VI; logic diagrams, component location diagrams; logic equations, and wiring lists in section VII. These portions of the manual provide necessary information for trouble isolation to a replaceable assembly or part.

4-8. Additional troubleshooting information is provided in other computer-related manuals. Volume Three of the computer documentation describes principles of operation for the I/O section of the computer. Separate operating and service manuals are provided for processor and interface options. Procedures for running diagnostic test programs are contained in the Manual of Diagnostics. Other software and system manuals describe the software used with the computer and provide system-level operating procedures.

4-9. BASIC CHECKOUT.

4-10. GENERAL.

4-11. The basic checkout test procedure is performed using operating switches and indicators to check the overall performance of the computer. This test procedure should be conducted immeidately after the computer is installed, as required thereafter as part of a regularly scheduled preventive maintenance program, as the first step of troubleshooting, and after repairs or modifications are made to the computer. The basic checkout should always be performed prior to attempting to perform the diagnostic checkout. Successful completion of all test steps in the basic checkout procedure ensures that the computer is operational to the extent that diagnostic test program can be loaded into memory and at least partially executed.

4-12. REQUIRED TEST EQUIPMENT.

4-13. A four-digit dc digital voltmeter (equivalent to a HP 3439A Plug-in Digital Voltmeter with a HP 3441A Range Selector) is required for performing the basic checkout procedure. The following test equipment, or its equivalent, should be available in the event it is required for troubleshooting:

a. HP 180A Plug-In Oscilloscope Main Frame.

b. HP 1801A Vertical Amplifier (plug-in for HP 180A).

c. HP 1820A Time Base (plug-in for HP 180A).

d. HP 10004A Miniature Resistive Divider Probes (10:1).

e. HP 427A Multi-Function Meter.

f. HP 10525A Logic Probe.

g. Extender card (part no. 02116-63216).

h. Extender cable (part no. 5060-8315).

i. Extender cable (part no. 02115-6047).

4-14. TEST PROCEDURE.

4-15. The basic checkout procedure consists of a series of tests that check the operation of key circuit functions in the computer. The purpose of these tests is to provide an expedient means of detecting obvious trouble symptoms. The results of each test, when compared to expected normal results, provides an indication as to whether or not the circuit under test is functioning normally. Instructions are included for analyzing trouble symptoms. Troubles encountered during the performance of the basic checkout must be corrected before diagnostic testing is attempted.

4-16. Instructions for performing the basic checkout procedure are contained in the following steps:

Note

If computer power is on at the start of this procedure, check the status of all front panel indicators before turning off the power. If possible, check the indicators while the computer is in the run mode, and again while the computer is in the halt mode. Carefully note and record any trouble symptoms which are observed as well as those reported by the computer operator. This information may prove useful in the troubleshooting process.

a. At the front panel of the computer, turn off power.

b. Open the door assembly and remove the four retaining screws securing the card cage to the mainframe. Fully extend the card cage from the cabinet and swing it out to the servicing position.

WARNING

Dangerous ac line voltage is present in the computer even though the POWER switch has been turned off at the front panel. Protective panels and covers installed on the power supply, in the bottom of the card cage, and over the wiring side of the POWER switch are designed to prevent personal contact with components that are wired directly to the hot side of the ac line. Use caution when servicing in these areas even though the protective panels and covers are in place. If it is necessary to remove a protective panel or cover during servicing, first turn off all ac line voltage from the computer by disconnecting the power cord from ac power input connector A300J1 at the rear panel of the computer. If it is necessary to apply power to the computer while a protective panel or cover is removed, use extreme caution to avoid contact with the exposed area. Refer to paragraph 5-7 for additional safety information before proceeding.

c. Inspect the electrical assemblies and parts comprising the door assembly, backplane, and power supply for visible indications of trouble, such as burned wiring, broken wiring connections, loose or improper cable connections, or plug-in cards installed in wrong slots or improperly seated in mating connectors. Also inspect for excessive dirt accumulations or foreign matter that could restrict airflow through the cabinet and cause overheating. Take immediate action to correct any condition that may be the cause of trouble. Note those conditions that do not require immediate corrective action, but which should be serviced when regularly scheduled preventive maintenance is performed.

d. At the front panel of the computer, check that the LOADER switch is in the PROTECTED position. On the display board located behind the front panel, check that the MEMORY, PHASE, and INSTRUCTION switches are in the NORM position. If these switches are not set as specified, set them to the NORM position before proceeding.

Note

If the 12588A Power Failure Interrupt With Automatic Restart Option (option 008) is installed, the computer program may start automatically when power is turned on. To prevent this from happening, press and hold either the HALT switch or the PRESET switch whenever power is turned on.

e. At the front panel of the computer, turn on power. Check that fans A300B1 at the top of the power supply, A304B2 and A305B3 on the bottom of the heat sink assemblies, and A200B1, A200B2, and A200B3 on the bottom of the card cage are operating properly. Check each fan for abnormal airflow and audible indications of defective motor bearings, fan blade obstructions, or other indications of abnormal operation. If all fans are operating normally, proceed to step "f." Otherwise, select the applicable step from those following and proceed as directed:

(1) If all fans are inoperative, turn off power. Check the condition of fuse A312F1 (see figure 4-109). If the fuse is blown, replace it and repeat step "e" above. If the fuse blows again, refer to paragraph 4-510 and troubleshoot for a short in the ac distribution circuits. If the fuse was intact when checked, refer to paragraph 4-509 and troubleshoot for an open condition in the ac distribution circuits.

(2) If one or more but not all fans are inoperative, turn off power. Disconnect the power cord from ac power input connector A300J1 at the rear panel of the computer and check the wiring to the inoperative fan (see figure 3-6). If defective wiring is not the cause of the trouble, replace the inoperative fan, and repeat step "e."

CAUTION

Do not continue with this procedure unless all fans are operating normally. Loss of airflow from an inoperative or improperly operating fan may cause overheating which could result in serious damage to computer components. Turn off power and do not attempt further operation until the trouble has been corrected.

f. Make a general inspection of the indicators on the front panel of the computer. Then select the applicable step from those following and proceed as directed:

(1) If all indicators are off, check the +4.5 supply voltage at the +4.5V test point on overvoltage protection assembly A121. If the indication is abnormal, refer to paragraph 4-513 and troubleshoot the +4.5-volt supply. If the indication is normal, refer to paragraph 4-515 and troubleshoot the +7-volt supply.

Note

Step (2) following applies only to computers equipped with POWER indicator A502DS109.

(2) If the POWER indicator is on and all other indicators are off, refer to paragraph 4-515 and troubleshoot the +7-volt supply.

(3) If at least some of the indicators are on, check whether the indicators listed in table 4-1 are providing normal indications. If all indicators are normal, proceed with step "g." If an abnormal indication is encountered, take the corrective action specified in the table.

g. At the front panel of the computer, press and release the PRESET switch and check that the PRESET indicator goes off. If the indication is normal, proceed to step "h". If the indication is abnormal, refer to paragraph 4-81 and troubleshoot the circuits associated with the PRESET switch.

Note

Throughout this manual, displays by binary indicators 0 through 15 of the T-REGISTER MEMORY DATA display, P-REGISTER PROGRAM COUNTER display, M-REGISTER MEMORY ADDRESS display, A-REGISTER ACCUMULATOR display, and B-REGISTER ACCUMULATOR display are expressed as six digit octal numbers. For example, a sixteen bit binary display of 0 000 110 111 010 101 (corresponding to indicators 15 through 0 as viewed from left to right at the computer front panel, with indicators that are on representing a binary 1, and indicators that are off representing a binary 0) is expressed as 006725. Settings for the switches in the SWITCH REGISTER are also expressed as six digit octal numbers. For example, the setting 1 011 100 001 111 000 for switches 15 through 0 (as viewed from left to right at the front panel, with binary 1 selected by switches set to the up position, and binary 0 selected by switches set to the down position is expressed as 134170.

h. Set the SWITCH REGISTER to 000000 (switches 15 through 0 in the down position) and sequentially press LOAD MEMORY, LOAD ADDRESS, LOAD A, and LOAD B switches. Set the SWITCH REGISTER to 177777 (switches 15 through 0 in the up position). Press and release the LOAD A switch and check the A-REGISTER ACCUMULATOR display for an indication of 177777 (indicators 15 through 0 on). If the indication is normal, proceed to step "i". If all indicators in the display fail to go on, refer to paragraph 4-86 and troubleshoot the circuits associated with the LOAD A switch. If only one of the indicators in the display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, troubleshoot the circuits associated with the unresponsive indicator.

i. Set the SWITCH REGISTER to 000000 (switches 15 through 0 in the down position). Press and release the LOAD A switch and check the A-REGISTER ACCUMULATOR display for an indication of 000000 (indicators 15 through 0 off). If the indication is normal, proceed to step "j". If all indicators in the display fail to go off, refer to paragraph 4-86 and troubleshoot the circuits associated with the LOAD A switch. If only one of the indicators in the display fails to go off, troubleshoot the circuits associated with the unresponsive indicator.

j. Set the SWITCH REGISTER to 177777. Press and release the LOAD B switch and check the B-REGISTER ACCUMULATOR display for an indication of 177777. If the indication is normal, proceed to step "k". If all indicators in the display fail to go on, refer to paragraph 4-92 and troubleshoot the circuits associated with the LOAD B switch. If only one of the indicators in the display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, troubleshoot the circuits associated with the unresponsive indicator.

k. Set the SWITCH REGISTER to 000000. Press and release the LOAD B switch and check the B-REGISTER ACCUMULATOR display for an indication of 000000. If the indication is normal, proceed to step "l". If all indicators in the display fail to go off, refer to paragraph 4-92 and troubleshoot the circuits associated with the LOAD B switch. If only one of the indicators in the display fails to go off, troubleshoot the circuits associated with the unresponsive indicators.

Table 4-1. Front Panel Indicator Initialization, Checkout and Trouble Analysis

INDICATOR	NORMAL INDICATION	IF INDICATION IS ABNORMAL
POWER	On	Replace POWER indicator lamp A502DS109. If lamp replacement fails to correct the trouble check for proper operation of the +12-volt power supply. If +12-volt power is available, refer to paragraph 4-68 and troubleshoot the circuits associated with the POWER indicator.
RUN	Off	Press and release the HALT switch. If the RUN indicator remains on, troubleshoot the circuits associated with the RUN indicator. If pressing the HALT switch turns off the RUN indicator, refer to paragraph 4-517 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal.
HALT	On	Press and release the HALT switch. If the HALT indicator is now on, refer to paragraph 4-517 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the HALT indicator remains off, replace indicator lamp A502DS107. If lamp replacement fails to correct the trouble, refer to paragraph 4-76 and troubleshoot the circuits associated with the HALT indicator.
FETCH	On	Press and release the PRESET switch. If the FETCH indicator is now on, refer to paragraph 4-517 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the FETCH indicator remains off, replace indicator lamp A501DS84. If lamp replacement fails to correct the trouble, refer to paragraph 4-167 and troubleshoot the circuits associated with the FETCH indicator.
INDIRECT	Off	Press and release the PRESET switch. If the indicator is now off, troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the INDIRECT indicator remains on, refer to paragraph 4-171 and troubleshoot the circuits associated with the INDIRECT indicator.
EXECUTE	Off	Press and release the PRESET switch. If the EXECUTE indicator is now off, refer to paragraph 4-517 and troubleshoot the circuits associated with the Power On/Off Pulse (POFP) signal. If the EXECUTE indicator is still on, refer to paragraph 4-176 and troubleshoot the circuits associated with the EXECUTE indicator.
PRESET	On	Replace indicator lamp A502DS108. If lamp replacement fails to correct the trouble, refer to paragraph 4-81 and troubleshoot the circuits associated with the PRESET indicator.
PARITY HALT	Off	Refer to the operating and service manual for the HP 12591A Parity Error Option (manual part no. 12591-9001) and troubleshoot the circuits associated with the PARITY HALT indicator. *Only certain computers with serial number prefix 980- are equipped with this indicator.

l. Set the SWITCH REGISTER to 177777. Press and release the LOAD ADDRESS switch and check both the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display for an indication of 177777. If the indication by both displays is normal, proceed to step "m". If all indicators in either or both displays fail to go on, refer to paragraph 4-98 and troubleshoot the circuits associated with the LOAD ADDRESS switch. If only one indicator in either display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, troubleshoot the circuits associated with the unresponsive indicator.

m. Set the SWITCH REGISTER to 000000. Press and release the LOAD ADDRESS switch and check both the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display for an indication of 000000. If the indication by both displays is normal, proceed to step "n". If all indicators in either or both displays fail to go off, refer to paragraph 4-98 and troubleshoot the circuits associated with the LOAD ADDRESS switch. If only one indicator in either display fails to go off, troubleshoot the circuits associated with the unresponsive indicator.

n. Set the SWITCH REGISTER to 177777. Press and release the LOAD MEMORY switch and check the T-REGISTER MEMORY DATA display for an indication of 177777. If the indication is normal, proceed to step "0". If all indicators in the display fail to light, refer to paragraph 4-106 and troubleshoot the circuits associated with the LOAD MEMORY switch. If only one indicator in the display fails to go on, replace the associated indicator lamp. If lamp replacement fails to correct the trouble, troubleshoot the circuits associated with the unresponsive indicator.

o. Set the SWITCH REGISTER to 000000. Press and release the LOAD MEMORY switch and check the T-REGISTER MEMORY DATA display for an indication of 000000. If the indication is normal, proceed to step "p". If all indicators in the display fail to go off, refer to paragraph 4-106 and troubleshoot the circuits associated with the LOAD MEMORY switch. If only one of the indicators in the display fails to go off, troubleshoot the circuits associated with the unresponsive indicator.

p. Set the SWITCH REGISTER to 177770 and press and release the LOAD ADDRESS switch. While observing the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display, press and release the LOAD MEMORY switch seven times and check that both displays are incremented by a count of one each time the LOAD MEMORY switch is pressed and released. Both displays should indicate 177777 after the LOAD MEMORY switch has been pressed and released seven times. If the indication by either or both displays is abnormal, refer to paragraph 4-106 and troubleshoot the circuits associated with the LOAD MEMORY switch. If the indication by both displays is normal, press the LOAD MEMORY switch two more times. Both displays should indicate 000000 when the LOAD MEMORY switch is pressed the second time. If the indications by both displays are normal, proceed to step "q". If the indication by either display is abnormal, troubleshoot the circuits associated with the carry bit signals generated on the arithmetic logic cards in slots 102, 103, 104, and 105.

q. Set the SWITCH REGISTER to 177770 and press and release the LOAD ADDRESS switch. While observing the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display, press and release the DISPLAY MEMORY switch seven times and check that both displays are incremented by a count of one each time the DISPLAY MEMORY switch is pressed and released. (Both displays should indicate 177777 after the DISPLAY MEMORY switch has been pressed and released seven times.) If the indication by both displays is normal, proceed to step "r". If the indication by either or both displays is abnormal, refer to paragraph 4-116 and troubleshoot the circuits associated with the DISPLAY MEMORY switch.

r. Set the SWITCH REGISTER to 177770 and press and release the LOAD ADDRESS switch. While observing the P-REGISTER PROGRAM COUNTER display and the M-REGISTER MEMORY ADDRESS display, press and release the SINGLE CYCLE switch seven times and check that both displays are incremented by a count of one each time the SINGLE CYCLE switch is pressed and released. (Both displays should indicate 177777 after the SINGLE CYCLE switch has been pressed and released seven times.) If the indication is normal, proceed to step "s". If the indication by either or both displays is abnormal, refer to paragraph 4-124 and troubleshoot the circuits associated with the SINGLE CYCLE switch.

Note

Use care when performing steps "s" and "t" following to prevent the loader program from being destroyed. If this should happen, reload the required instruction words into the protected area of memory using the applicable procedure and listing presented in table 4-3, and repeat steps "s" and "t" before proceeding to step "u".

s. Determine which loader program is required for the software system used with the computer. Then, using the verification procedure presented in table 4-3, check the contents of all 64 memory locations in the protected area of memory. If the content is correct, proceed to step "t". If incorrect, attempt to load the correct words using the applicable procedure and listing presented in table 4-3. Then verify the contents in the reloaded memory locations to ensure that each word is loaded properly. If this is not the case, refer to paragraph 4-156 and troubleshoot the memory timing circuits before proceeding to paragraph 4-458 and troubleshooting the circuits comprising the memory section of the computer.

t. Again, using the verification procedure presented in table 4-3, recheck the contents of the first 12 memory locations in the protected area of memory (addresses 0m7700 through 0m7713). If all 12 instructions are still correct, proceed to step "u". If any one or all of the instructions are now incorrect, refer to paragraph 4-458 and troubleshoot the circuits associated with memory write circuits.

Note

Make sure the LOADER switch has been reset to the PROTECTED position before proceeding. This protects the absolute loader program and is also necessary to obtain correct results while performing step "v".

u. At the front panel of the computer, proceed as follows:

Note

Steps (1) through (8) below contain a step-by-step procedure for manually loading a test program into the computer memory in preparation for performing steps "v" through "y". The test program consists of five instructions that can be stored in any five consecutive memory locations in a memory page (other than protected, reserved, or inaccessible locations). The memory locations specified for these instructions are typical, and may be changed to any unused area in memory to prevent destroying program data or instructions already stored in the specified locations. Therefore, if a starting address other than 004000 is used, modify the octal values accordingly for the SWITCH REGISTER settings given in steps (1), (6), and (8).

(1) Set the SWITCH REGISTER to 004000 (typical address for the first instruction of the program) and press and release the LOAD ADDRESS switch.

(2) Set the SWITCH REGISTER to 002400 (CLA) and press and release the LOAD MEMORY switch.

(3) Set the SWITCH REGISTER to 060001 (LDA) and press and release the LOAD MEMORY switch.

(4) Set the SWITCH REGISTER to 006400 (CLB) and press and release the LOAD MEMORY switch.

(5) Set the SWITCH REGISTER to 164000 (LDB,I) and press and release the LOAD MEMORY switch.

(6) Set the SWITCH REGISTER to 026000 (JMP) and press and release the LOAD MEMORY switch.

(7) Set the SWITCH REGISTER to 177777, and in turn, press and release the LOAD A switch and the LOAD B switch.

(8) Set the SWITCH REGISTER to 004000 (the starting address of test program), and press and release the LOAD ADDRESS switch. Then proceed to step "v".

v. Refer to table 4-2. While observing the front panel for the indications specified in the table, press and release the SINGLE CYCLE switch exactly nine times. If all indications are normal, proceed to step "w". If an indication associated with the FETCH, INDIRECT, or EXECUTE indicators is abnormal, refer to paragraph 4-164 and troubleshoot the phase logic circuits. If an indication associated with either the A-REGISTER ACCUMULATOR display or the B-REGISTER ACCUMULATOR display is abnormal, determine which instruction failed to process; then refer to table 4-6 and troubleshoot accordingly.

w. Check the M-REGISTER MEMORY ADDRESS display for an indication of 004000 (the starting address used for test program at step "u" (1) above). If the indication is normal, proceed to step "x". If the indication is abnormal, refer to paragraph 4-220 and troubleshoot the circuits associated with the JMP instruction.

x. Press and release the RUN switch and check that the RUN indicator goes on and the HALT indicator goes off. If the indication is normal, proceed to step "y". If the indication for either the RUN or the HALT indicator is abnormal, refer to paragraph 4-71 and troubleshoot the circuits associated with the RUN switch and RUN indicator.

y. Press and release the HALT switch and check that the RUN indicator goes off and the HALT indicator goes on. If the indication is normal, proceed to step "z". If the indication for either the RUN or the HALT indicator is abnormal, refer to paragraph 4-76 and troubleshoot the circuits associated with the HALT switch and HALT indicator.

z. If all indications in the preceding steps were normal, slide the card cage into the cabinet and close the door assembly. Then refer to paragraph 4-17 and perform the diagnostic checkout procedure.

4-17. DIAGNOSTIC CHECKOUT.

4-18. GENERAL.

4-19. Diagnostic checkout consists of running a series of test programs that automatically perform a dynamic test of computer operation by exercising major portions of the circuit functions in the control, arithmetic,

Table 4-2. Phase Logic Indicators, Checkout and Trouble Analysis

TIMES SINGLE CYCLE SWITCH IS PRESSED	CIRCUIT ACTION	INDICATION AT FRONT PANEL				
		FETCH INDICATOR	INDIRECT INDICATOR	EXECUTE INDICATOR	A-REGISTER ACCUMULATOR DISPLAY	B-REGISTER ACCUMULATOR DISPLAY
0	Initial indication.	On	Off	Off	177777	177777
1	Fetch and execute CLA instruction and set phase 1.	On	Off	Off	000000	177777
2	Fetch LDA instruction and set phase 3.	Off	Off	On	000000	177777
3	Execute LDA instruction and set phase 1.	On	Off	Off	177777	177777
4	Fetch and execute CLB instruction and set phase 1.	On	Off	Off	177777	000000
5	Fetch LDB,I instruction and set phase 2.	Off	On	Off	177777	000000
6	Set indirect address and set phase 2.	Off	On	Off	177777	000000
7	Set phase 3.	Off	Off	On	177777	000000
8	Execute LDB,I instruction and set phase 1.	On	Off	Off	177777	177777
9	Fetch and execute JMP instruction and set phase 1.	On	Off	Off	177777	177777

memory, and input/output sections. The diagnostic checkout test procedure should be conducted immediately after the computer is installed, as required thereafter as part of a regularly scheduled preventive maintenance program, during troubleshooting, and after making repairs or modifications to the computer. Information and instructions pertinent to performing the diagnostic checkout are presented in paragraphs 4-20 through 4-33 following.

4-20. REQUIRED PROGRAM TAPES AND PROCEDURES.

4-21. Diagnostic test programs are stored in absolute form on punched paper tapes. Tapes required for testing are referenced by name and part number in diagnostic program procedures contained in the Manual of Diagnostics. For ease of identification, labels specifying program name and part number are affixed to the storage box containing the tape, and to the beginning of the tape itself.

4-22. The diagnostic program procedures in the Manual of Diagnostics also provide instructions for running the diagnostic test programs. Each procedure within the Manual of Diagnostics is identified by a part number printed on the title page of the document. The names and part numbers of the procedures used for running the test programs that check the basic circuits of the computer are as follows:

a. Alter-Skip Instruction Test (part no. 02116-91761).

b. Memory Reference Instruction Test (part no. 02116-91762).

c. Shift-Rotate Instruction Test (part no. 02116-91763).

d. High Memory Address Test (part no. 02116-91792).

e. Low Memory Address Test (part no. 02116-91792).

f. High Memory Pattern Test (part no. 02116-91782).

g. Low Memory Pattern Test (part no. 02116-91782).

h. Input/Output Interrupt Test (part no. 02116-91768).

i. Power Fail Interrupt Test (part no. 02116-91759), or if option 008 is installed in the computer, Power Fail With Auto Restart Test (part no. 02116-91769).

Note

Diagnostic test procedures for test programs used in testing optional processing and interfacing circuits are referenced in the operating and service manuals furnished with the options.

4-23. TEST ASSUMPTIONS.

4-24. Performance of the diagnostic checkout is based on the following assumptions:

a. *No trouble symptoms are encountered when the basic checkout procedure is performed.* (The basic checkout procedure, presented in paragraph 4-9, provides a confidence check of computer operation and should be performed first, before the diagnostic checkout is attempted. Any trouble experienced during basic checkout should be corrected before the diagnostic test programs are loaded and run.)

b. *A valid loader program is stored in the protected area of memory.* Loading absolute programs into the computer from paper tape requires that a properly configured loader program be stored in the protected area of memory. Refer to table 4-3 for procedures used in verifying the contents of the protected area of memory, and for loading words into this area of memory from the front panel of the computer. Table 4-3 also provides listings for both the standard Basic Binary Loader (BBL) program and the Basic Binary Disc Loader (BBDL) program. These listings also appear on the Tape Loading Instruction Card, part number 5080-6599, supplied as part of the computer accessory kit described in Section I of this manual. Either loader program can be used for loading diagnostic test programs. However, the loader program used must also be compatible with the software system used with the computer. Refer to the applicable software and system manuals provided with the computer to determine which loader program should be stored in the protected area of memory.

c. *Availability of a tape reading device, in good operating condition, that is properly interfaced to the computer and capable of reading tapes punched in absolute form.* (Suitable devices typically used with the computer are described in paragraph 4-29.)

4-25. TEST PROCEDURE.

4-26. TEST SEQUENCE. The diagnostic checkout procedure for the basic computer is performed using the diagnostic program procedures listed in paragraph 4-22. Using these procedures, and the applicable tape loading procedure presented in paragraphs 4-28 through 4-31, load and run in sequence the alter-skip, memory reference, and shift-rotate test programs. Then load and run in any desired order the remaining test programs listed in paragraph 4-22, followed by the test programs for all optional processing and interfacing circuits installed in the computer. If all test programs run without error, the computer is ready for normal operation.

4-27. ERROR HALTS. If an error halt is encountered in the course of running a diagnostic test program, use the information presented in the diagnostic program procedure to determine which instruction or sequence of instructions in the program the computer failed to process. Then refer to table 4-6 and troubleshoot the circuits associated with the improperly processed instruction.

4-28. PROCEDURES FOR LOADING DIAGNOSTIC TAPES.

4-29. Typical input devices that can be used to read test programs from punched paper tapes and transfer them into computer memory include the HP 2748A Punched Tape Reader, the HP 2758A Punched Tape Reader-Reroller, and the HP 2752A Teleprinter. Procedures for using these devices are presented in the following paragraphs. For procedures using other devices, refer to the specific manual for the device, or the appropriate system documentation.

4-30. LOADING DIAGNOSTIC TAPES USING THE HP 2748A TAPE READER. The procedure for using the 2748A to load programs from punched paper tapes is as follows:

a. At the tape reader, press the POWER switch to energize the unit.

b. Press the LOAD switch to release the reader pinch roller.

c. Thread the tape through the tape reader as instructed in the 2748A Tape Reader Operating and Service Manual (manual part no. 02748-90023).

d. Press the READ switch. (The tape reader is now ready to read the tape.)

Note

To configure the address specified in step "e" following, replace the variable "m" in the starting address with the number corresponding to the size of computer memory (i.e., 1 for 8K, 3 for 16K, 5 for 24K, or 7 for 32K).

e. At the computer front panel, press the HALT switch. (The HALT indicator should now be on, and the RUN indicator should be off.) Enter 0m7700 (the starting address of the loader program stored in the protected area of memory) into the SWITCH REGISTER and press the LOAD ADDRESS switch.

Table 4-3. Loader Listings and Procedures

Absolute Listing for Basic Binary Loader (BBL) Program

ADDRESS	0	1	2	3	4	5	6	7
0m7700:	107700	063770	106501	004010	002400	006020	063771	073736
0m7710:	006401	067773	006006	027717	107700	102077	027700	017762
0m7720:	002003	027712	003104	073774	017762	017753	070001	073775
0m7730:	063775	043772	002040	027751	017753	044000	dddddd	002101
0m7740:	102000	037775	037774	027730	017753	054000	027711	102011
0m7750:	027700	102055	027700	dddddd	017762	001727	073776	017762
0m7760:	033776	127753	dddddd	1037cc	1023cc	027764	1025cc	127762
0m7770:	173775	153775	1n0100	177765	dddddd	dddddd	dddddd	dddddd

Absolute Listing for Basic Binary Disc Loader (BBDL) Program

ADDRESS	0	1	2	3	4	5	6	7
0m7700:	107700	002401	063726	006700	017742	007306	027713	002006
0m7710:	027703	102077	027700	077754	017742	017742	074000	077757
0m7720:	067757	047755	002040	027740	017742	040001	177757	037757
0m7730:	000040	037754	027720	017742	054000	027702	102011	027700
0m7740:	102055	027700	dddddd	006600	1037cc	1023cc	027745	1074cc
0m7750:	002041	127742	005767	027744	dddddd	1n0100	0200zz	dddddd
0m7760:	107700	063756	102606	002700	1026qq	001500	102602	063777
0m7770:	102702	102602	103706	1027zz	067776	074077	024077	177700

Variables

- cc = punched tape reader or teleprinter address
- dddddd = indeterminable (Load all zeros in memory locations designated "indeterminable" when loading. Disregard as insignificant the content of memory locations designated as "indeterminable" when verifying.)
- m = 1 for 8K, 3 for 16K, 5 for 24K, 7 for 32K memory
- n = 6 for 8K, 4 for 16K, 2 for 24K, 0 for 32K memory
- zz = first disc channel
- qq = second disc channel

LOADING PROCEDURE

To load into the protected area of memory, refer to the applicable listing and proceed as follows:

Note

Be sure to use proper values for all variables specified in the listing.

a. Set LOADER switch to ENABLED.

b. Enter the address of the word to be loaded into the SWITCH REGISTER.

c. Press and release LOAD ADDRESS switch.

d. Enter the instruction into the SWITCH REGISTER.

e. Press and release LOAD MEMORY switch.

f. Repeat steps "b" thru "e" for each instruction loaded. (Steps "b" and "c" can be omitted when loading into consecutive memory locations.)

g. Set the LOADER switch to PROTECTED after all desired instructions have been loaded.

VERIFICATION PROCEDURE

To verify the contents of the protected area of memory, refer to the applicable listing above and proceed as follows:

a. Enter address of location to be verified into the SWITCH REGISTER.

b. Press and release LOAD ADDRESS switch.

c. Set LOADER switch to ENABLED.

d. Press and release DISPLAY MEMORY switch. The content of the memory location selected in step "a" above is now indicated by the T-REGISTER MEMORY DATA display. Each time the DISPLAY MEMORY switch is pressed and released, the content of the next consecutive memory location is displayed. Because the M-register is incremented by one each time the DISPLAY MEMORY switch is pressed, the address indicated by the M-REGISTER MEMORY ADDRESS display is always one address higher than the address of the data currently displayed by the T-REGISTER indicators.

e. Set the LOADER switch to PROTECTED after all desired locations have been displayed.

f. Select the desired tape reading option from table 4-4 and set SWITCH REGISTER switches 0 and 15 accordingly. (For the program to be read from the tape and loaded into memory, the "load tape" option must be selected by positioning switches 0 and 15 to "0" (down). If the verify checksum or compare options are selected, the program on the tape will be read, but will not be loaded into memory. Note that the BBDL loader program is not capable of performing the "verify checksum" and "compare" options. Therefore, if the BBDL loader program rather than the BBL loader program is residing in the protected area of memory, the "load tape" option is the only option available and must be selected.)

Table 4-4. Tape Reading Options

OPTION	SWITCH REGISTER SETTING	
	BIT 15	BIT 0
Load tape (reads tape and loads contents into memory)	0	0
*Verify checksum (reads tape without loading)	0	1
*Compare the contents of the tape with the contents of memory (reads tape without loading)	1	0/1

*Selectable only in configurations using the HP 2748A or 2758A Punched Tape Reader in conjunction with the BBL loader program.

g. Set the LOADER switch to ENABLED. Then, in turn, press the PRESET and RUN switches. The computer should go into the run mode (RUN indicator on) while the program tape processes through the tape reader. When the computer halts (RUN indicator off; HALT indicator on), set the LOADER switch to PROTECTED and check the T-REGISTER MEMORY DATA indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to paragraph 4-33 and table 4-5.) If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-5 and proceed as directed.

Note

If the paper tape is ejected from the tape reader and the computer does not halt after the tape is read, press and release the HALT switch on the computer front panel. Then check the loader program in the protected area of memory according to the procedure given in table 4-3. If the contents of the protected memory locations are correct, refer to paragraph 4-392 and troubleshoot the circuits associated with the halt instruction. If the halt circuits are not the cause of the trouble, refer to the manuals for the tape reader and the tape-reader interface and troubleshoot accordingly.

h. At the tape reader, press the LOAD switch to remove the tape from the unit. Then rewind the tape and return it to its storage box.

4-31. LOADING DIAGNOSTIC TAPES WITH THE HP 2758A TAPE READER-REROLLER. The procedure for using the tape reader-reroller to load programs from punched paper tapes is as follows:

a. At the tape reader-reroller, press the POWER switch to energize the unit.

b. Press the LOAD switch to release the reader pinch roller.

c. Thread the tape through the tape reader as instructed in the 2758A Tape Reader-Reroller Operating and Service Manual (manual part no. 02758-90173).

d. Press the READ switch. (The tape reader is now ready to read the tape.)

Note

To configure the address specified in step "e" following replace the variable "m" in the starting address with the number corresponding to the size of computer memory (i.e., 1 for 8K, 3 for 16K, 5 for 24K, or 7 for 32K).

e. At the computer front panel, press the HALT switch. (The HALT indicator should now be on, and the RUN indicator should be off.) Enter 0m7700 (the starting address of the loader program stored in the protected area of memory) into the SWITCH REGISTER and press the LOAD ADDRESS switch.

f. Select the desired tape reading option from table 4-4 and set SWITCH REGISTER switches 0 and 15 accordingly. (For the program to be read from the tape and loaded into memory, the "load tape" option must be selected by positioning switches 0 and 15 to "0" (down). If the verify checksum or compare options are selected, the program on the tape will be read, but will not be loaded into memory. Note that the BBDL loader program is not capable of performing the "verify checksum" and "compare" options. Therefore, if the BBDL loader program rather than the BBL loader program is residing in the protected area of memory, the "load tape" option is the only option available and must be selected.)

g. Set the LOADER switch to ENABLED. then, in turn, press the PRESET and RUN switches. The Computer should go into the run mode (RUN indicator on) while the program tape processes through the tape reader. When the

computer halts (RUN indicator off; HALT indicator on), set the LOADER switch to PROTECTED and check the T-REGISTER MEMORY DATA indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to paragraph 4-33 and table 4-5.) If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-5 and proceed as directed.

Note

If the paper tape is ejected from the tape reader and the computer does not halt after the tape is read, press and release the HALT switch on the computer front panel. Then check the loader program in the protected area of memory according to the procedure given in table 4-3. If the contents of the protected memory locations are correct, refer to paragraph 4-392 and troubleshoot the circuitry associated with the halt instruction. If the halt circuits are not the cause of the trouble, refer to the manuals for the tape reader and the tape-reader interface and troubleshooting accordingly.

h. At the tape reader, press the LOAD switch to remove the tape from the unit. Then return the tape to its storage box.

4-32. LOADING DIAGNOSTIC TAPES USING THE HP 2752A TELEPRINTER. The procedure for using the teleprinter tape reader to load programs from punched paper tapes is as follows:

a. At the teleprinter, set the LINE/OFF/LOCAL switch to LINE.

Table 4-5. Loading Halts

T-REGISTER MEMORY DATA DISPLAY	EXPLANATION	REQUIRED ACTION
102077	End-of-tape. Ten consecutive feed frames have been detected and interpreted as an end-of-tape condition.	This indication is normal. Proceed with the applicable procedure for running the program which was loaded into the computer memory.
102011	Checksum error. The A-register contains the checksum from the tape. The B-register contains the computed checksum.	Using the procedures given in paragraphs 4-29 through 4-32, as applicable, reload the program into computer memory. Then execute the checksum option again. If a checksum error still occurs, check the program and/or the computer for the cause of the error.
102055	Address error. An attempt has been made to destroy the loader program, or to load outside the memory limits.	Using the procedures given in paragraphs 4-29 through 4-32, as applicable, recheck all steps and attempt to load the program again. If an address error still occurs, check the program and/or the computer for the cause of the error.
102000	Compare error. The tape being read does not compare with memory. The A-register contains the word from the tape which did not agree.	To find the address of the word in memory which did not compare with the word in the A-register, press the SINGLE CYCLE switch twice. The contents of the T-register, minus one, is the address of the word. Using the procedures given in paragraphs 4-29 through 4-32, as applicable, reload the program into computer memory. Then execute the compare option again. If a compare error still occurs, check the program and/or the computer for the cause of the error.

b. Carefully position the program tape in the teleprinter tape reader.

c. Set the START/STOP/FREE switch to START. (The tape reader is now ready to read the tape.)

Note

To configure the address specified in step "d" following, replace the variable "m" in the starting address with the number corresponding to the size of the computer memory (i.e., 1 for 8K, 3 for 16K, 5 for 24K, or 7 for 32K).

d. At the computer front panel, press the HALT switch. (The HALT indicator should now be on, and the RUN indicator should be off.) Enter 0m7700 (the starting address of the loader program stored in the protected area of memory) into the SWITCH REGISTER and press the LOAD ADDRESS switch.

e. Ensure that SWITCH REGISTER switches 0 and 15 are set to the "0" (down) position. Positioning switches 0 and 15 to "0" selects the "load tape" option. The "verify checksum" and "compare" options specified in table 4-4 cannot be performed using the teleprinter tape reader.

f. Set the LOADER switch to ENABLED. Then, in turn, press the PRESET and RUN switches. The computer should go into the run mode (RUN indicator on) while the program tape processes through the tape reader. When the computer halts (RUN indicator off; HALT indicator on), set the LOADER switch to PROTECTED and check the T-REGISTER MEMORY DATA indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to paragraph 4-33 and table 4-5). If the indication is normal, proceed with the applicable instructions for running the program now in memory. If the indication is abnormal, refer to table 4-5 and proceed as directed.

Note

If the paper tape is ejected from the tape reader and the computer does not halt after the tape is read, manually press and release the HALT switch on the computer front panel. Then check the loader program in the protected area of memory according to the procedure given in table 4-3. If the contents of the protected memory locations are correct, refer to paragraph 4-392 and troubleshoot the circuits associated with the halt instruction. If the halt circuits are not the cause of the trouble, refer to the manuals for the teleprinter and teleprinter interface and troubleshoot accordingly.

g. At the teleprinter, set the START/STOP/FREE switch to STOP, remove the tape from the reader, rewind, and return it to its storage box.

4-33. LOADING HALTS. After all program data is read from a test tape and transferred into memory, the associated tape reader and the computer will halt with a normal indication of 102077 (end-of-tape condition) displayed by the T-REGISTER MEMORY DATA indicators. This signals the operator to continue with the applicable procedure for running the program now stored in memory. If a halt occurs while a tape is being loaded and an indication other than 102077 is displayed, refer to table 4-5 and proceed as directed.

4-34. TROUBLESHOOTING REFERENCE INFORMATION.

4-35. GENERAL.

4-36. Troubleshooting information consists of circuit descriptions, test procedures, diagrams, and other reference material required during trouble analysis and repair. Effective use of this information aids the user in isolating the trouble to a faulty circuit function, locating the defective assembly, subassembly, or part, making the required repair, and preparing the computer for return to service.

4-37. The purpose and use of the troubleshooting information found in this section, consisting of the items listed below, is explained in paragraphs 4-39 through 4-53.

a. A diagram showing machine-language formats for the basic instruction set.

b. An alphabetical listing of program instructions which includes troubleshooting references for associated circuit functions.

c. Circuit descriptions and test procedures.

d. Troubleshooting diagrams.

4-38. Troubleshooting information found in other sections of this manual, and in other manuals included in the computer documentation, is discussed in paragraphs 4-54 through 4-59.

4-39. PROGRAM INSTRUCTION FORMATS.

4-40. Program instruction formats are shown in figure 4-1. This figure summarizes information needed for using machine language to program the computer. Bit patterns are shown for the basic instruction set which is comprised of memory reference instructions, input/output instructions, register reference instructions in the shift-rotate group (SRG), and register reference instructions in the alter-skip group (ASG).

4-41. For additional information pertaining to computer machine-language, refer to Volume One, the Specifications and Basic Operation Manual (manual part no. 02116-91755).

4-42. LIST OF PROGRAM INSTRUCTIONS AND TROUBLESHOOTING REFERENCES.

4-43. A list of program instructions and troubleshooting references is presented in table 4-6. This table lists, alphabetically, by mnemonic, the instructions comprising the basic instruction set for the computer. The main purpose of this table is to provide references to the circuit-level troubleshooting data within this section of the manual that applies to the instructions listed. Type, definition, and a brief descriptive summary is given for each instruction.

4-44. For additional information on each instruction, refer to Volume One, the Specifications and Basic Operation Manual (manual part no. 02116-91755). For detailed information at the circuit level, refer to the paragraph and figure listed in the "REFERENCES" column of table 4-6.

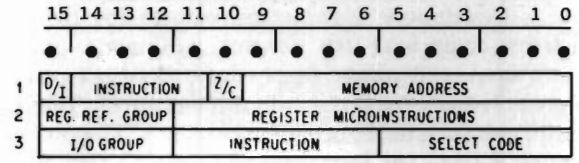
4-45. CIRCUIT DESCRIPTIONS AND TEST PROCEDURES.

4-46. Descriptions and test procedures for the circuit functions comprising the control, arithmetic, memory, input/output, and power supply sections of the computer are presented in paragraphs 4-60 through 4-517. The circuit descriptions include information which is helpful during troubleshooting. The test procedures include test data and suggested test methods which can be used to substantiate or disclaim that the circuit under test is the cause of the trouble.

4-47. In the event that the circuit under test is not the cause of the trouble, references are provided to troubleshooting data for related circuit functions which could cause the trouble symptom. If it is determined that the circuit under test is the cause of the trouble, use of the troubleshooting diagrams in this section, together with the detailed schematic diagrams, parts location diagrams, equations, and interconnection and wiring information in section VII will provide the additional data needed to isolate the trouble to a replaceable or repairable assembly or part.

(Text continues on page 4-22.)

BASIC INSTRUCTION FORMATS



1 MEMORY REFERENCE INSTRUCTIONS
2 REGISTER REFERENCE INSTRUCTIONS
3 INPUT/OUTPUT INSTRUCTIONS

BASIC INSTRUCTION SET

TYPE	MNEMONIC	DESCRIPTION
Memory Reference	AND	"And" (M) to A; result in A
	XOR	"Exclusive or" (M) to A; result in A
	IOR	"Inclusive or" (M) to A; result in A
	JSB	Jump to subroutine, save P
	JMP	Jump, unconditionally
	ISZ	Increment (M); skip if result zero
	ADA/B	Add (M) to A or B; result in A or B
	CPA/B	Compare (M) with A or B; skip if unequal
	LDA/B	Load (M) into A or B
	STA/B	Store A or B into M; A/B unchanged
Register Reference		SHIFT-ROTATE GROUP
	NOP	No operation
	CLE	Clear E (Extend)
	SLA/B	Skip if least significant bit of A/B is zero
	A/BLS	A/B arithmetic left shift one bit
	A/BRS	A/B arithmetic right shift one bit
	RA/BL	Rotate A/B left one bit
	RA/BR	Rotate A/B right one bit
	A/BLR	A/B left shift one bit, sign cleared
	ERA/B	Rotate E right one bit with A or B
	ELA/B	Rotate E left one bit with A or B
	A/BLF	Rotate A or B left four bits
		ALTER-SKIP GROUP
	CLA/B	Clear A or B
	CMA/B	Complement A/B (ones complement)
	CCA/B	Clear-complement A/B (set to -1)
	CLE	Clear E (Extend)
	CME	Complement E
	CCE	Clear-complement E (set E)
	SEZ	Skip if E is zero
	SSA/B	Skip if sign of A/B is zero (positive)
	SLA/B	Skip if least significant bit of A/B is zero
	INA/B	Increment A/B by one
	SZA/B	Skip if A/B is zero
	RSS	Reverse skip sense
Input/ Output		OVERFLOW
	STO	Set overflow bit
	CLO	Clear overflow bit
	SOC	Skip if overflow bit clear
	SOS	Skip if overflow bit set
	HLT	Halt program
	STF	Set flag bit of selected I/O channel
	CLF	Clear flag of selected I/O channel
	SFC	Skip if flag clear
	SFS	Skip if flag set
	MIA/B	Merge ("or") I/O channel into A/B
	LIA/B	Load I/O channel into A/B
	OTA/B	Output A/B to I/O channel
	STC	Set control bit of selected channel
	CLC	Clear control bit of selected channel

- (M) = Contents of Memory Location M
- Overflow instructions are coded under I/O group

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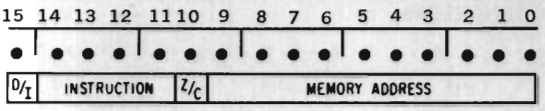
MEMORY REFERENCE INSTRUCTIONS



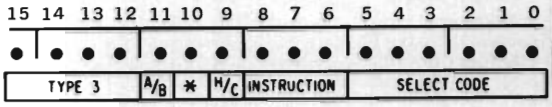
AND	0	0	1	0
XOR	0	1	0	0
IOR	0	1	1	0
JSB	0	0	1	1
JMP	0	1	0	1
ISZ	0	1	1	1
ADA	1	0	0	0
ADB	1	0	0	1
CPA	1	0	1	0
CPB	1	0	1	1
LDA	1	1	0	0
LDB	1	1	0	1
STA	1	1	1	0
TB	1	1	1	1

TRUTH TABLE

	AND	XOR	IOR
A Contents	0 0 1 1	0 0 1 1	0 0 1 1
Memory	0 1 0 1	0 1 0 1	0 1 0 1
Result (in A)	0 0 0 1	0 1 1 0	0 1 1 1

1 = True, 0 = False

INPUT/OUTPUT INSTRUCTIONS



MAC	1	0	0	0		0										
HLT	1	0	0	0		1	†	0	0	0						
STF	1	0	0	0		1	0	0	0	1						
CLF	1	0	0	0		1	1	0	0	1						
SFC	1	0	0	0		1	0	0	1	0						
SFS	1	0	0	0		1	0	0	1	1						
MIA	1	0	0	0	0	1	†	1	0	0						
MIB	1	0	0	0	1	1	†	1	0	0						
LIA	1	0	0	0	0	1	†	1	0	1						
LIB	1	0	0	0	1	1	†	1	0	1						
OTA	1	0	0	0	0	1	†	1	1	0						
OTB	1	0	0	0	1	1	†	1	1	0						
STC	1	0	0	0	0	1	†	1	1	1						
CLC	1	0	0	0	1	1	†	1	1	1						
STO	1	0	0	0		1	0	0	0	1	0	0	0	0	0	1
CLO	1	0	0	0		1	1	0	0	1	0	0	0	0	0	1
SOC	1	0	0	0		1	†	0	1	0	0	0	0	0	0	1
SOS	1	0	0	0		1	†	0	1	1	0	0	0	0	0	1

*Macroinstruction if "0"; standard I/O instruction if "1".
†Clear Flag FF if "0", hold if "1".

Figure 4-1. Program Instruction Formats (Sheet 1 of 2)

Register Reference Instructions (Shift-Rotate Group)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE 2				A/B	0	D/E	COL 1			2	D/E	3	COL 4		
NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CLE	0	0	0	0		0					1					
SLA	0	0	0	0	0	0							1			
SLB	0	0	0	0	1	0							1			
ALS	0	0	0	0	0	0	1	0	0	0		X		X	X	X
BLS	0	0	0	0	1	0	1	0	0	0		X		X	X	X
ARS	0	0	0	0	0	0	1	0	0	1		X		X	X	X
BRS	0	0	0	0	1	0	1	0	0	1		X		X	X	X
RAL	0	0	0	0	0	0	1	0	1	0		X		X	X	X
RBL	0	0	0	0	1	0	1	0	1	0		X		X	X	X
RAR	0	0	0	0	0	0	1	0	1	1		X		X	X	X
RBR	0	0	0	0	1	0	1	0	1	1		X		X	X	X
ALR	0	0	0	0	0	0	1	1	0	0		X		X	X	X
BLR	0	0	0	0	1	0	1	1	0	0		X		X	X	X
ERA	0	0	0	0	0	0	1	1	0	1		X		X	X	X
ERB	0	0	0	0	1	0	1	1	0	1		X		X	X	X
ELA	0	0	0	0	0	0	1	1	1	0		X		X	X	X
ELB	0	0	0	0	1	0	1	1	1	0		X		X	X	X
ALF	0	0	0	0	0	0	1	1	1	1		X		X	X	X
BLF	0	0	0	0	1	0	1	1	1	1		X		X	X	X

SELECTION TABLE

1	2	3	4
ALS ARS RAL RAR ALR ERA ELA ALF	CLE	SLA	ALS ARS RAL RAR ALR ERA ELA ALF
BLS BRS RBL RBR BLR ERB ELB BLF	CLE	SLB	BLS BRS RBL RBR BLR ERB ELB BLF

COMBINING GUIDE

1. Choose up to 4 instructions, one from each column of the Selection Table.
2. Use a one-bit for Bit 9 to Enable column 1 instructions, and a one-bit for Bit 4 to Enable column 4 instructions. Figure above shows column 1 enabled (executed first) with duplicate column 4 pattern (executed last) indicated by X's.
3. Use a one-bit for Bit 5 to select column 2 (CLE), or a zero-bit to exclude CLE.
4. Use a one-bit for Bit 3 to select column 3 (SLA/B), or a zero-bit to exclude SLA/B.

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Register Reference Instructions (Alter-Skip Group)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE 2				A/B	1	COL 1		COL. 3		2	4	5	6	7	8
CLA	0	0	0	0	0	1	0	1								
CLB	0	0	0	0	1	1	0	1								
CMA	0	0	0	0	0	1	1	0								
CMB	0	0	0	0	1	1	1	0								
CCA	0	0	0	0	0	1	1	1								
CCB	0	0	0	0	1	1	1	1								
SEZ	0	0	0	0		1					1					
CLE	0	0	0	0		1			0	1						
CME	0	0	0	0		1			1	0						
CCE	0	0	0	0		1			1	1						
SSA	0	0	0	0	0	1						1				
SSB	0	0	0	0	1	1						1				
SLA	0	0	0	0	0	1							1			
SLB	0	0	0	0	1	1							1			
INA	0	0	0	0	0	1								1		
INB	0	0	0	0	1	1								1		
SZA	0	0	0	0	0	1									1	
SZB	0	0	0	0	1	1									1	
RSS	0	0	0	0		1										1

SELECTION TABLE

1	2	3	4	5	6	7	8
CLA CMA CCA	SEZ	CLE CME CCE	SSA	SLA	INA	SZA	RSS
CLB CMB CCB	SEZ	CLE CME CCE	SSB	SLB	INB	SZB	RSS

COMBINING GUIDE

1. Choose up to 8 instructions, one from each column of the Selection Table.
2. Use the specified two-bit combinations of Bits 9 and 8, plus A/B Bit 11, to encode column 1 instructions.
3. Use the specified two-bit combinations of Bits 7 and 6 to encode column 3 instructions.
4. Use a one-bit in Bits 5, 4, 3, 2, 1, plus A/B Bit 11, to encode column 2, 4, 5, 6, 7 instructions respectively.
5. Use a one-bit for Bit 0 to encode column 8.

Figure 4-1. Program Instruction Formats (Sheet 2 of 2)

Table 4-6. Program Instruction Index and Troubleshooting Reference Guide

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA	FIGURE
ADA	Memory Reference	Add to A-register. The contents of the addressed memory location are added to the contents of the A-register. The sum is stored in the A-register, and the contents of the memory location are unaltered. The result of the addition may set the Extend FF or Overflow FF.	4-233	4-53
ADB	Memory Reference	Add to B-register. The contents of the addressed memory location are added to the contents of the B-register. The sum is stored in the B-register, and the contents of the memory location are unaltered. The result of the addition may set the Extend FF or Overflow FF.	4-233	4-53
ALF	Register Reference (SRG)	Rotate all A-register bits left four places. The bits in positions 15, 14, 13, and 12 are rotated around into bit positions 3, 2, 1, and 0, respectively. This is equivalent to four successive RAL instructions.	4-317	4-67
ALR	Register Reference (SRG)	Shift A-register bits 0 through 14 left one place, arithmetically, and clear the sign bit. Bit position 0 is cleared, and the bit shifted out of position 14 is lost. Bit position 15 (sign bit) is cleared.	4-299	4-64
ALS	Register Reference (SRG)	Shift A-register bits 0 through 14 left one place, arithmetically. Bit position 0 is cleared, and the bit shifted out of bit position 14 is lost. Bit position 15 (sign bit) is not affected.	4-275	4-60
AND	Memory Reference	"And" to A-register. The contents of the addressed memory location are logically "anded" to the contents of the A-register. The result is stored in the A-register, and the contents of the memory location are unaltered.	4-195	4-47
ARS	Register Reference (SRG)	Shift A-register bits 0 through 15 right one place, arithmetically. The bit shifted out of position 0 is lost. The bit value of position 15 (sign bit) is shifted into position 14, but the bit in position 15 is unaltered.	4-281	4-61
BLF	Register Reference (SRG)	Rotate all B-register bits left four places. The bits in positions 15, 14, 13, and 12 are rotated around into bit positions 3, 2, 1, and 0, respectively. This is equivalent to four successive RAL instructions.	4-317	4-67
BLR	Register Reference (SRG)	Shift B-register bits 0 through 14 left one place, arithmetically, and clear the sign bit. Bit position 0 is cleared, and the bit shifted out of position 14 is lost. Bit position 15 (sign bit) is cleared.	4-299	4-64
BLS	Register Reference (SRG)	Shift B-register bits 0 through 14 left one place, arithmetically. Bit position 0 is cleared, and the bit shifted out of bit position 14 is lost. Bit position 15 (sign bit) is not affected.	4-275	4-60
BRS	Register Reference (SRG)	Shift B-register bits 0 through 15 right one place, arithmetically. The bit shifted out of position 0 is lost. The bit value of position 15 (sign bit) is shifted into position 14, but the bit in position 15 is unaltered.	4-281	4-61

Table 4-6. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA	FIGURE
CCA	Register Reference (ASG)	Clear then complement A-Register. Clears all 16 bit positions to zeros and then loads ones in all 16 bit positions. (This is the two's complement form of -1).	4-333	4-70
CCB	Register Reference (ASG)	Clear then complement B-register. Clears all 16 bit positions to zeros and then loads ones in all 16 bit positions. (This is the two's complement form of -1).	4-333	4-70
CCE	Register Reference (ASG)	Clear then complement E-register. Clears and then sets the Extend FF.	4-349	4-73
CLA	Register Reference (ASG)	Clear A-register. Clears all 16 bit position to zero.	4-323	4-68
CLB	Register Reference (ASG)	Clear B-register. Clears all 16 bit positions to zero.	4-323	4-57
CLC	Input/Output	Clear control bit on the I/O channel addressed by the select code. Clears the Control FF on the interface card residing in the addressed I/O channel to prevent the external device from interrupting. A CLC instruction addressed to select code 00 (octal) clears all Control FFs, effectively inhibiting all external devices from interrupting. A CLF instruction (see below) can be combined with the CLC instruction.	4-436	4-87
CLE	Register Reference (SRG and ASG)	Clear E-register. Clears the Extend FF.	4-264 and 4-339	4-58 and 4-71
CLF	Input/Output	Clear flag bit on the I/O channel addressed by the select code. Clears the Flag FF on the interface card residing in the addressed I/O channel to permit the external device to send a flag signal when ready. A CLF instruction addressed to select code 00 (octal) clears the Interrupt System Enable FF to disable the entire interrupt system, but does not effect the status of the Flag FFs on the individual interface cards.	4-403	4-81
CLO	Input/Output	Clear overflow register. Clears the Overflow FF.	4-446	4-89
CMA	Register Reference (ASG)	Complement A-register. Reverses the state of all 16 bit positions.	4-328	4-69
CMB	Register Reference (ASG)	Complement B-register. Reverses the state of all 16 bit positions.	4-328	4-69

Table 4-6. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA	FIGURE
CME	Register Reference (ASG)	Complement E-register. Reverses the state of the Extend FF.	4-344	4-72
CPA	Memory Reference	Compare to A-register, skip if unequal. The contents of the addressed memory location are compared with the contents of the A-register. If the two 16-bit words are different, the P- and M-registers are incremented by two instead of one, and the next instruction in the program sequence is skipped. If the two words are identical, the P- and M-registers are incremented by one, and the program proceeds normally to the next instruction in sequence. The contents of neither the A-register nor the addressed memory location are altered.	4-239	4-54
CPB	Memory Reference	Compare to B-register, skip if unequal. The contents of the addressed memory location are compared with the contents of the B-register. If the two 16-bit words are different, the P- and M-registers are incremented by two instead of one, and the next instruction in the program sequence is skipped. If the two words are identical, the P- and M-registers are incremented by one, and the program proceeds normally to the next instruction in sequence. The contents of neither the A-register nor the addressed memory location are altered.	4-239	4-54
ELA	Register Reference (SRG)	Rotate E-register left with A-register, one place. The bit in position 15 of the A-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 0 of the A-register.	4-311	4-66
ELB	Register Reference (SRG)	Rotate E-register left with B-register, one place. The bit in position 15 of the B-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 0 of the B-register.	4-311	4-66
ERA	Register Reference (SRG)	Rotate E-register right with A-register, one place. The bit in position 0 of the A-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 15 of the A-register.	4-305	4-65
ERB	Register Reference (SRG)	Rotate E-register right with B-register, one place. The bit is position 0 of the B-register is rotated into the Extend FF. The Extend FF bit is rotated into bit position 15 of the B-register.	4-305	4-65
HLT	Input/Output	Halt. Stops the computer and holds or clears the Flag FF on the interface card residing in the addressed I/O channel. Execution of this instruction has the same effect as pressing the HALT switch (the HALT indicator goes on, all front panel control switches are enabled, and no interrupts can occur.) The HLT instruction word will be displayed in the T-register, and the P-register will indicate the halt memory location plus one.	4-392	4-79

Table 4-6. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA	FIGURE
INA	Register Reference (ASG)	Increment A-register by one. Steps the count held in the A-register by one. The result of this operation may set the Extend FF or Overflow FF.	4-372	4-77
INB	Register Reference (ASG)	Increment B-register by one. Steps the count held in the A-register by one. The result of this operation may set the Extend FF or Overflow FF.	4-372	4-77
IOR	Memory Reference	Inclusive "or" to A-register. The contents of the addressed memory location are combined with the contents of the A-register by an inclusive "or" logic operation. The result is stored in the A-register, and the contents of the addressed memory location are unaltered.	4-207	4-49
ISZ	Memory Reference	Increment and skip if zero. The count stored in the addressed memory location is stepped by one. If as a result of this operation the count in the memory location advances to zero, the P- and M-registers are incremented by two instead of one, and the next instruction in the program sequence is skipped. If the count in the memory location advances to some value other than zero, the P- and M-registers are incremented by one, and the program proceeds normally to the next instruction in sequence. Incrementing the A- and B-registers with this instruction has no effect on the Extend or Overflow FFs.	4-226	4-52
JMP	Memory Reference	Jump. Sets the P- and M-registers to the address contained in the instruction word. The next instruction read from memory will be from this memory location.	4-220	4-51
JSB	Memory Reference	Jump to subroutine. Execution of this instruction, located in memory location "P", causes program control to jump unconditionally to memory location "X" which is specified in the address portion of the JSB instruction. The contents of the P-register ("P") plus one is stored in "X" as the return address for the main program. The next instruction executed will be that contained in location "X + 1". A return to the main program sequence at "P + 1" can be achieved by a jump indirect through location "X".	4-213	4-50
LDA	Memory Reference	Load into A-register. The A-register is cleared and then loaded with the contents of the address memory location. The contents of the memory location are unaltered.	4-245	4-55
LDB	Memory Reference	Load into B-register. The B-register is cleared and then loaded with the contents of the address memory location. The contents of the memory location are unaltered.	4-245	4-55
LIA	Input/Output	Load input into A-register. The contents of the buffer register on the interface card residing in the addressed I/O channel are loaded into the A-register. Previous contents in the A-register are lost.	4-424	4-85

Table 4-6. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA	FIGURE
LIB	Input/Output	Load input into B-register. The contents of the buffer register on the interface card residing in the addressed I/O channel are loaded into the B-register. Previous contents in the B-register are lost.	4-424	4-85
MAC	Special	Macroinstruction. This instruction provides up to 2048 entries to macroinstruction subroutines. It is used only by special options and special software, and is not included as one of the instructions in the basic instruction set for the computer. The basic computer processes a MAC instruction in the same manner as a NOP instruction.	NA	NA
MIA	Input/Output	Merge input into A-register. The contents of the buffer register on the interface card residing in the addressed I/O channel are merged with the contents of the A-register by performing the inclusive "or" function. The results of the merger are stored in the A-register. The previous contents of the A-register are lost.	4-418	4-84
MIB	Input/Output	Merge input into B-register. The contents of the buffer register on the interface card residing in the addressed I/O channel are merged with the contents of the A-register by performing the inclusive "or" function. The results of the merger are stored in the B-register. The previous contents of the B-register are lost.	4-418	4-84
NOP	Register Reference (SRG)	No operation. No processing operation is performed. Only a memory cycle occurs.	4-259	4-57
OTA	Input/Output	Output from A-register. The contents of the A-register are loaded into the buffer register on the interface card residing in the addressed I/O channel. If the buffer register has less than 16 bit positions, the least significant bits from the A-register are normally loaded. The contents of the A-register remain unaltered.	4-430	4-86
OTB	Input/Output	Output from B-register. The contents of the B-register are loaded into the buffer register on the interface card residing in the addressed I/O channel, If the buffer register has less than 16 bit positions, the least significant bits from the B-register are normally loaded. The contents of the B-register remain unaltered.	4-430	4-86
RAL	Register Reference (SRG)	Rotate all A-register bits left one place. The bit in position 15 is rotated around to bit position 0.	4-287	4-62
RAR	Register Reference (SRG)	Rotate all A-register bits right one place. The bit in position 0 is rotated around to bit position 15.	4-293	4-63
RBL	Register Reference (SRG)	Rotate all B-register bits left one place. The bit in position 15 is rotated around to bit position 0.	4-287	4-62
RBR	Register Reference (SRG)	Rotate all B-register bits right one place. The bit in position 0 is rotated around to bit position 15.	4-293	4-63

Table 4-6. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA	FIGURE
RSS	Register Reference (ASG)	Reverse skip sense. When processed alone (not combined with any of the ASG skip instructions), this instruction causes an unconditional skip. When combined with one or more other ASG skip instructions (SEZ, SSA, SSB, SLA, SLB, SZA, or SZB), this instruction causes a skip if a non-zero condition is sensed. If the instruction word includes SSA/B and SLA/B, both bits (15 and 0) must be a logical 1 for the skip to occur. In all other cases a skip occurs if any non-zero condition is sensed.	4-384	NA
SEZ	Register Reference (ASG)	Skip if E-register is zero. The next instruction is skipped if the Extend FF is clear.	4-354	4-74
SFC	Input/Output	Skip if flag clear. The next instruction is skipped if the Flag FF on the interface card residing in the addressed I/O channel is clear. Checks the status of the Interrupt System Enable FF if select code 00 (octal) is used in the instruction word.	4-408	4-82
SFS	Input/Output	Skip if flag set. The next instruction is skipped if the Flag FF on the interface card residing in the addressed I/O channel is set. Checks the status of the Interrupt System Enable FF if select code 00 (octal) is used in the instruction word.	4-413	4-83
SLA	Register Reference (SRG and ASG)	Skip if least significant bit of the A-register is zero. The next instruction is skipped if the FF in bit position 0 is clear (an even number stored in the A-register).	4-269 and 4-366	4-59 and 4-76
SLB	Register Reference (SRG and ASG)	Skip if least significant bit of the B-register is zero. The next instruction is skipped if the FF in bit position 0 is clear (an even number stored in the B-register).	4-269 and 4-366	4-59 and 4-76
SOC	Input/Output	Skip if overflow register is clear. The next instruction is skipped if the Overflow FF is clear. The Overflow FF will be set or cleared following execution of this instruction, depending on the status of the H/C bit in the instruction word, whether a skip occurs or not.	4-451	4-90
SOS	Input/Output	Skip if overflow register is set. The next instruction is skipped if the Overflow FF is set. The Overflow FF will be set or cleared following execution of this instruction, depending on the status of the H/C bit in the instruction word, whether a skip occurs or not.	4-451	4-90
SSA	Register Reference (ASG)	Skip if sign bit of A-register is zero. The next instruction is skipped if the FF in bit position 15 (sign bit) is clear (positive).	4-360	4-75
SSB	Register Reference (ASG)	Skip if sign bit of B-register is zero. The next instruction is skipped if the FF in bit position 15 (sign bit) is clear (positive).	4-360	4-75

Table 4-6. Program Instruction Index and Troubleshooting Reference Guide (Continued)

INSTRUCTION		DEFINITION AND DESCRIPTION	REFERENCES	
MNEMONIC	TYPE		PARA	FIGURE
STA	Memory Reference	Store A-register contents. The contents of the A-register are stored in the addressed memory location. The prior contents of the memory location are lost, but the A-register contents are unaltered.	4-251	4-56
STB	Memory Reference	Store B-register contents. The contents of the B-register are stored in the addressed memory location. The prior contents of the memory location are lost, but the B-register contents are unaltered.	4-251	4-56
STC	Input/Output	Set control bit on the I/O channel addressed by the select code. Sets the Control FF on the interface card residing in the addressed I/O channel. This enables the external device to perform its input or output function, and its flag to interrupt the program.	4-436	4-87
STF	Input/Output	Set flag bit on the I/O channel addressed by the select code. Sets the Flag FF on the interface card residing in the addressed I/O channel. This causes an interrupt during the next machine cycle if the interrupt system is enabled, and if the Control FF on the interface card is set. A STF instruction addressed to select code 00 (octal) sets the Interrupt System Enable FF to enable the entire interrupt system.	4-398	4-80
STO	Input/Output	Set overflow register. Sets the Overflow FF.	4-441	4-88
SZA	Register Reference (ASG)	Skip if A-register is zero. The next instruction is skipped if the contents of the A-register are equal to zero (all 16 bit positions clear).	4-378	4-78
SZB	Register Reference (ASG)	Skip if B-register is zero. The next instruction is skipped if the contents of the B-register are equal to zero (all 16 bit positions clear).	4-378	4-78
XOR	Memory Reference	Exclusive "or" to A-register. The contents of the addressed memory location are combined with the contents of the A-register by an exclusive "or" logic operation. The result is stored in the A-register, and the contents of the addressed memory location are unaltered.	4-201	4-48

4-48. TROUBLESHOOTING DIAGRAMS.

4-49. The troubleshooting diagrams presented in figures 4-2 through 4-109 of this section consist of timing diagrams, waveforms, and servicing diagrams. The purpose and use of these diagrams is described in the following paragraphs.

4-50. TIMING DIAGRAMS. Timing diagrams are provided to show timing relationships between signals associated with a given circuit function. The timing diagram for the basic timing circuit (figure 4-15) is a typical example. The signals shown in timing diagrams are "idealized" (i.e., not shown as they would actually appear on an oscilloscope). This can be seen by comparing the 10 MHz oscillator output and time T0 signal as they are shown in figure 4-15 to the actual oscilloscope waveforms shown in figure 4-16.

4-51. WAVEFORM DIAGRAMS. Waveform diagrams are provided to show computer signals as they actually appear on an oscilloscope. The waveforms in figure 4-16 are a typical example. All waveforms in this manual were observed on an HP 180A Plug-in Oscilloscope Main Frame equipped with an HP 1801A Vertical Amplifier, an HP 1820A Time Base, and HP 10004A Miniature Resistive Divider Probes (10:1). Unless otherwise noted in the waveform diagram or in text, oscilloscope connections and settings are as specified in table 4-7.

Table 4-7. Oscilloscope Settings and Connections

Channel A:	
Input	As specified
Input coupling	DC
Polarity	Positive
Volts/cm	As specified
Channel B:	
Input	As specified
Input coupling	DC
Polarity	Positive
Volts/cm	As specified
Triggering:	
Mode	Internal
Source	Channel B
Slope	Positive
Coupling	DC
Display mode	Chopped
Time/cm	As specified
Magnification	x1
Graticule divisions	Centimeters

4-52. SERVICING DIAGRAMS. The servicing diagrams in this section include schematic diagrams, logic diagrams, and block diagrams that show signal flow and interconnections for a complete circuit function. The purpose of these diagrams is to provide the information needed at circuit level that will enable the user to localize a trouble symptom to a faulty assembly, and in some instances, isolate the trouble directly to the part that failed. Typical servicing diagrams are shown in figure 4-3, 4-47, and 4-103.

4-53. To undertsand and properly use the servicing block diagrams presented for the instruction processing circuits (figure 4-47 through 4-90), refer to figure 4-47 as a typical example and review the following information:

a. The signal flow and timing shown on each diagram is applicable to the phase during which the instruction is executed. Some instructions are executed during the fetch phase (phase 1), while others are executed during the execute phase (phase 3).

b. The timing and phase signals used in executing the instruction are shown extending from the block representing timing generator card A106. This block is located on the left side of each diagram.

c. The bit pattern for the instruction, as stored in the instruction register (I-register), is indicated in a separate block for instruction decoder card A107. This block is located in the top-left of each diagram.

d. Blocks representing the circuits that decode and process the instruction are grouped at the top-right of each diagram.

e. Blocks representing the circuits that increment the P- and M-registers are grouped at the bottom-right of each diagram.

f. Blocks representing the circuits that perform the memory operation which occurs when the instruction is processed are grouped at the left of each diagram.

g. Blocks, or groups of blocks, representing circuits that perform special operations during the processing of a given instruction are included on each diagram as required.

h. The "and" gate symbol, as used on these diagrams, indicates that the associated signals at the input of the symbol are logically combined in some manner to produce the signal at the output of the symbol, but are not necessarily "anded".

i. The numbers within the blocks and symbols, where the signal flow lines originate or terminate, correspond to the pins on the 86-pin connector of the associated plug-in card assembly.

j. An asterisk within a block or symbol denotes the termination of a signal flowing within the associated plug-in card assembly (i.e. the signal is not routed through the backplane to reach its destination).

k. The mnemonics on the signal flow lines are defined in section VII of this manual.

l. Equations for the signals shown are also given in section VII.

m. In the timing diagram presented in the lower-left corner, the signals shown are "idealized", as explained in paragraph 4-50. A vertical arrow pointing downward denotes a signal that is continuously false during the timing cycle. A vertical arrow pointing upward denotes a signal that is continuously true during the timing cycle. Some signals (i.e., SBO, RBO, etc.) are active at various times during the processing of an instruction. Only the conditions needed to execute the instruction are shown in the timing diagram. Data signals, and control signals that are active but perform no useful function during processing of a particular instruction, are not shown.

4-54. INFORMATION IN OTHER SECTIONS.

4-55. Information in other sections of this manual which may be required during troubleshooting includes:

a. Circuit descriptions and related diagrams presented in section III.

b. Preventive and corrective maintenance instructions presented in section V.

c. Replaceable parts tables and diagrams in section VI.

d. Detailed logic diagrams, schematic diagrams, parts location diagrams, wiring information, logic equations, and other tabular data presented in section VII.

4-56. Total familiarity with the content, purpose, and use of the information presented in these sections is recommended before attempting to troubleshoot or repair the computer.

4-57. INFORMATION IN OTHER MANUALS.

4-58. Information in other manuals which may be required for troubleshooting includes:

a. Reference information presented in Volume One, Specifications and Basic Operation (manual part no. 02116-91755).

b. General information concerning the input/output system presented in Volume Three, Input/Output System Operation (manual part no. 02116-91757).

c. Detailed documentation in the operating and service manuals for processor and interfacing options installed in the computer.

d. Diagnostic test procedures presented in the Manual of Diagnostics.

4-59. Familiarity with the content, purpose and use of the information presented in these manuals is recommended before attempting to troubleshoot or repair the computer.

4-60. CONTROL SECTION AND ARITHMETIC SECTION TROUBLESHOOTING.

4-61. GENERAL.

4-62. Troubleshooting the control and arithmetic sections of the computer consists of performing the basic checkout (paragraph 4-9) and the diagnostic checkout (paragraph 4-17) to test the overall operation of the circuits comprising these sections. Trouble symptoms encountered during the performance of the checkout procedures are used to determine which circuit function is most likely to be causing the trouble indication. References are then provided to applicable circuit level troubleshooting data for the suspected circuit function.

4-63. Troubleshooting data for the control and arithmetic sections consists of descriptions, test procedures, and troubleshooting diagrams for the following circuit functions:

a. Front panel switch and indicator circuits (paragraph 4-65).

b. Timing circuits (paragraph 4-151).

c. Phase logic circuits (paragraph 4-164).

d. A- and B-register addressing circuits (paragraph 4-187).

e. Memory reference instruction processing circuits (paragraph 4-193).

f. Register reference instruction processing circuits (paragraph 4-257).

g. Input/output instruction processing circuits (paragraph 4-390).

4-64. When troubleshooting these circuits, refer to sections V, VI, and VII of this manual for detailed schematic and logic diagrams, parts location diagrams, interconnection and wiring information, replaceable parts information, and corrective maintenance instructions.

4-65. FRONT PANEL SWITCH AND INDICATOR CIRCUITS.

4-66. Troubleshooting data for the circuits associated with the following switches and indicators are presented in the referenced paragraphs:

a. A- and B-REGISTER indicators (paragraphs 4-86 and 4-92).

b. DISPLAY MEMORY switch (paragraph 4-116).

c. EXECUTE indicator (paragraph 4-176).

d. EXTEND indicator (paragraphs 4-264, 4-339, and 4-372).

e. FETCH indicator (paragraph 4-167).

f. HALT switch and indicator (paragraph 4-76).

g. INDIRECT indicator (paragraph 4-171).

h. INSTRUCTION switch (paragraph 4-146).

i. LOAD A switch (paragraph 4-86).

j. LOAD ADDRESS switch (paragraph 4-98).

k. LOAD B switch (paragraph 4-92).

l. LOAD MEMORY switch (paragraph 4-106).

m. M-REGISTER indicators (paragraphs 4-98, 4-116, and 4-124).

n. MEMORY switch (paragraph 4-136).

o. OVERFLOW indicator (paragraphs 4-441 and 4-446).

p. P-REGISTER indicators (paragraphs 4-98, 4-116, and 4-124).

q. PARITY indicator (paragraph 4-67).

r. PHASE switch (paragraph 4-141).

s. POWER switch (paragraph 3-95) and POWER indicator (paragraph 3-95 and 4-68).

t. PRESET switch and indicator (paragraph 4-81).

u. RUN switch and indicator (paragraph 4-71).

v. SINGLE CYCLE switch (paragraph 4-124).

w. SWITCH REGISTER switches (paragraphs 4-86, 4-92, 4-98, and 4-106).

x. T-REGISTER indicators (paragraphs 4-106 and 4-116).

4-67. Use the operating and service manual for the HP 12591A Parity Error Option (manual part no. 12591-9001) to troubleshoot the circuits associated with the PARITY indicator.

4-68. POWER INDICATOR. The following paragraphs provide a description and test procedure for the circuits associated with POWER indicator DS109, mounted only on control panel assembly A502 of early 980- computers.

4-69. Description. The circuit for the POWER indicator is shown in figure 4-2. Indicator lamp DS109 is powered by the Power Indicator (PIND) signal at pin 49 of power fail interrupt card A6. Dropping resistor A6R4 is connected between the +12-volt dc supply and one side of the lamp filament. The other side of the lamp filament is connected to ground through terminal G on display board A501.

4-70. Test Procedure. Using a multi-function meter and the information presented in figure 4-2, proceed as follows:

a. Press the POWER switch to turn on power. Then check the +12-volt dc supply at A100TB2-1. If normal, proceed to step "b". If abnormal, refer to paragraph 4-508 and troubleshoot the power supply.

b. Press and release the POWER switch to turn off power. After checking to ensure that indicator lamp A502DS109 is not defective, make continuity and resistance checks of points between A501-G and A100TB2-1.

4-71. RUN SWITCH AND INDICATOR. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with RUN switch S107 and RUN indicator lamp DS107 which are located on control panel assembly A502.

4-72. Description. The circuits associated with the RUN switch and RUN indicator are shown in figure 4-3. The timing diagram included in this figure shows the sequential events that occur when the RUN switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the RUN and HALT switches are in the released position as shown.

4-73. The RUN switch is a momentary-action type switch. When pressed, it places +4.5 volts at pin 2 of A101MC65 (RNS FF) causing the output at pin 13 to go false. This false signal is felt at input pin 6. Input pin 7 of MC65 is false due to open contacts 1 and 3 of the pressed RUN switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal RNS at pin 44 of front panel coupler card A101. As long as the RUN switch is pressed, signal RNS remains true. When the RUN switch is released, +4.5 volts is transferred to input pin 7 of MC65 which causes output pin 9 to go false.

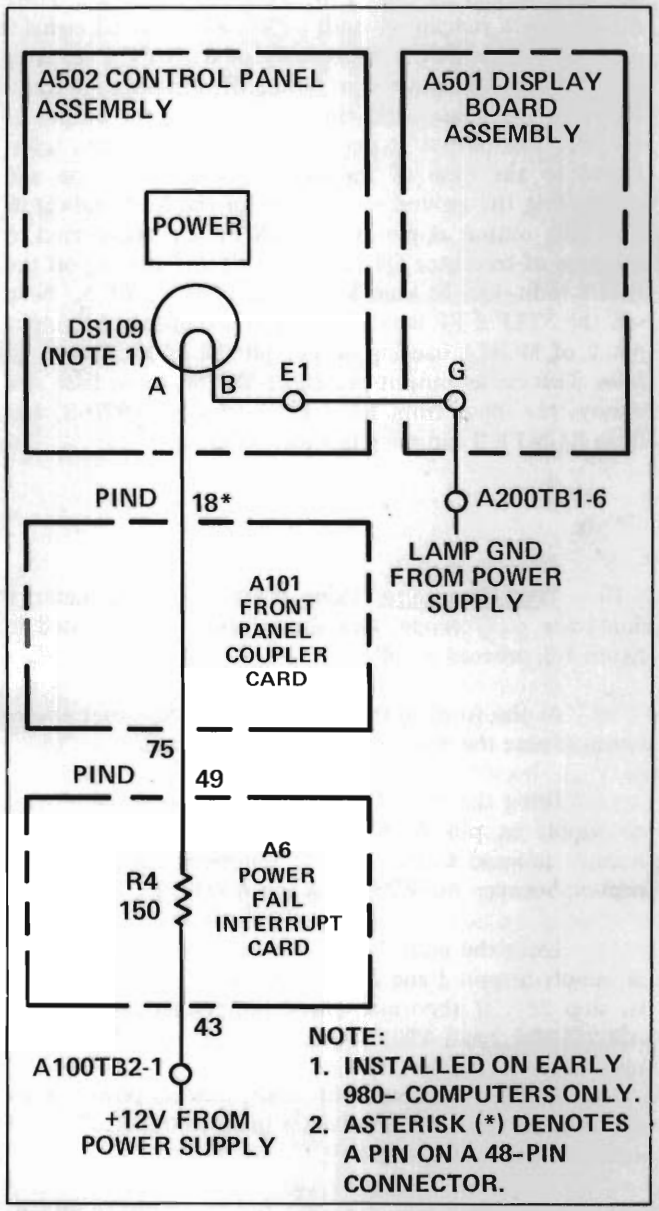

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Figure 4-2. POWER Indicator Circuit, Servicing Diagram

4-74. Signal RNS is transferred through pin 70 of timing generator card A106 to input pin 14 of "and" gate MC86D and input pin 6 of "and" gate MC76B. When signal RNS is true, output pin 13 of MC86D goes true. This true signal is transferred to pin 1 of STEP 1 FF MC94A. At the first time T2, the STEP 1 FF sets and remains set until the first time T2 after the RUN switch is released. The output at pin 13 of the STEP 1 FF is transferred to pin 7 of STEP 2 FF MC94B which sets at the next time T1 and remains set until the first time T1 after the RUN switch is released. The output of the STEP 1 FF is also transferred to input pin 9 of "and" gate MC76C. Input pin 7 of MC76C is held true at this time by "nor" gate MC87A. Thus, output pin 10 of MC76C goes true at time T2 and remains true until the following time T1 when STEP 2 FF sets (1.4 microseconds). This output is transferred through MC76B to input pin 14 of MC84 (RUN FF 1) and to input pin 14 of MC74 (RUN FF 2). At the end of time T5, RUN FF 1 will set. At the end of time T7S, RUN FF 2 will set. These flip-flops will remain set until a PRESET or HALT signal is received at pins 8 or 9 respectively of RUN FF 1 resetting this flip-flop. The outputs of both RUN flip-flops are transferred to the phase logic circuit along with the output of MC76C. The output at pin 13 of RUN FF 2 is also transferred to the base of transistor Q5 turning it on and completing the ground connection for the RUN indicator. The false output at pin 10 of RUN FF 2 is transferred to the base of transistor Q4 turning it off and turning off the HALT indicator. At time T1 after the STEP 1 FF has been set, the STEP 2 FF is set. Its output is transferred to input pin 2 of MC87A causing output pin 13 of MC87A to go false. This causes output pin 10 of MC76C to go false and remove the input from RUN FF 1 (through MC76B) and from RUN FF 2 and the phase logic circuits.

4-75. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-3, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +7-volt dc supply at pin A of RUN indicator A502DS107. If normal, proceed to step "c". If abnormal, check the connection between A502DS107-A and A501-(+).

c. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S107. If normal, proceed to step "d". If abnormal, check the connection between A502S107-1,2 and A101-39,40.

d. At the computer front panel, turn off power. After checking to ensure that indicator lamp A502DS107 is not defective, proceed to step "e".

e. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

f. At the computer front panel, turn on power.

g. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-70.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

h. At the computer front panel, press and hold the RUN switch and check the oscilloscope display for a logic 1 level. Then release the RUN switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A101MC65, A101MC83, and the RUN switch A502S107 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A106MC87-13.

j. At the computer front panel, press and hold the RUN switch and check the oscilloscope display for a logic 1 level. Then release the RUN switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check MC86D, STEP 1 FF MC94A, and STEP 2 FF MC94B as the most probable cause of trouble.

k. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10.1 probe).

(5) Channel A input: A206MC76-10.

(6) Channel B input: A106TP1 (time T0).

l. At the computer front panel, repeatedly press and release the RUN switch. After one machine cycle (1.6 μs) a pulse 1.4 μs in duration should be observed. If the oscilloscope display is normal, proceed to step "m". If the oscilloscope display is abnormal, check A106MC76C as the most probable cause of trouble.

m. Place the channel A oscilloscope probe on A106MC76-13. At the computer front panel, repeatedly press and release the RUN switch and check the oscilloscope display for a 1.4 μs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "n". If the oscilloscope display is abnormal, check A106MC76B as the most probable cause of trouble.

n. Place the channel A oscilloscope probe on A106MC84-13 (RUN FF 1). At the computer front panel, press and release the RUN switch and check the oscilloscope display for a logic 1 level. Then press and release the HALT switch and check the oscilloscope for a logic 0 level. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check pin 1 of MC84 for a 45 ηs to 55 ηs pulse occurring every 1.6 μs and pin 8 of MC84 for a logic 0 level. With the oscilloscope probe on pin 9 of MC84 press and release the HALT switch and check the oscilloscope display for a voltage level change from logic 0 to logic 1 back to logic 0. If the indication at pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If the indication at pin 8 is abnormal, refer to paragraph 4-81 and troubleshoot the circuits associated with the PRESET switch. If the indication at pin 9 is abnormal, refer to paragraph 4-76 and troubleshoot the circuits associated with the HALT switch.

o. Place the channel A oscilloscope probe on A106MC74-13 (RUN FF 2). At the computer front panel, press and release the RUN switch and check the oscilloscope display for a logic 1 level. Then press and release the HALT switch and check the oscilloscope for a logic 0 level. If the oscilloscope display is normal, proceed to step "p". If the oscilloscope display is abnormal, check pin 1 of MC74 for a 45 ηs to 55 ηs pulse occurring every 1.6 μs, and check pin 8 of MC74 for a logic 1 level. If the indication at pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If the indication at pin 8 is abnormal, check diode CR1 for an open condition.

p. Place the channel A oscilloscope probe on pin 7 of the 48-pin connector of A106 and check the oscilloscope display for a +7-volt level. At the computer front panel, press and release the RUN switch and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check transistor Q5 for an open or shorted condition.

q. At the computer front panel, turn off power.

r. Using a multi-function meter, check the line between pin 7 of cable 106 and RUN indicator A502DS107-B for continuity.

s. If all indications of the above test procedure are normal, the RUN switch and indicator circuits are operating normally.

4-76. HALT SWITCH AND INDICATOR. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with HALT switch S106 and HALT indicator lamp DS106 located on control panel assembly A502.

4-77. Description. The circuits associated with the HALT switch and HALT indicator are shown in figure 4-3. The timing diagram included in this figure shows the sequential events that occur when the HALT switch is pressed and released. In the following description it is assumed that initially RUN FF 1 and RUN FF 2 flip-flops are in the set condition, the RUN indicator is on, the HALT indicator is off, and the contacts of the RUN and HALT switches are in the released position as shown.

4-78. The HALT switch is a momentary-action type switch. When pressed, it places +4.5 volts through pins R and 54 of front panel coupler card A101 and pin 50 of timing generator card A106 to input pin 6 of HLS FF MC64 on the timing generator card. The output at pin 9 of MC64 will go false. This false signal is felt at input pin 2. Input pin 1 of MC64 is false due to open contacts 1 and 3 of the pressed HALT switch. Input pins 1 and 2 being false cause output pin 13 to go true. As long as the HALT switch is pressed, the output at pin 13 remains true. As soon as the HALT switch is released +4.5 volts is transferred to input pin 1 of MC64 which causes output pin 13 to go false.

4-79. The true condition at output pin 13 of MC64 is transferred to the direct reset input pin 9 of MC84 (RUN FF 1) causing its output pin 10 to go true. Output pin 10 of RUN FF 1 is connected through diode CR1 to the reset input pin 8 of MC74 (RUN FF 2) and at time T7S this flip-flop is reset. The outputs of both RUN flip-flops are transferred to the phase logic circuitry and by resetting these flip-flops no signals can be generated from the phase logic circuitry and all machine processing will stop. The output at pin 10 of RUN FF 2 is also transferred to the base of NPN transistor Q4 turning it on, completing the ground connection for the HALT indicator turning it on. The false output at pin 13 of RUN FF 2 is transferred to the base of transistor Q5 turning it off and turning off the RUN indicator.

4-80. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-3, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +7-volt dc supply at pin A of HALT indicator A502DS106. If normal, proceed to step "c". If abnormal, check the connection between A502DS106-A and A501-(+).

c. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of HALT switch A502S106. If normal, proceed to step "d". If abnormal, check the connection between A502S106-1,2 and A101-39,40.

d. At the computer front panel, turn off power. After checking to ensure that indicator lamp A502DS106 is not defective, proceed to step "e".

e. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

f. At the computer front panel, turn on power.

g. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-50.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

h. At the computer front panel, press and hold the HALT switch and check the oscilloscope display for a logic 1 level. Then release the HALT switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A101MC84, and the HALT switch A502S106 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A106MC64-13.

j. At the computer front panel, press and hold the HALT switch and check the oscilloscope display for a logic 1 level. Then releast the HALT switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check MC64 as the most probable cause of trouble.

k. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC84-10.

(6) Channel B input: A106TP1 (time T0).

l. At the computer front panel, press and release the RUN switch and check the oscilloscope display for a logic 0 level. Then press and release the HALT switch and check the oscilloscope for a logic 1 level. If the oscilloscope display is normal, proceed to step "m". If the oscilloscope display is abnormal, check A106MC84-1 for 200 ηs pulse occurring every 1.6 μs, check pin 8 for a logic 0 level, with the oscilloscope probe on A106MC84-14, repeatedly press and release the RUN switch and check the oscilloscope display for a 1.4 μs pulse occurring every 1.6 μs. If pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If pin 8 is abnormal, refer to paragraph 4-81 and troubleshoot the PRESET switch circuit. If pin 14 is abnormal, refer to paragraph 4-71 and troubleshoot the RUN switch circuits.

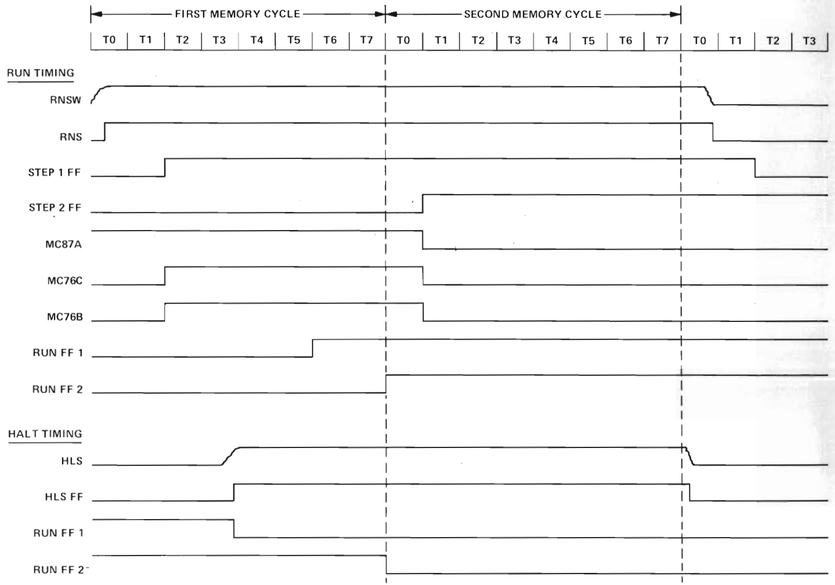
m. Place the oscilloscope probe on A106MC74-10 (RUN FF 2). At the computer front panel, press and release the RUN switch and check the oscilloscope display for a logic 0 level. Then press and release the HALT switch and check the oscilloscope for a logic 1 level. If the oscilloscope display is normal, proceed to step "n". If the oscilloscope display is abnormal, check A106MC74-1 for a 45 ηs to 55 ηs pulse occurring every 1.6 μs, and check pin 8 for a logic 1 level. If pin 1 is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits. If pin 8 is abnormal, check diode CR1 for an open condition.

n. Place the oscilloscope probe on pin 8 of the 48-pin connector of A106 and check the oscilloscope display for a logic 0 level. At the computer front panel, press and release the RUN switch and check the oscilloscope display for a +7-volt level. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check transistor Q4 for a shorted condition.

o. At the computer front panel, press and release the HALT switch and turn off power.

p. Using a multi-function meter, check the connection between pin 8 of cable 106 and the HALT indicator A502DS106-B for continuity.

q. If all indications of the above test procedure are normal, the HALT switch and indicator circuits are operating normally.



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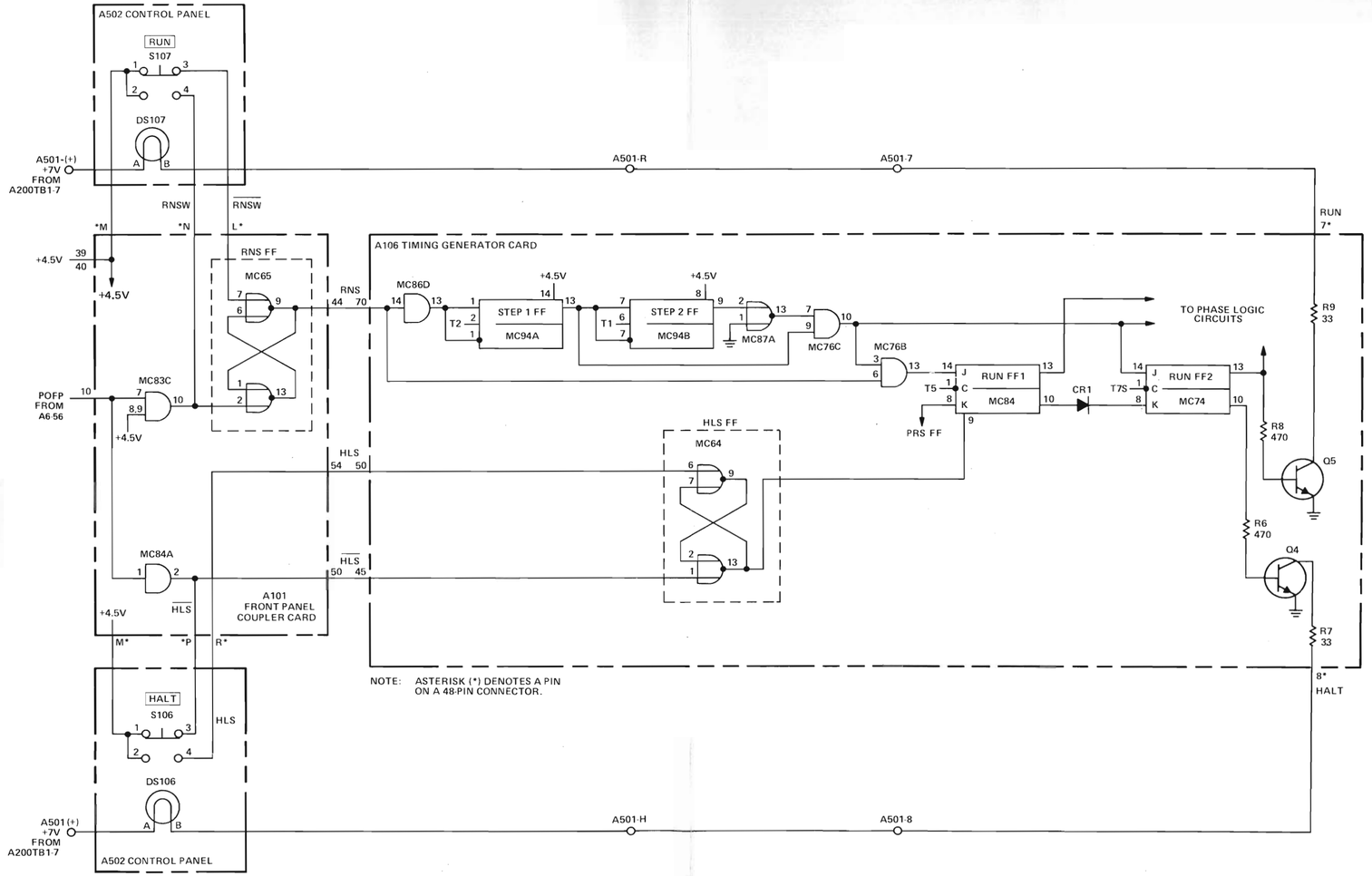


Figure 4-3. RUN and HALT Switch and Indicator Circuits, Servicing Diagram

4-81. PRESET SWITCH AND INDICATOR. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with PRESET switch S108 and PRESET indicator lamp DS108 located on control panel assembly A502.

4-82. Description. The circuits associated with the PRESET switch and PRESET indicator are shown in figure 4-4. The timing diagram included in this figure shows the sequential events that occur when the PRESET switch is pressed and released. In the following description it is assumed that initially all flip-flops except the PH1 flip-flop are in the reset condition, the PRESET indicator is on, the RUN indicator is off, the HALT indicator is on, the FETCH indicator can be off or on, and the contacts of the PRESET switch are in the released position as shown.

4-83. The PRESET switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin J of front panel coupler card A101 to pin 2 of "and" gate MC83A. The signal $\overline{RF2}$ is transferred to pin 1 of MC83A from RUN FF 2 reset output pin 10 on timing generator card A106. Therefore the machine must be in a halt mode for the PRESET switch to be effective. The signal PRS at output pin 14 of MC83A is transferred through pin 30 of the front panel coupler card, and pin 78 of power fail interrupt card A6, to input pin 6 of MC47 (FLAG FF) on the power fail interrupt card. With a true signal at input pin 6 of MC47, the FLAG FF is reset and output pin 9 will go false if input pin 1 of MC47 is false. This causes transistor Q1 of the power fail card to stop conducting and the PRESET indicator to go out.

4-84. Signal PRS is also transferred through pin 78 of timing generator card A106 to input pin 6 of MC115 (PRS FF) on the timing generator card. This causes output pin 9 of MC115 to go false. This false output is transferred to input pin 2 of MC115. Input pin 1 of MC115 is false due to open contacts 1 and 3 of the pressed PRESET switch. The two false inputs at pins 1 and 2 of MC115 cause output pin 13 to go true. This true output is transferred to input pin 14 of "and" gate MC114A and at time T5 causes the signal POPIO to be generated at output pin 13 of MC114A. This signal is transferred through pin 61 of the timing generator card to the I/O control card A201 where it conditions the I/O section for data transfer. The true output of MC115 is also transferred through the single input "and" gates MC106C and MC106A to the reset input pin 8 of MC84 (RUN FF1) to the direct reset pin 9 of MC74 (RUN FF 2) and through "and" gate MC53B to the set input pin 14 of MC44 (PH1 FF). This forces RUN FF 1 to be reset at the first time T5 after the PRESET switch is pressed, RUN FF 2 to be reset immediately assuring that the RUN indicator will be off and the HALT indicator will be on, and causing PH1 FF to be set if the PHASE switch (PNS) is in the NORM position, at the first time T7 and TS after the PRESET switch is pressed and turn on the FETCH indicator. Thus, pressing the PRESET switch will precondition the computer for phase 1 (FETCH phase) operation.

4-85. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-4, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +7-volt dc supply at pin A of PRESET indicator A502DS108. If normal, proceed to step "c". If abnormal, check the connection between A502DS108-A and A501-(+).

c. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S108. If normal, proceed to step "d". If abnormal, check the connection between A502S108-1,2 and A101-39,40.

d. At the computer front panel, turn off power. After checking to ensure that indicator lamp A502DS108 is not defective, proceed to step "e".

e. Using the extender card (part no. 02116-63216) extend power fail interrupt card A6 from the card cage.

f. At the computer front panel, turn on power.

g. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A6-78.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

h. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a logic 1 level. Then release the PRESET switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A101MC83 and the PRESET switch A502S108 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A6MC47-9.

j. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a logic 0 level. Then release the PRESET switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, refer to the power fail interrupt schematic and check MC47 and its input circuits as the most probable cause of trouble.

k. Place the channel A oscilloscope probe on the collector of transistor Q1 and check the oscilloscope display for a +7-volt level. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check transistor Q1 for a shorted condition, resistor R1 for an open condition, and the connection between A6-35 and A502DS108-B for continuity.

l. At the computer front panel, turn off power.

m. Using the extender card and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

n. At the computer front panel, turn on power.

o. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC115-13.

(6) Channel B input: A106TP1 (time T0).

p. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a logic 1 level. Then release the PRESET switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check MC115 (PRS FF) and the connection between A101-30 and A106-78 as the most probable causes of trouble.

q. Place the channel A oscilloscope probe on A106MC114-13. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a 200 ηs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check A106MC114-2 for the 200 ηs pulse above referred to. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

r. Place the channel A oscilloscope probe on A106MC84-8 (RUN FF 1). At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a logic 1 level. If the oscilloscope display is normal, proceed to step "s". If the oscilloscope display is abnormal, check A106MC106-9 in the same manner.

s. If, at this point in the test procedure, all checks have indicated normal operation but the RUN or HALT indicators are not off and on respectively, refer to paragraphs 4-71 and 4-76 and troubleshoot the RUN and HALT switches. If the checks have indicated normal operation and the RUN and HALT indicators are off and on respectively, proceed to step "t".

t. Place the channel A oscilloscope probe on A106MC-53-13. At the computer front panel, press and hold the PRESET switch and check the oscilloscope display for a logic 1 level. Then release the PRESET switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "u". If the oscilloscope display is abnormal, check A106MC53-6 for a +4.5-volt level.

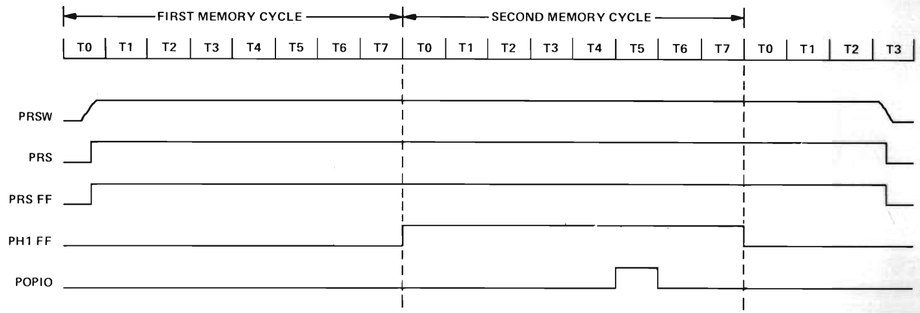
u. Place the channel A oscilloscope probe on A106MC-44-13 (PH1 FF) and check the oscilloscope display for a logic 1 level. If the oscilloscope display is normal, proceed to step "v". If the oscilloscope display is abnormal, check A106MC44-1 for a 45 ηs to 55 ηs pulse occurring every 1.6 μs and A106MC44-8 for a logic 0 level. If these pins are abnormal, refer to paragraphs 4-141 and 4-164 and the timing generator schematic and check the PHASE switch circuits, the phase logic circuits and A106MC35 as the most probable cause of trouble.

v. Place the channel A oscilloscope probe on the collector of transistor A106Q6 and check the oscilloscope display for a 0-volt level. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check transistor A106Q6 for an open condition.

w. At the computer front panel, turn off power.

x. Using a multi-function meter, check the line between pin 3 of cable 106 and the FETCH indicator A501DS84 and A501-(+) for continuity.

y. If all indications of the above test procedure are normal, the PRESET switch and indicator circuits are operating normally.



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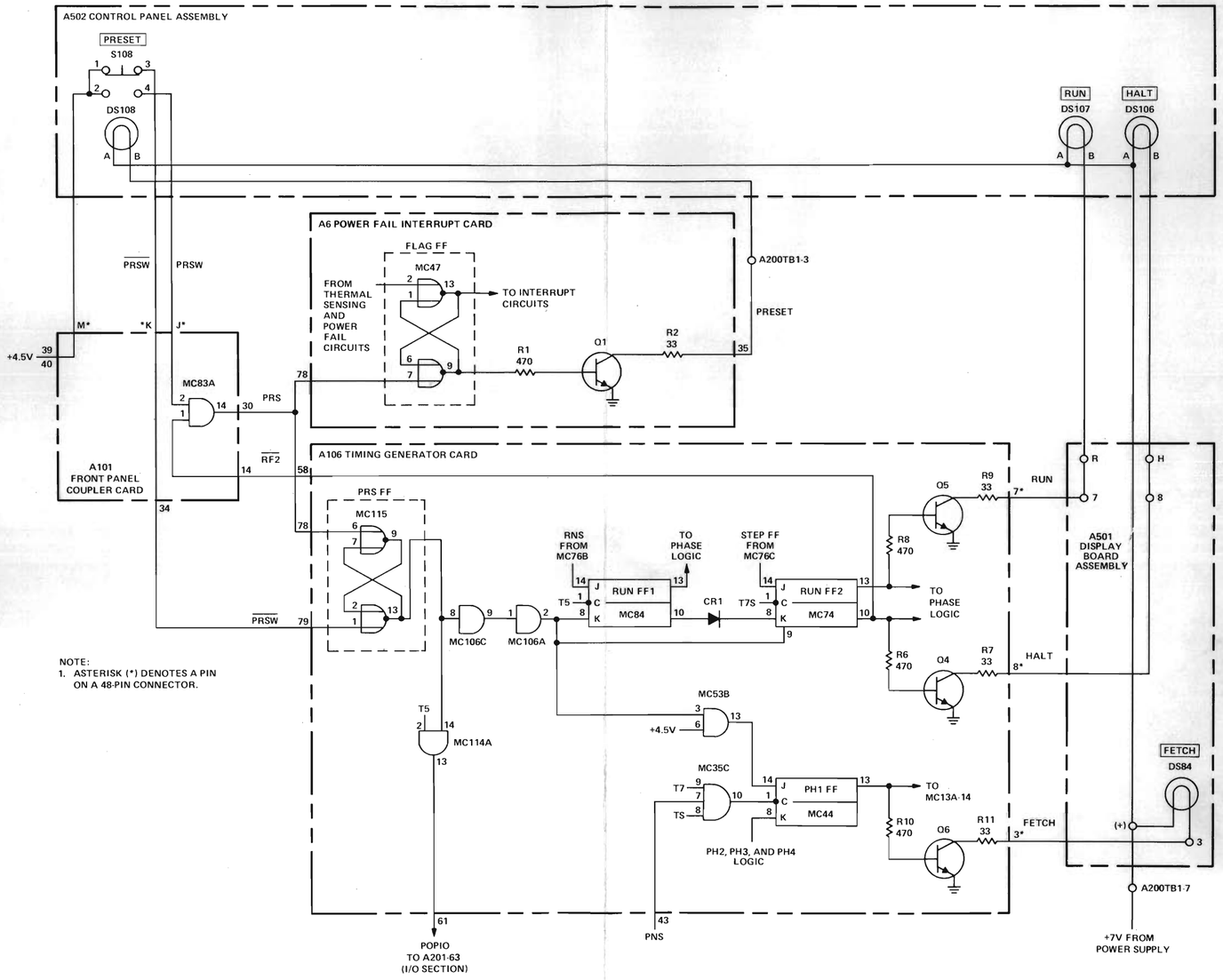


Figure 4-4. PRESET Switch and Indicator Circuit, Servicing Diagram

4-86. LOAD A SWITCH, A-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with LOAD A switch S104 and the SWITCH REGISTER switches located on control panel assembly A502, and the A-REGISTER indicators located on display board assembly A501.

4-87. Description. The circuits associated with the LOAD A switch are shown in figure 4-5. The timing diagram included in this figure shows the sequential events that occur when the LOAD A switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD A switch are in the released position as shown.

4-88. The LOAD A switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin T of front panel coupler card A101 to pin 3 of "and" gate MC93B. The signal $\overline{RF2}$ is transferred to A101MC93-6 from A106MC74-10 (RUN FF 2) on timing generator card A106. Therefore the machine must be in a halt mode for the LOAD A switch to be effective. With a true signal at input pins 3 and 6 of MC93B output pin 13 will go true. This true signal is transferred to A101MC85-2 (LOAD A FF) causing A101MC85-13 to go false. This false signal is felt at A101MC85-6. Input pin 7 of MC85 is false due to open contacts 1 and 3 of the pressed LOAD A switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal LAS at pin 62 of front panel coupler card A101. As long as the LOAD A switch is pressed, signal LAS remains true. As soon as the LOAD A switch is released, +4.5 volts is transferred to A101MC85-7 which causes output pin 9 to go false.

4-89. The signal LAS is transferred through pin 62 of the front panel coupler card, and pin 80 of the timing generator card to pin 1 of "and" gate MC117A and pin 14 of "and" gate MC116A. At time T2 the signal SWSA is generated by MC117A at output pin 14. This signal is transferred through pin 84 of the timing generator card and pin 35 of the instruction decoder card A107 to pin 2 of "and" gate MC77A. At time T2 and TS the signal STBA is generated at the output pin 13 of MC77A. This signal is transferred through pin 50 of the instruction decoder card and pin 38 of the arithmetic logic cards A102 through A105 to the clock input pin 1 of the A-register flip-flops and is used to clock the data on the T-bus into the A-register flip-flops.

4-90. As soon as the signal LAS is true at pin 14 of MC116A the signal SEO is generated at pin 13 of MC116A of the timing generator card. This signal is transferred through pin 72 of the timing generator card and pin 22 of the shift logic card A108 where it is used to generate the signal ISR, which enables the switch register gates on the front panel coupler card and transfers the switch register data to the IOBI lines. At time T2 the signal SEO also generates the signal IOI which is used to gate the data on the IOBI lines to the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where at time T2 it is used to generate the negative going signal $\overline{EOFE}$ at pin 13 of MC112A on the instruction decoder card. The signal $\overline{EOFE}$ is transferred through pin 67 of the instruction decoder card and pin 83 of the address decoder memory card A14 where it is used to generate the negative going signal $\overline{EOF}$ at pin 9 of "and" gate MC107B on the memory address decoder card. This signal is transferred through pin 75 of the memory address decoder card and pin 76 of the arithmetic logic cards. The signal $\overline{EOF}$ is used in the arithmetic logic cards to gate the data on the S-bus and R-bus to the T-bus. (The R-bus is cleared to all "zeros" at this time.) The T-bus data is then placed into the A-register flip-flops by the clock pulse STBA and each "1" bit will be indicated by a lighted A-register indicator lamp. Thus the LOAD A switch, when pressed, transfers the switch register data into the A-register and each switch that was in the up ("1") position will cause the corresponding A-register indicator lamp to light.

4-91. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-5, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S104. If normal, proceed to step "c". If abnormal, check the connection between A502S104-1,2 and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

e. At the computer front panel, turn on power.

f. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-80.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

g. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a logic 1 level. Then release the LOAD A switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "h". If the oscilloscope display is abnormal, check A101MC85, A101MC93B, and the LOAD A switch A502S104 and A106MC74 as the most probable cause of trouble.

h. Place the oscilloscope probe on A106M116-13.

i. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a logic 1 level. Then release the LOAD A switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "j". If the oscilloscope display is abnormal, check A106MC116 as the most probable cause of trouble.

j. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC117-14.

(6) Channel B input: A106TP1 (time T0).

k. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a 200 ηs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check A106MC117-2 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

l. At the computer front panel, turn off power.

m. Using the extender card, extend shift logic card A108 from the card cage.

n. At the computer front panel, turn on power.

o. Place the channel A oscilloscope probe on pin 84 of the shift logic card.

p. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a logic 1 level. Then release the LOAD A switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check A108MC106A and A108MC127A as the most probable cause of trouble.

q. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a 200 ηs pulse occuring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check MC44A and MC64A as the most probable cause of trouble.

r. At the computer front panel, turn off power.

s. Using the extender card, extend instruction decoder card A107 from the card cage.

t. At the computer front panel, turn on power.

u. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "v". If the oscilloscope display is abnormal, check MC112A and MC122A as the most probable cause of trouble.

v. Place the channel A oscilloscope probe on pin 50 of the instruction decoder card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check MC77A as the most probable cause of trouble.

w. At the computer front panel, turn off power.

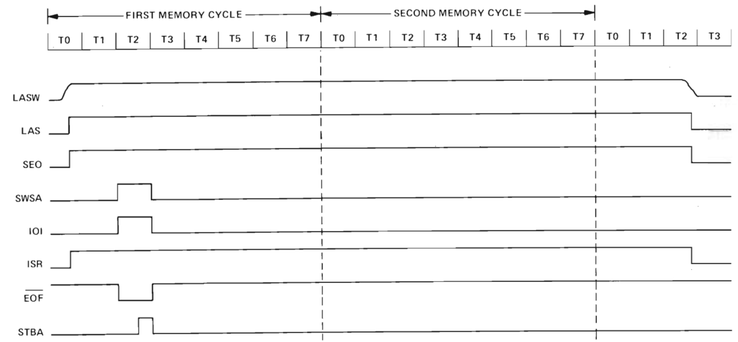
x. Using the extender card, extend memory address decoder card A14 from the card cage.

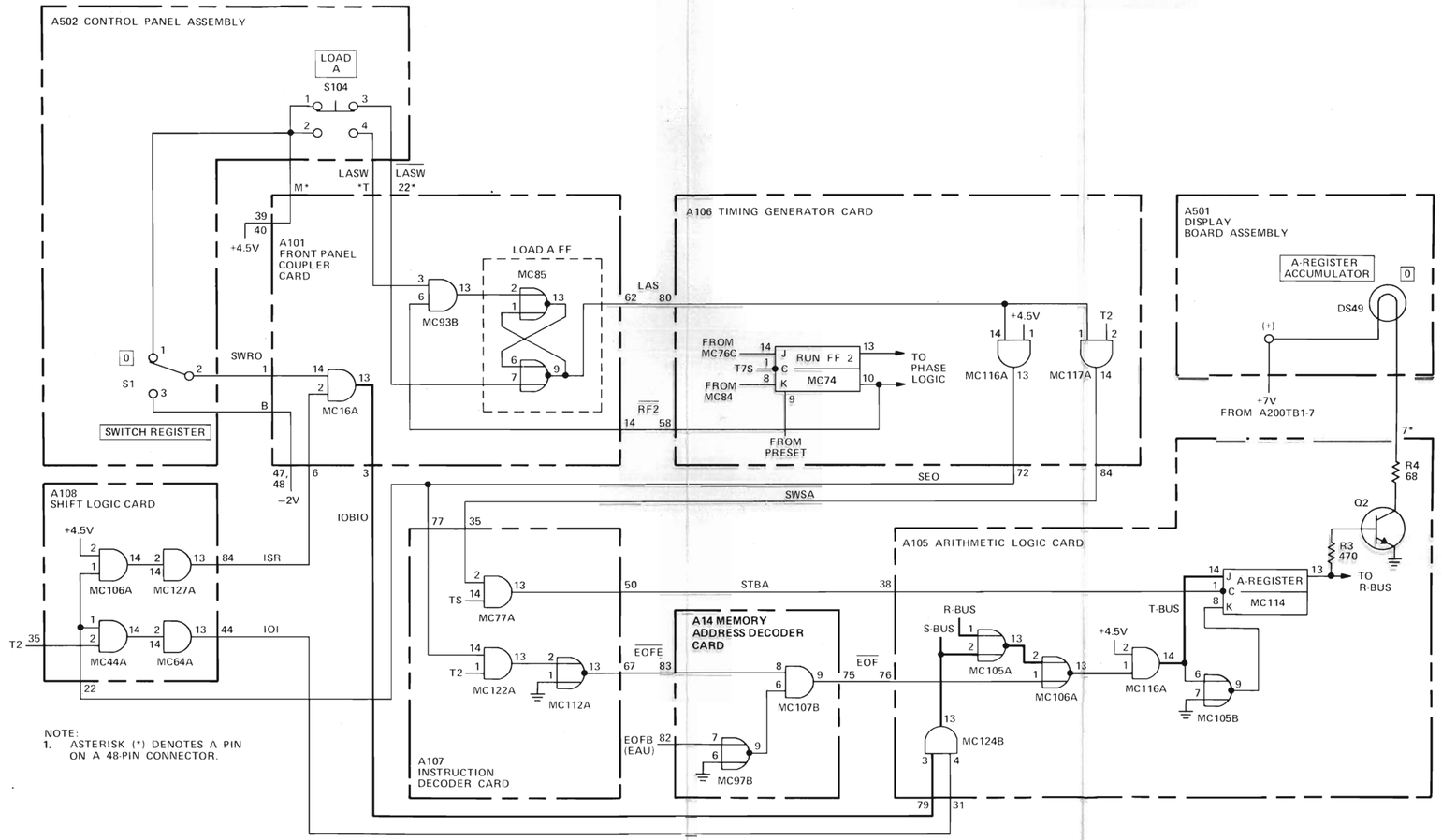
y. At the computer front panel, turn on power

z. Place the channel A oscilloscope probe on pin 75 of the memory address decoder card. At the computer front panel, press and hold the LOAD A switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "aa". If the oscilloscope display is abnormal, check MC97B and MC107B as the most probable cause of trouble.

aa. Check the arithmetic logic card (A102 through A105) that controls the A-register bit or bits in question. Also check the particular SWITCH REGISTER switch or switches on control panel A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the A-register indicator lamp or lamps, to the +7-volt connection (+) on display board assembly A501 for continuity.

bb. If all indications of the above test procedures are normal, the LOAD A switch and circuits are operating normally.





NOTE:
1. ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.

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Figure 4-5. LOAD A Switch Circuit, Servicing Diagram

4-92. LOAD B SWITCH, B-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with LOAD B switch S103 and the SWITCH REGISTER switches located on control panel assembly A502, and the B-REGISTER indicators located on display board assembly A501.

4-93. Description. The circuits associated with the LOAD B switch are shown in figure 4-6. The timing diagram included in the figure shows the sequential events that occur when the LOAD B switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD B switch are in the released position as shown.

4-94. The LOAD B switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin U of front panel coupler card A101 to pins 8 and 9 of "and" gate MC93C. The signal $\overline{RF2}$ is transferred to A101MC93-7 from A106MC74-10 (RUN FF 2) on timing generator card A106. Therefore the machine must be in a halt mode for the LOAD B switch to be effective. With a true signal at input pins 8, 9 and 7 of MC93C output pin 10 will go true. This true signal is transferred to A101MC95-2 of (LOAD B FF) causing A101MC95-13 to go false. This false signal is felt at A101MC85-6. Input pin 7 of MC95 is false due to open contacts 1 and 3 of the pressed LOAD B switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal LBS at pin 66 of front panel coupler card A101. As long as the LOAD B switch is pressed, signal LBS remains true. As soon as the LOAD B switch is released, +4.5 volts is transferred to A101MC95-7 which causes output pin 9 to go false.

4-95. The signal LBS is transferred through pin 66 of the front panel coupler card, and pin 65 of the timing generator card to pin 6 of "and" gate MC117B and pin 2 of "and" gate MC116B. At time T2 the signal SWSB is generated by MC117B at output pin 13. This signal is transferred through pin 71 of the timing generator card and pin 24 of the instruction decoder card A107 to pin 6 of "and" gate MC77B. At time T2 and TS the signal STBB is generated at the output pin 9 of MC77B. This signal is transferred through pin 51 of the instruction decoder card and pin 26 of the arithmetic logic cards A102 through A105 to the clock input pin 1 of the B-register flip-flops and is used to clock the data on the T-bus into the B-register flip-flops.

4-96. As soon as the signal LBS is true at pin 2 of MC116B the signal SEO is generated at pin 13 of MC116B of the timing generator card. This signal is transferred through pin 72 of the timing generator card and pin 22 of the shift logic card A108 where it is used to generate the signal ISR, which enables the switch register gates on the front panel coupler card and transfers the switch register data to the IOBI lines. At time T2 the signal SEO also generates the signal IOI which is used to gate the data on the IOBI lines to the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where at time T2 it is used to generate the negative going signal $\overline{EOFE}$ at pin 13 of MC112A on the instruction decoder card. The signal $\overline{EOFE}$ is transferred through pin 67 of the instruction decoder card and pin 83 of the memory address decoder card A14 where it is used to generate the negative going signal $\overline{EOF}$ at pin 9 of "and" gate MC107B on the direct memory logic card. This signal is transferred through pin 75 of the memory address decoder card and pin 76 of the arithmetic logic cards. The signal $\overline{EOF}$ is used in the arithmetic logic cards to gate the data on the S-bus and R-bus to the T-bus. (The R-bus is cleared to "zeros" at this time.) The T-bus data is then placed into the B-register flip-flops by the clock pulse STBB and each "1" bit will be indicated by a lighted B-register indicator lamp. Thus the LOAD B switch, when pressed, transfers the switch register data into the B-register and each switch that was in the up ("1") position will cause the corresponding B-register indicator lamp to light.

4-97. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-6, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S103. If normal, proceed to step "c". If abnormal, check the connection between A502S103-1,2 and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

e. At the computer front panel, turn on power.

f. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-65.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

g. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a logic 1 level. Then release the LOAD B switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "h". If the oscilloscope display is abnormal, check A101MC95, A101MC93C, and the LOAD B switch A502S103 and A106MC74 as the most probable cause of trouble.

h. Place the oscilloscope probe on A106MC116-13.

i. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a logic 1 level. Then release the LOAD B switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "j". If the oscilloscope display is abnormal, check A106MC116 as the most probable cause of trouble.

j. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC117-13.

(6) Channel B input: A106TP1 (time T0).

k. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check A106MC117-3 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

l. At the computer front panel, turn off power.

m. Using the extender card, extend shift logic card A108 from the card cage.

n. At the computer front panel, turn on power.

o. Place the channel A oscilloscope probe on pin 84 of the shift logic card.

p. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a logic 1 level. Then release the LOAD B switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check A108MC106A and A108MC127A as the most probable cause of trouble.

q. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check MC44A and MC64A as the most probable cause of trouble.

r. At the computer front panel, turn off power.

s. Using the extender card, extend instruction decoder card A107 from the card cage.

t. At the computer front panel, turn on power.

u. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "v". If the oscilloscope display is abnormal, check MC112A and MC122A as the most probable cause of trouble.

v. Place the channel A oscilloscope probe on pin 51 of the instruction decoder card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check MC77B as the most probable cause of trouble.

w. At the computer front panel, turn off power.

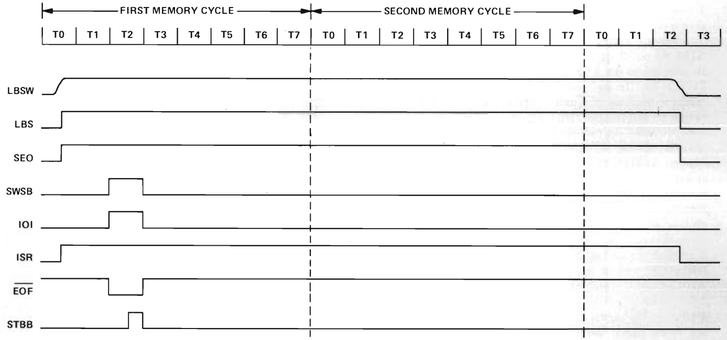
x. Using the extender card, extend memory address decoder card A14 from the card cage.

y. At the computer front panel, turn on power.

z. Place the channel A oscilloscope probe on pin 75 of the memory address decoder card. At the computer front panel, press and hold the LOAD B switch and check the oscilloscope display for a negative going 100 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "aa". If the oscilloscope display is abnormal, check MC97B and MC107B as the most probable cause of trouble.

aa. Check the arithmetic logic card (A101 through A105) that controls B-register bit or bits in question. Also check the particular SWITCH REGISTER switch or switches on control panel A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the B-register indicator lamp or lamps, to the +7-volt connection (+) on display board assembly A501 for continuity.

bb. If all indications of the above test procedure are normal, the LOAD B switch and circuits are operating normally.



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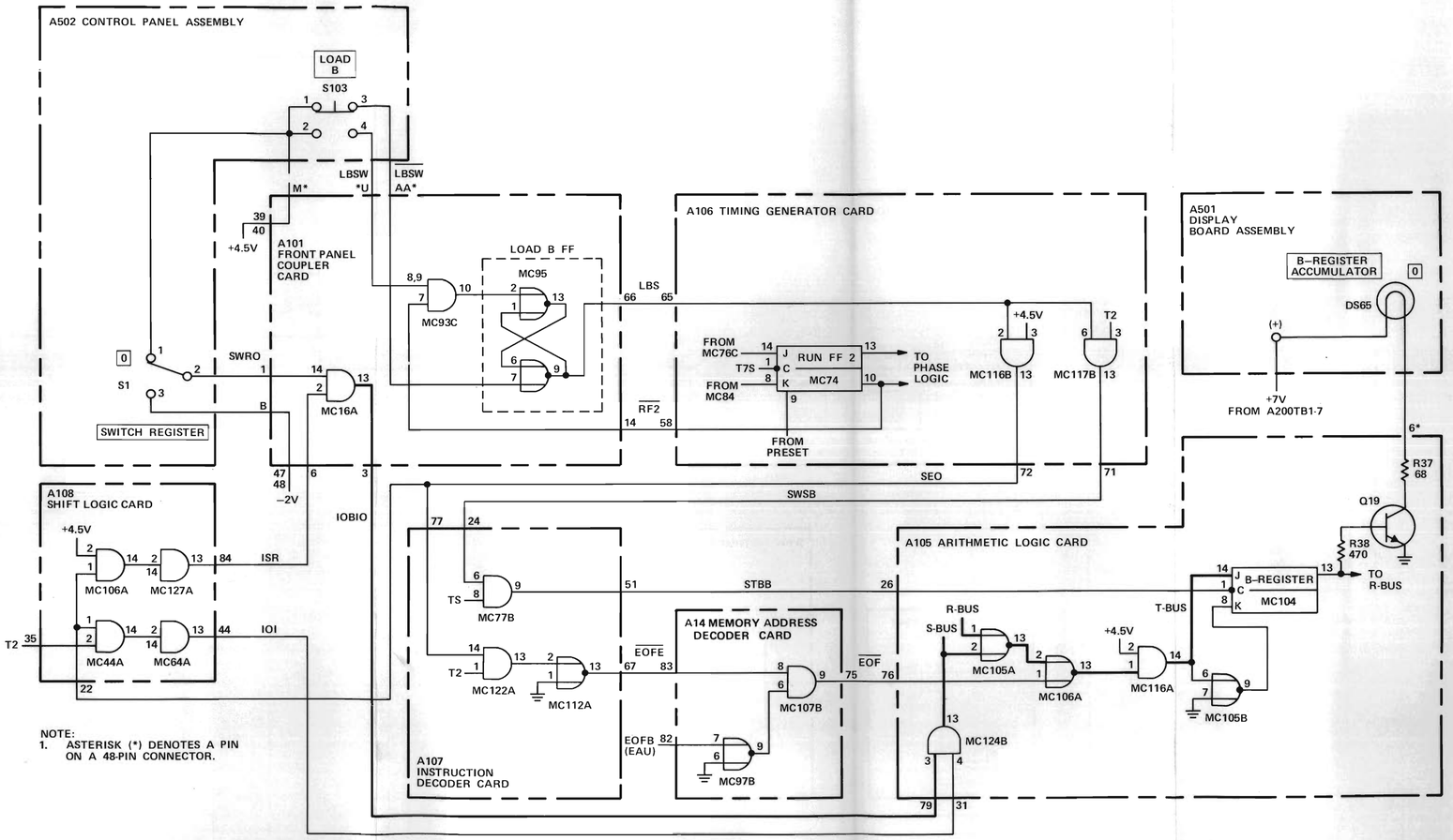


Figure 4-6. LOAD B Switch Circuit, Servicing Diagram

4-98. LOAD ADDRESS SWITCH, P- AND M-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and trouble-shooting procedure for the circuits associated with LOAD switches located on control panel assembly A502, and the P- and M-register indicators located on display board assembly A501.

4-99. Description. The circuits associated with the LOAD ADDRESS switch are shown in figure 4-7. The timing diagram included in this figure shows the sequential events that occur when the LOAD ADDRESS switch is pressed and released. In the following description it is assumed that initially all flip-flops shown are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD ADDRESS switch are in the released position as shown.

4-100. The LOAD ADDRESS switch is a momentary-action type switch. When pressed, it places +4.5 volts through the switch and pin V of front panel coupler card A101 to pin 2 of "and" gate MC103A. The signal RF2 is transferred to pin 1 of MC103A from A106MC74-10 (RUN FF 2) on timing generator card A106. Therefore the machine must be in a halt mode for the LOAD ADDRESS switch to be effective. With a true signal at input pins 1 and 2 of MC103A output pin 14 will go true. This true signal is transferred to A101MC105-2 (LOAD ADDRESS FF) causing A101MC105-13 to go false. This false signal is felt at input pin 6 of MC105. Input pin 7 of MC105 is false due to open contacts 1 and 3 of the pressed LOAD ADDRESS switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signals LADS at pin 70 of front panel coupler card A101. As long as the LOAD ADDRESS switch is pressed, signal LADS remains true. As soon as the LOAD ADDRESS switch is released, +4.5 volts is transferred to A101MC105-7 which causes output pin 9 to go false.

4-101. The signal LADS is transferred through pin 70 of the front panel coupler card, and pin 68 of the timing generator card to pin 8 of "and" gate MC116D, pin 9 of "and" gate MC117C, pin 6 of "and" gate MC107B, and pin 7 of "and" gate MC106B. At time T2 the signal SWSM is generated by MC117C at output pin 10. This signal is transferred through pin 73 of the timing generator card and pin 26 of instruction decoder card A107 to pins 7 and 14 of "and" gates MC55B and MC66A respectively. At time T2 and TS the signals STM (0-15) are generated and transferred through pins 20, 21, 27, and 28 of the instruction decoder card. These signals are transferred from the instruction decoder card, through pins 22 and 29 of the arithmetic logic cards A102 through A105 to the clock input pin 1 of the M-register flip-flops and is used to clock the data on the T-bus into the M-register flip-flops.

4-102. Time T2 and signal LADS also causes the signal SWSP to be generated by MC107B at output pin 13. This signal is transferred through pin 64 of the timing generator card and pin 37 of the instruction decoder card to pins 8 and 8 of "and" gates MC34C and MC36B respectively. At time T2 and TS the signals STP (0-15) are generated and transferred through pins 7, 8, and 74 of the instruction decoder card. These signals are transferred from the instruction decoder card, through pins 23 and 44 of the arithmetic logic cards to the clock input pin 1 of the P-register flip-flops and is used to clock the data on the T-bus into the P-register flip-flops.

4-103. The signal LADS being applied to pin 7 of MC106B causes both RUN FF 1 (MC84) and RUN FF 2 (MC74) to be reset. It also causes the PH1 FF (MC44) to be set at the end (time T7S) of the first machine cycle after the LOAD ADDRESS switch is pressed.

4-104. As soon as the signal LADS is true at pin 8 of MC116D the signal SEO is generated at pin 10 of MC116D of the timing generator card. This signal is transferred through pin 72 of the timing generator card and pin 22 of the shift logic card A108 where it is used to generate the signal ISR, which enables the switch register gates on the front panel coupler card and transfers the switch register data to the IOBI lines. At time T2 the signal SEO also generates the signal IOI which is used to gate the data on the IOBI lines to the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where at time T2 it is used to generate the negative going signal $\overline{\text{EOFE}}$ at pin 13 of MC112A on the instruction decoder card. The signal $\overline{\text{EOFE}}$ is transferred through pin 67 of the instruction decoder card and pin 83 of the memory address decoder card A14 where it is used to generate the negative going signal $\overline{\text{EOF}}$ at pin 9 of "and" gate MC107B on the direct memory logic card. This signal is transferred through pin 75 of the memory address decoder card and pin 76 of the arithmetic logic cards. The signal $\overline{\text{EOF}}$ is used in the arithmetic logic cards to gate the data on the S-bus and R-bus onto the T-bus. (The R-bus is cleared to "zeros" at this time.) The T-bus data is then placed into the M- and P-register flip-flops by the clock signals STM (0-15) and STP (0-15) and each "1" bit will be indicated by a lighted M- and P-register indicator lamp. Thus the LOAD ADDRESS switch, when pressed, transfers the switch register data into the M- and P-registers and each switch that was in the up ("1") position will cause the corresponding M- and P-register indicator lamp to light.

4-105. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information presented in figure 4-7, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S102. If normal, proceed to step "c". If abnormal, check the connection between A502S102-1,2 and A101-39,40 for continuity.

c. At the computer front panel, turn on power.

d. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

e. At the computer front panel, turn on power.

f. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-68.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

g. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a logic 1 level. Then release the LOAD ADDRESS switch and check the oscilloscope display of a logic 0 level. If the oscilloscope display is normal, proceed to step "h". If the oscilloscope display is abnormal, check A101MC105, A101MC103A, LOAD ADDRESS switch A502S102, and A106MC74 as the most probable cause of trouble.

h. Place the channel A oscilloscope probe on A106MC116-10.

i. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a logic 0 level. Then release the LOAD ADDRESS switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "j". If the oscilloscope display is abnormal, check A106MC116-9 for a +4.5-volt level.

j. Place the channel A oscilloscope probe on A106MC44-13.

k. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a logic 1 level. Then release the LOAD ADDRESS switch and check the oscilloscope display for a logic 1 level. If the oscilloscope display is normal, proceed to step "l". If the oscilloscope display is abnormal, check MC44, MC53, and MC106 as the most probable cause of trouble.

l. Place the channel A oscilloscope probe on A106MC106-2.

m. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a logic 1 level. Then release the LOAD ADDRESS switch and check the oscilloscope display for a logic 0 level.

n. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106MC117-10.

(6) Channel B input: A106TP1 (time T0).

o. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, check A106MC117-7 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

p. Place the channel A oscilloscope probe on A106MC107-13.

q. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "r". If the oscilloscope display is abnormal, check A106MC107-3 for the 200 ηs pulse referred to above. If the display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

r. At the computer front panel, turn off power.

s. Using the extender card, extend shift logic card A108 from the card cage.

t. At the computer front panel, turn on power.

u. Place the channel A oscilloscope probe on pin 84 of the shift logic card.

v. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a logic 1 level. Then release the LOAD ADDRESS switch and check the oscilloscope display for the logic 0 level. If the oscilloscope display is normal, proceed to step "w". If the oscilloscope display is abnormal, check MC106A and MC127A as the most probable cause of trouble.

w. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and

hold the LOAD ADDRESS switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "x". If the oscilloscope display is abnormal, check MC44A and MC64A as the most probable cause of trouble.

x. At the computer front panel, turn off power.

y. Using the extender card, extend instruction decoder card A107 from the card cage.

z. At the computer front panel, turn on power.

aa. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "bb". If the oscilloscope display is abnormal, check MC112A and MC122A as the most probable cause of trouble.

bb. Place the channel A oscilloscope probe on pin 7 of the instruction decoder card. At the computer front panel, press and hold the LOAD ADDRESS switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. Place the oscilloscope probe on pins 8, 20, 21, 27, 28, and 74 of the instruction decoder card and check the oscilloscope for a 45 μs to 55 μs pulse occurring every 1.6 μs from each of these pins. If the oscilloscope displays are normal, proceed to step "cc". If any of the oscilloscope displays are abnormal, check MC34, MC36, MC55, MC56, and MC66 as the most probable cause of trouble.

cc. At the computer front panel, turn off power.

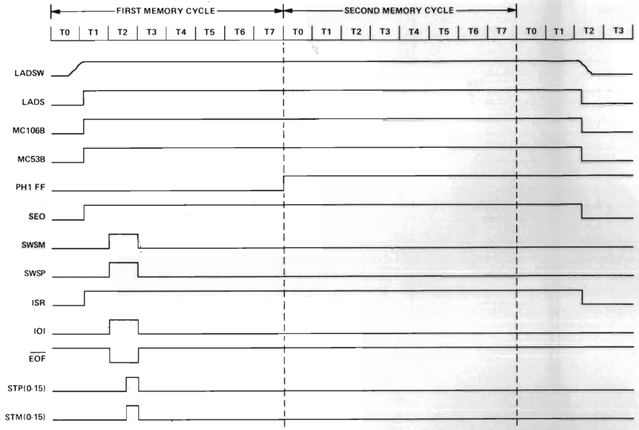
dd. Using the extender card, extend memory address decoder card A14 from the card cage.

ee. At the computer front panel, turn on power.

ff. Place the channel A oscilloscope probe on pin 75 of the memory address decoder card and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "gg". If the oscilloscope display is abnormal, check MC97B and MC107B as the most probable cause of trouble.

gg. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the LOAD ADDRESS switch the switch register data is not being properly transferred into the M- and P-registers and displayed by the M- and P-register indicator lamps, refer to figure 4-7 and check the arithmetic logic card (A102 through A105) that controls the M- and P-register bit or bits in question. Also check the particular switch register switch or switches on control panel assembly A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the M- and P-register indicator lamp or lamps, to the +7-volt connection (+) on display board assembly A501 for continuity.

hh. If all indications of the above test procedure are normal, the LOAD ADDRESS switch and circuits are operating normally.



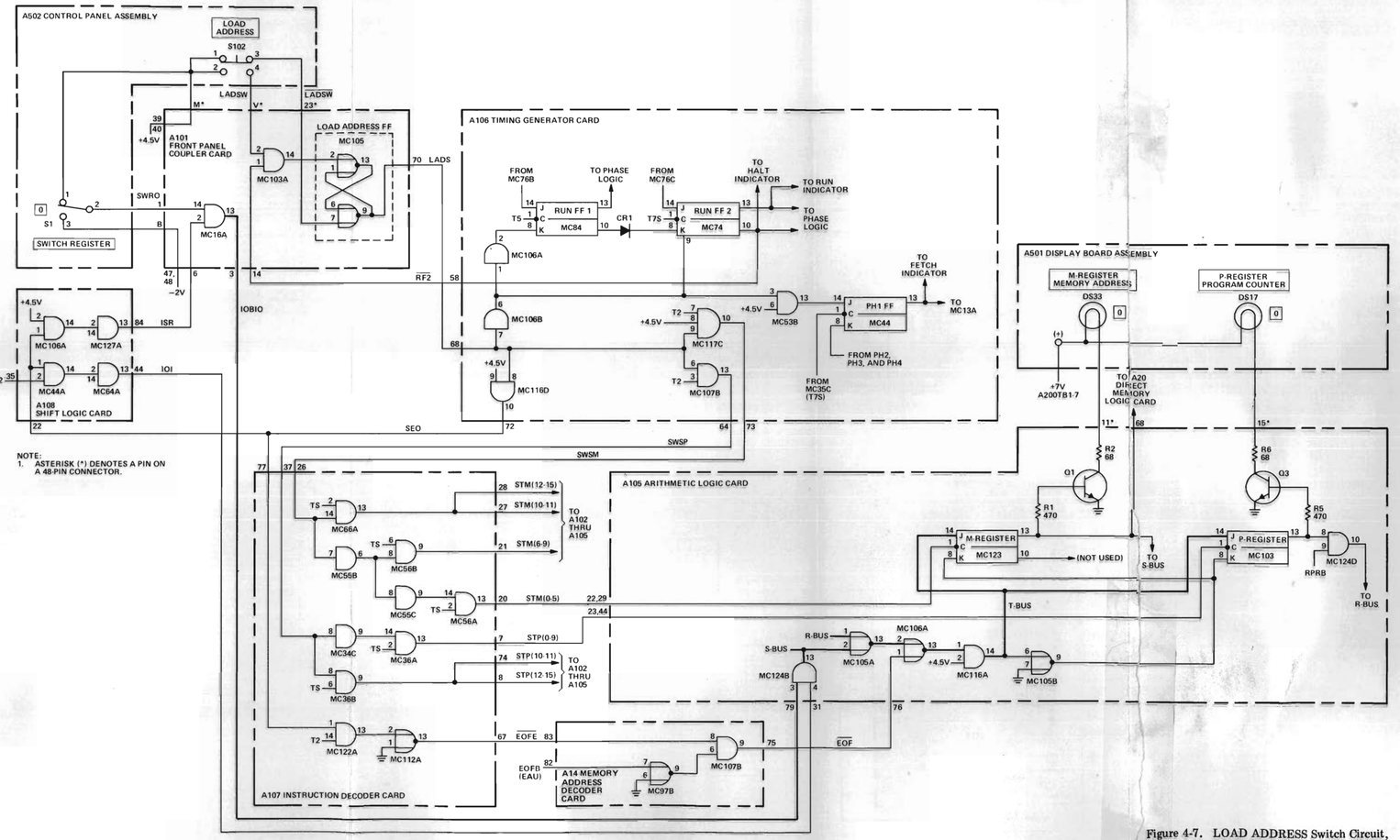


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Figure 4-7. LOAD ADDRESS Switch Circuit, Servicing Diagram

4-106. LOAD MEMORY SWITCH, T-REGISTER INDICATORS, AND SWITCH REGISTER SWITCHES. The following paragraphs provide a description and trouble-shooting procedure for the circuits associated with LOAD MEMORY switch S105 and the SWITCH REGISTER switches located on control panel assembly A502, and the T-register indicators located on display board assembly A501.

4-107. Description. The circuits associated with the LOAD MEMORY switch are shown in figure 4-8. The timing diagram included in this figure shows the sequential events that occur when the LOAD MEMORY switch is pressed and released. In the following description it is assumed that initially all flip-flops shown on the timing generator card A106 are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the LOAD MEMORY switch are in the released position as shown.

4-108. The LOAD MEMORY switch is a momentary-action type switch. When pressed, it transfers +4.5 volts through the switch, and pin S of the front panel coupler card A101 to pin 2 of "and" gate MC93A. The signal $\overline{RF2}$ is transferred to A101MC93-1 from A106MC74-10 (RUN FF 2) on the timing generator card A106. Therefore, the computer must be in the halt mode for the switch to be effective. With a true signal at input pins 1 and 2 of MC93A output pin 14 will go true. This true signal is transferred to A101MC75-2 (LOAD MEMORY FF) causing A101MC75-13 to go false. This false signal is felt at A101MC75-6. Input pin 7 of MC75 is false due to open contacts 1 and 3 of the pressed LOAD MEMORY switch. Input pins 6 and 7 being false cause output pin 9 to go true and generator signal LMS at pin 58 of front panel coupler card A101. As long as the LOAD MEMORY switch is pressed, signal LMS remains true. As soon as the LOAD MEMORY switch is released, +4.5 volts it transferred to A101MC75-7 which causes output pin 9 to go false.

4-109. The signal LMS is transferred through pin 58 of the front panel coupler card, pin 46 of the timing generator card and through "and" gate MC86C to the set and reset pin 1 of STEP 1 FF MC94A. The first time T2 after the switch has been pressed STEP 1 FF will be set and will remain set until the first time T2 after the switch is released. The output pin 13 of STEP 1 FF is transferred to the set and reset input pin 7 of the STEP 2 FF MC94B which is set at the next time T1 and remains set until the time T1 after the switch is released. The output of STEP 1 FF is also felt at pin 9 of "and" gate MC76C. The output of STEP 2 FF is transferred to input pin 2 of "nor" gate MC87A causing its output pin 13 to go false. This false output is felt at input pin 7 of "and" gate MC76C causing its output pin 10 to go false. This action results in a 1.4 μs pulse being generated at the output pin 10 of MC76C. This pulse from pin 10 of MC76C is transferred to the phase logic pin 3 of MC33 B, and to the set input pin 14 of RUN FF 2 MC74 and at time T7S the output pin 13 of MC74 goes true causing the RUN indicator to go on for 1.6 μs and enabling "and" gate MC27A. The reset output pin 10 of MC74 goes false at the same time the set output goes true. This false output causes the HALT indicator to go out and the LOAD MEMORY switch gate MC93A on the front panel coupler card to be disabled thereby disabling the switch for 1.6 μs. The signal LMS is also transferred through "and" gate MC96C to input pin 6 of "and" gate MC33B causing the output pin 13 of MC33B to go true. This true output is transferred throughout the phase logic and causes all flip-flops to be reset except PH3 FF which it causes to be set at time T7 and TS. The signal LMS is also transferred to special logic which is used when attempting to load data into memory locations 000000 or 000001 (the A- or B-registers). The signal LMS is also transferred to the memory timing circuits where it is used to inhibit the signal MST thereby preventing the sense amplifier data being transferred into the T-register. It is also used to enable the signal MWL which will allow the new T-register data to be transferred into memory. The signal LMS is also transferred to input pins 7 and 2 of "and" gates MC116C and MC107A respectively where the signals SEO and SWST are generated at the output pins 10 and 14 respectively of the respective gates and pins 72 and 62 respectively of the timing generator card. The output pin 13 of PH3 FF is transferred to input pin 14 of "and" gate MC15A and through "and" gate MC25A to input pin 2 of "and" gate MC37A. The output of "and" gate MC27A which is generated by the set output pin 13 of RUN FF 2 is transferred to input pins 2 and 14 of MC15A and MC37A respectively and allow the signal PH3 to be generated at the output pin 13 of MC37A. The signals PH3 and P123 are transferred out of the timing generator card on pins 60 and 23 respectively. The signal P123 is transferred through "and" gate MC56B to the memory timing logic where it is used to enable the memory timing signal MTE which allows the necessary memory timing to be generated and the new data to be written into memory.

4-110. The signal SEO is transferred to pin 22 of the shift logic card A108 where it is used to generate the signal ISR which enables the switch register gates on the front panel coupler card transferring the switch register data onto the IOBI lines. It is also used in the shift logic card at time T2 to generate the signal IOI at pin 44 of the card. The signal IOI is transferred to pin 31 of the arithmetic logic cards A102 through A105 where it is used to gate the data on the IOBI lines onto the S-bus. The signal SEO is also transferred to pin 77 of the instruction decoder card where it is used at time T2 to generate the negative going signal $\overline{EOFE}$ at pin 67 of that card. The signal $\overline{EOFE}$ is transferred from pin 67 of the instruction decoder card to pin 83 of the memory address decoder card. A14 where it is used to generate the negative going signal $\overline{EOF}$ at pin 75 of that card. The signal $\overline{EOF}$ is transferred to pin 76 of the arithmetic logic cards where it is used to transfer the R- and S-bus data onto the T-bus at time T2.

4-111. At time T0 the signal P123 causes the signal RST to be generated at pin 58 of the instruction decoder card. This signal is transferred to pin 7 of the arithmetic logic cards where it is used as a direct reset signal for all T-register flip-flops.

4-112. At time T2 the signal SWST was generated in the timing generator card. At time T2 and TS the signal SWST

causes the signal STBT to be generated at pin 63 of the instruction decoder card. The signal STBT is transferred to pin 51 of the arithmetic logic cards where it is used to clock the T-bus data into the T-register flip-flops. Each "1" bit being indicated by a lighted T-register indicator lamp on the door assembly.

4-113. At time T6T7 the signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) are generated within the instruction decoder card. These signals are transferred to the arithmetic logic cards where they are used to transfer the P-register data to the R-bus, set bit zero of the S-bus to a "1", add the R- and S-bus data together and transfer this combined data (P-register plus one) to the T-bus, and store the T-bus data into the P- and M-register flip-flops. This new P- and M-register data being indicated by the P- and M-register indicator lamps on the door assembly.

4-114. Thus by pressing the LOAD MEMORY switch the data toggled into the switch register is transferred via the T-register into the memory location addressed by the M-register and the P- and M-registers are incremented by one.

4-115. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-8, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S105. If normal, proceed to step "c". If abnormal, check the connection between A502S105-1,2 and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: channel B.

(3) Time/cm: 0.2 μs

(4) Channel A and B volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-46.

(6) Channel B input: A106TP1 (Time T0).

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

f. At the computer front panel, turn on power. Press and hold the LOAD MEMORY switch and check the oscilloscope display for a logic 1 level. Then release the LOAD MEMORY switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check A101MC75, A101MC93A, LOAD MEMORY switch A502S105, and A106MC74 as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on A106MC116-10.

h. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a logic 1 level. Then release the LOAD MEMORY switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A106MC116 as the most probable cause of trouble.

i. Place the channel A oscilloscope probe on A106MC86-9.

j. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a logic 1 level. Then release the LOAD MEMORY switch and check the oscilloscope display for a logic 0 level.

k. At the oscilloscope, make the following settings and connections:

(1) Time/cm: 1.0 μs

(2) Channel A input: A106MC107-14.

l. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "m". If the oscilloscope display is abnormal, check A106MC107-1 for the 200 ηs pulse referred to above. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

m. At the oscilloscope, make the following settings and connections:

(1) Time/cm: 2ms.

(2) Channel A input: A106MC24-13.

n. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.4 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check A106MC24, A106MC33, A106MC76, A106MC87, A106-MC94, and A106MC96 as the most probable cause of trouble.

o. Place the channel A oscilloscope probe on pin 60 of the timing generator card.

p. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope display is abnormal, check A106MC15-2 for a 1.6 μs pulse every time the switch is pressed. If this display is abnormal, check A106MC27 as the most probable cause of trouble.

q. Place the channel A oscilloscope probe on pin 23 of the timing generator card.

r. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "s". If the oscilloscope display is abnormal, check A106MC37, and A106MC25 as the most probable cause of trouble.

s. Place the channel A oscilloscope probe on A106MC56-6.

t. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "u". If the oscilloscope display is abnormal, the most probable cause of trouble is A106MC56.

u. At the computer front panel, turn off power.

v. Using the extender card, extend shift logic card A108 from the card cage.

w. At the computer front panel, turn on power.

x. Place the channel A oscilloscope probe on pin 84 of the shift logic card and adjust time/cm to 1.0 μs.

y. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a logic 1 level. Then release the LOAD MEMORY switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "z". If the oscilloscope display is abnormal, check A108MC106 and A108MC127 as the most probable cause of trouble.

z. Place the channel A oscilloscope probe on pin 44 of the shift logic card. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "aa". If the oscilloscope display is abnormal, check A108MC44 and A108MC64 as the most probable cause of trouble.

aa. At the computer front panel, turn off power.

bb. Using the extender card, extend instruction decoder card A107 from the card cage.

cc. At the computer front panel, turn on power.

dd. Place the channel A oscilloscope probe on pin 63 of the instruction decoder card.

ee. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "ff". If the oscilloscope display is abnormal, check A107MC92 as the most probable cause of trouble.

ff. Place the channel A oscilloscope probe on pin 67 of the instruction decoder card.

gg. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "hh". If the oscilloscope display is abnormal, check A107MC112 and A107MC122 as the most probable cause of trouble.

hh. At the oscilloscope, make the following settings and connections:

(1) Channel B volts/cm: 0.1 (if using 10:1 probe).

(2) Channel B input: A107-72.

ii. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "jj". If the oscilloscope display is abnormal, check A107MC106, A107MC107, and A107MC126 as the most probable cause of trouble.

jj. Place the oscilloscope probe on pin 81 of the instruction decoder card.

kk. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "ll". If the oscilloscope display is abnormal, check A107MC116, A107MC97, A107MC96, and A107MC106 as the most probable cause of trouble. Also check that the INSTRUCTION switch on the display board assembly A501 is in the NORM position.

ll. Place the channel A oscilloscope probe on pin 75 of the instruction decoder card.

mm. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is

pressed. If the display is normal, proceed to step "nn". If the display is abnormal, check A107MC107 and A107MC-127 as the most probable cause of trouble.

nn. Place the channel B oscilloscope probe on pin 58 of the instruction decoder card.

oo. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "pp". If the oscilloscope display is abnormal, check A107MC114 and A107MC125 as the most probable cause of trouble.

pp. Place the channel A oscilloscope probe on pin 7 of the instruction decoder card.

qq. At the computer front panel, repeatedly press and release the LOAD MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. Place the oscilloscope probe on pins 8, 20, 21, 27, 28, and 74 of the instruction decoder card and check the oscilloscope display for a 45 ηs to 55 ηs pulse from each of these pins every time the switch is pressed. If the oscilloscope displays are normal, proceed to step "rr". If any of the oscilloscope displays are abnormal, check A107MC34, A107MC35, A107MC36, A107MC53, A107-MC55, A107MC56, A107MC63 and A107MC66 as the most probable cause of trouble.

rr. At the computer front panel, turn off power.

ss. Using the extender card, extend memory address decoder card A14 from the card cage.

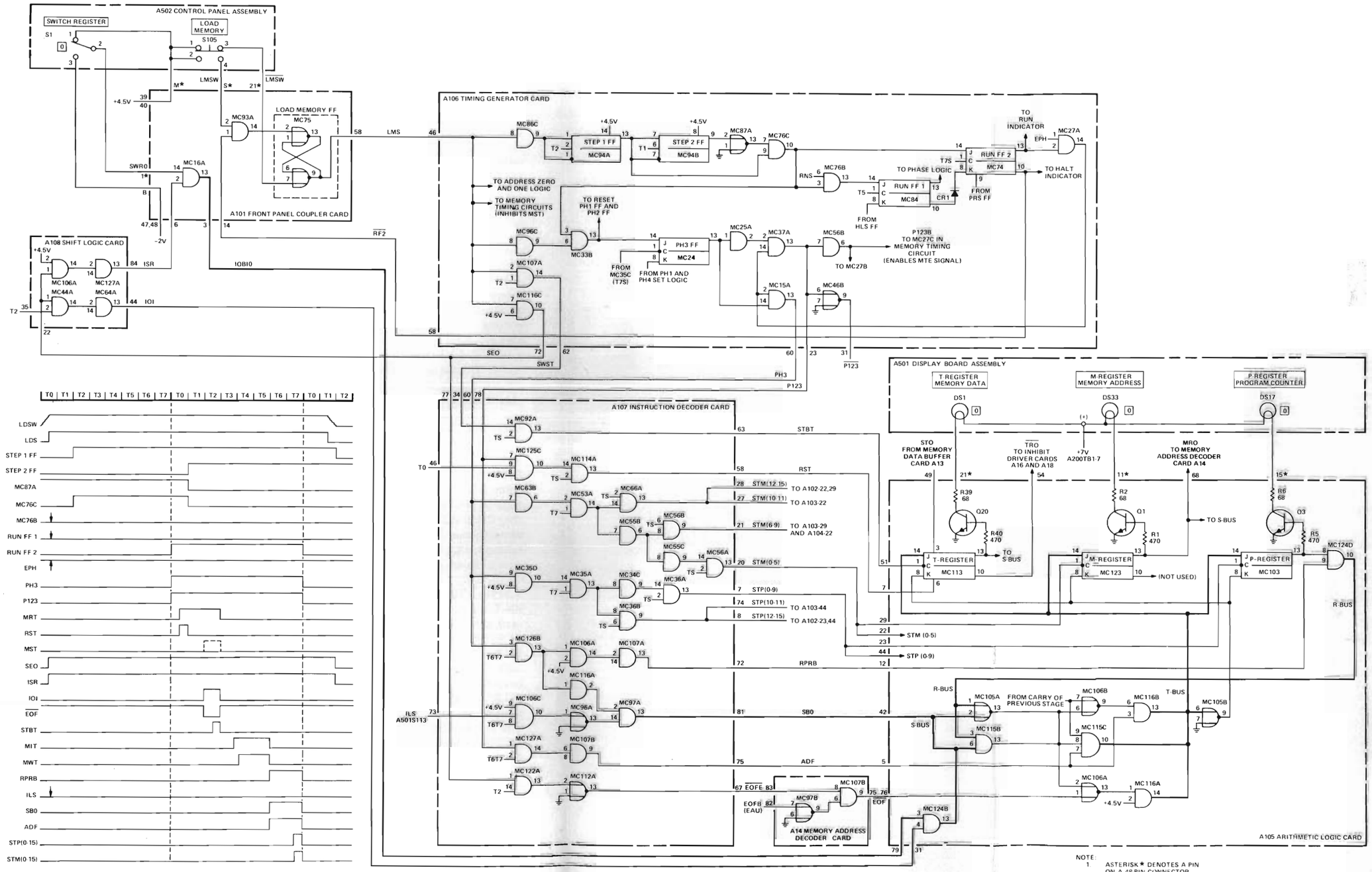
tt. At the computer front panel, turn on power.

uu. Place the channel B oscilloscope probe on pin 75 of memory address decoder card A14.

vv. At the computer front panel, press and hold the LOAD MEMORY switch and check the oscilloscope display for a negative going 200 ηs pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "ww". If the oscilloscope display is abnormal, check A14MC97 and A14MC107 as the most probable cause of trouble.

ww. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the LOAD MEMORY switch the switch register data is not being properly transferred into the addressed memory location and the P- and M-registers are not being properly incremented, refer to figure 4-8 and check the arithmetic logic card (A102 through A105) that controls the bit or bits in question. Also check the particular switch register switch or switches on control panel assembly A502 and the switch register gate or gates on front panel coupler card A101 for proper operation. Also check the cable connection from the arithmetic logic card, through the M- and P-register indicator lamp or lamps, to the +7-volt connection (+) on display board assembly A501 for continuity. The load memory process is also a function of the computer memory section. Refer to paragraph 4-458 for trouble-shooting information for that section.

xx. If all indications of the above test procedure are normal, the LOAD MEMORY switch and circuits are operating normally.



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NOTE:
1. ASTERISK * DENOTES A PIN ON A 48-PIN CONNECTOR.

Figure 4-8. LOAD MEMORY Switch Circuit, Servicing Diagram

4-116. DISPLAY MEMORY SWITCH AND T-, P-, AND M-REGISTER INDICATORS. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with DISPLAY MEMORY switch S101 located on control panel assembly A502, and the T-, P-, and M-register indicators located on display board assembly A501.

4-117. Description. The circuits associated with the DISPLAY MEMORY switch are shown in figure 4-9. The timing diagram included in this figure shows the sequential events that occur when the DISPLAY MEMORY switch is pressed and released. In the following description it is assumed that initially all flip-flops shown on the timing generator card A106 are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the DISPLAY MEMORY switch are in the released position as shown.

4-118. The DISPLAY MEMORY switch is a momentary-action type switch. When pressed, it transfers +4.5 volts through the switch, and pin W of the front panel coupler card A101 to pin 3 of "and" gate MC103B. The signal $\overline{RF2}$ is transferred to A101MC103-6 from A106MC74-10 (RUN FF 2) on the timing generator card A106. Therefore, the computer must be in the halt mode for the switch to be effective. With a true signal at input pins 3 and 6 of MC103B output pin 13 will go true. This true signal is transferred to A101MC115-2 (DISPLAY MEMORY FF) causing output pin 13 to go false. This false signal is felt at input pin 6 of MC115. Input pin 7 of MC115 is false due to open contacts 1 and 3 of the pressed DISPLAY MEMORY switch. Input pins 6 and 7 of MC115 being false cause output pin 9 to go true and generate signal DMS at pin 74 of front panel coupler card A101. As long as the DISPLAY MEMORY switch is pressed, signal DMS remains true. As soon as the DISPLAY MEMORY switch is released, +4.5 volts is transferred to input pin 7 of MC115 which causes output pin 9 to go false.

4-119. The signal DMS is transferred through pin 74 of the front panel coupler card, pin 59 of the timing generator card, through "and" gate MC86B to the set and reset pin 1 of STEP 1 FF MC94A. The first time T2 after the switch has been pressed STEP 1 FF will be set and will remain set until the first time T2 after the switch is released. The output pin 13 of STEP 1 FF is transferred to A106MC94-7 (STEP 2 FF) which becomes set at the next time T1 and remains set until the time T1 after the switch is released. The output of STEP 1 FF is also felt at pin 9 of "and" gate MC76C. The output of STEP 2 FF is transferred to input pin 2 of "nor" gate MC87A causing its output pin 13 to go false. This false output is felt at input pin 7 of "and" gate MC76C causing its output pin 10 to go false. This action results in a 1.4 μs pulse being generated at the output pin 10 of MC76C. This pulse from pin 10 of MC76C is transferred to pin 3 of "and" gate MC33B of the phase logic, and to the set input pin 14 of RUN FF 2 MC74 and at time T7S the output pin 13 of MC74 goes true causing the RUN indicator to go on for 1.6 μs and enabling "and" gate MC27A. The reset output pin 10 of MC74 goes false at the same time the set output goes true. This false output causes the HALT indicator to go out and the DISPLAY MEMORY switch gate MC103B on the front panel coupler card to be disabled thereby disabling the switch for 1.6 μs. The signal DMS is also transferred through "and" gate MC96D to input pin 6 of "and" gate MC33B causing the output pin 13 of MC33B to go true when input pin 3 is also true. This true output is transferred throughout the phase logic and causes all flip-flops to be reset except PH3 FF which it causes to be set at time T7S. The output at pin 13 of PH3 FF is transferred to input pin 14 of "and" gate MC15A and through "and" gate MC25A to input pin 2 of "and" gate MC37A. The output of "and" gate MC27A which is generated by the set output pin 13 of RUN FF 2 is transferred to input pins 2 and 14 of MC15A and MC37A respectively and allow the signals P123 and PH3 to be generated at the output pin 13 of MC37A and pin 13 of MC15A respectively. The signals PH3 and P123 are transferred out of the timing generator card on pins 60 and 23 respectively. The signal P123 is transferred through "and" gate MC56B to the memory timing logic where it is used to enable the memory timing signal MTE which allows the necessary memory timing to be generated and the memory data to be read into the sense amplifiers and thence into the T-register during time T2.

4-120. At time T0 the signal P123 causes the signal RST to be generated at pin 58 of the instruction decoder card. This signal is transferred to pin 7 of the arithmetic logic cards where it is used as a direct reset signal for all T-register flip-flops.

4-121. At time T6T7 the signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) are generated within the instruction decoder card. These signals are transferred to the arithmetic logic cards where they are used to transfer the P-register data to the R-bus, set bit zero of the S-bus to a "1", add the R- and S-bus data together and transfer this combined data (P-register plus one) to the T-bus, and store the T-bus data into the P- and M-register flip-flops. This new P- and M-register data being indicated by the P- and M-register indicator lamps on the door assembly.

4-122. Thus by pressing the DISPLAY MEMORY switch the data within the addressed memory location is transferred into the T-register and the P- and M-registers are incremented by one.

4-123. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-9, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S101. If normal, proceed to step "c". If abnormal, check the connection between A502S101-1,2 and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 1.0 μs.

(4) Channel B volts/cm: 0.1 (if using 10:1 probe).

(5) Channel B input: A106-59.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

f. At the computer front panel, turn on power. Press and hold the DISPLAY MEMORY switch and check the oscilloscope display for a logic 1 level. Then release the DISPLAY MEMORY switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check A101MC115, A101MC103B, DISPLAY MEMORY switch A502S101, and A106MC74 as the most probable cause of trouble.

g. Place the channel B oscilloscope probe on A106MC96-13.

h. At the computer front panel, press and hold the DISPLAY MEMORY switch and check the oscilloscope display for a logic 1 level. Then release the DISPLAY MEMORY switch and check the oscilloscope display for a logic 0 level.

i. Place the channel B oscilloscope probe on pin 13 of MC24.

j. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check A106MC24, and A106MC33 as the most probable cause of trouble.

k. Place the channel B oscilloscope probe on A106MC86-6.

l. At the computer front panel, press and hold the DISPLAY MEMORY switch and check the oscilloscope display for a logic 1 level. Then release the DISPLAY MEMORY switch and check the oscilloscope display for a logic 0 level.

m. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: Channel B.

(3) Time/cm: 1.0 μs.

(4) Channel B volts/cm: 0.1 (if using 10:1 probe).

(5) Channel B input: A106MC76-10.

(6) Channel B input: A106TP1 (time T0).

n. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.4 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "o". If the oscilloscope display is abnormal, check A106MC94, and A106MC87 as the most probable cause of trouble.

o. Place the channel B oscilloscope probe on pin 60 of the timing generator card.

p. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "q". If the oscilloscope is abnormal, check A106MC15-2 for a 1.6 μs pulse every time the switch is pressed. If this display is abnormal, check A106MC27 as the most probable cause of trouble.

q. Place the channel B oscilloscope probe on pin 23 of the timing generator card.

r. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "s". If the oscilloscope display is abnormal, check A106MC37, and A106MC25 as the most probable cause of trouble.

s. Place the channel B oscilloscope probe on A106MC56-6.

t. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed.

u. At the computer front panel, turn off power.

v. Using the extender card, extend instruction decoder card A107 from the card cage.

w. At the computer front panel, turn off power.

x. Place the channel B oscilloscope probe on pin 58 of the instruction decoder card.

y. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "z". If the oscilloscope display is abnormal, check A107MC114 and A107MC125 as the most probable cause of trouble.

z. Place the channel B oscilloscope probe on pin 72 of the instruction decoder card.

aa. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "bb". If the oscilloscope display is abnormal, check A107MC106, A107MC107, and A107MC126 as the most probable cause of trouble.

bb. Place the channel B oscilloscope probe on pin 81 of the instruction decoder card.

cc. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "dd". If the oscilloscope display is abnormal, check A107MC116, A107MC97, A107MC96, and A107MC106 as the most probable cause of trouble. Also check that the INSTRUCTION switch on the display board assembly A501 is in the NORM position.

dd. Place the channel B oscilloscope probe on pin 75 of the instruction decoder card.

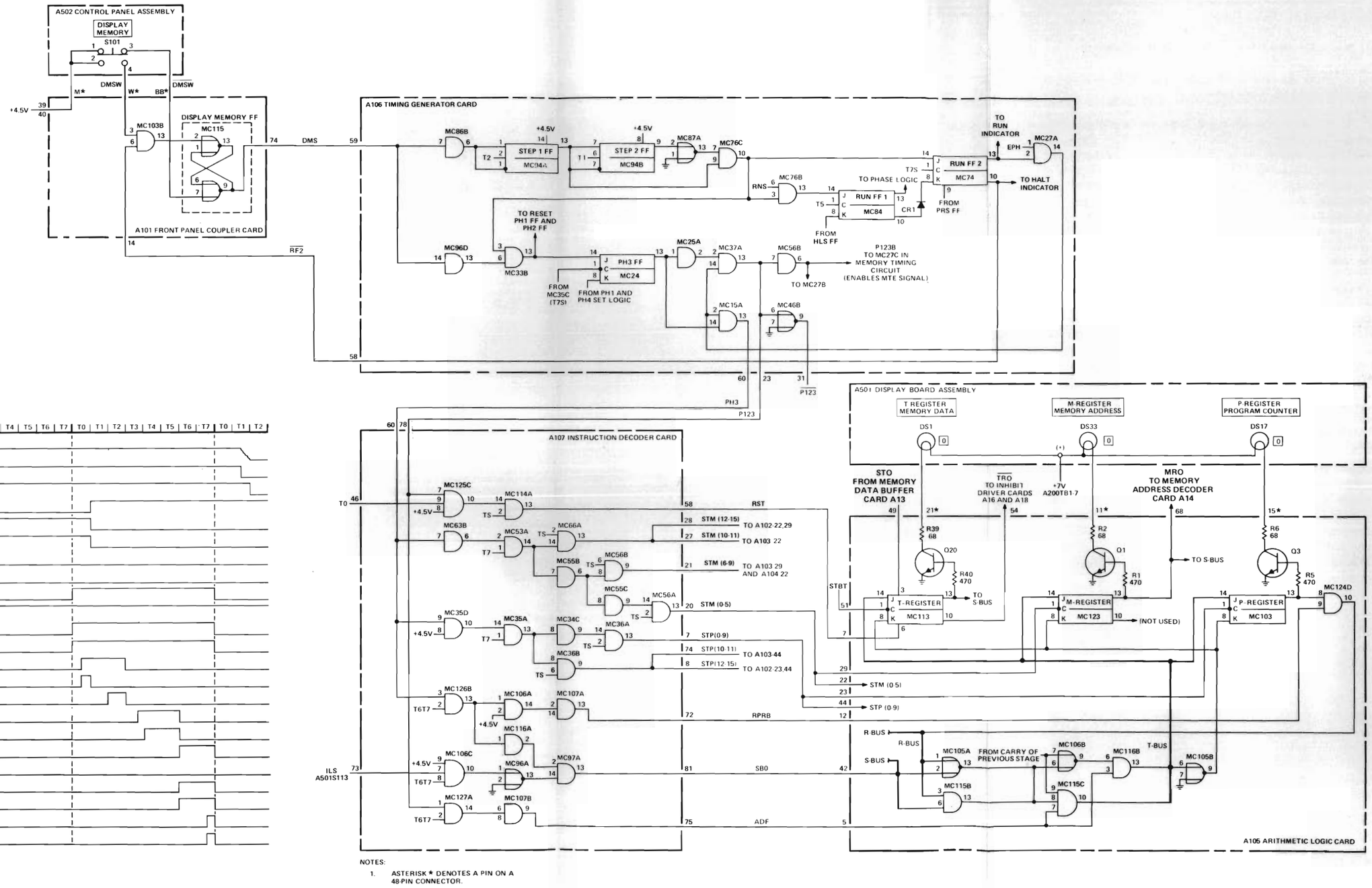
ee. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 400 ηs pulse every time the switch is pressed. If the display is normal, proceed to step "ff". If the display is abnormal, check A107MC107 and A107MC127 as the most probable cause of trouble.

ff. Place the channel B oscilloscope probe on pin 7 of the instruction decoder card.

gg. At the computer front panel, repeatedly press and release the DISPLAY MEMORY switch and check the oscilloscope display for a 45 ηs to 55 ηs pulse every time the switch is pressed. Place the oscilloscope probe on pins 8, 20, 21, 27, 28, and 74 of the instruction decoder card and check the oscilloscope display for a 45 ηs to 55 ηs pulse from each of these pins every time the switch is pressed. If the oscilloscope displays are normal, proceed to step "hh". If any of the oscilloscope displays are abnormal, check A107MC34, A107MC36, A107MC55, A107MC56, and A107MC66 as the most probable cause of trouble.

hh. If, at this point in the test procedure, all checks have indicated normal operation but by pressing the DISPLAY MEMORY switch the memory data is not being properly transferred into the T-register or the P- and M-registers are not being properly incremented, refer to figure 4-9 and check the arithmetic logic card A102 through A105 that controls the bit or bits in question. Also check the cable connection from the arithmetic logic card, through the T-, M-, and P-register indicator lamp or lamps, to the +7-volt connection on display board assembly A501-(+) for continuity.

ii. If all indications of the above test procedure are normal, the DISPLAY MEMORY switch and circuits are operating normally.



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NOTES:

1. ASTERISK * DENOTES A PIN ON A 48-PIN CONNECTOR.

Figure 4-9. DISPLAY MEMORY Switch Circuit, Servicing Diagram

4-124. SINGLE CYCLE SWITCH AND P- AND M-REGISTER INDICATORS. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with SINGLE CYCLE switch S100 located on control panel assembly A502 and the P- and M-register indicators located on display board assembly A501.

4-125. Description. The circuits associated with the SINGLE CYCLE switch are shown in figure 4-10. A timing diagram showing the sequential events events that occur when the SINGLE CYCLE switch is pressed is given in figure 4-10. In the following description it is assumed that initially all flip-flops shown on the timing generator card A106 are in the reset condition, the RUN indicator is off, the HALT indicator is on, and the contacts of the SINGLE CYCLE switch are in the released position as shown.

4-126. The SINGLE CYCLE switch is a momentary-action type switch. When pressed, it transfers +4.5 volts through the switch, and pin X of the front panel coupler card A101 to pin 7 of "and" gate MC103C. The signal $\overline{RF2}$ is transferred to pins 8 and 9 of MC103C from A106MC74-10 (RUN FF 2) on the timing generator card A106. Therefore, the computer must be in the halt mode for the switch to be effective. With a true signal at input pins 7, 8, and 9 of MC103 output pin 10 will go true. This true signal is transferred to A101MC125-2 (SINGLE CYCLE FF) causing output pin 13 to go false. This false signal is felt at input pin 6. Input pin 7 of MC125 is false due to open contacts 1 and 3 of the pressed SINGLE CYCLE switch. Input pins 6 and 7 being false cause output pin 9 to go true and generate signal SCS at pin 78 of front panel coupler card A101. As long as the SINGLE CYCLE switch is pressed, signal SCS remains true. As soon as the SINGLE CYCLE switch is released, +4.5 volts is transferred to input pin 7 of MC125 which causes output pin 9 to go false.

4-127. The signal SCS is transferred through pin 78 of the front panel coupler card, pin 56 of the timing generator card, through "and" gate MC86, to A106MC94-1 (STEP 1 FF). The first time T2 after the switch has been pressed STEP 1 FF will be set and will remain set until the first time T2 after the switch is released. The output pin 13 of STEP 1 FF is transferred to A106MC94-7 (STEP 2 FF) which is set at the next time T1 and remains set until the time T1 after the switch is released. The output of STEP 1 FF is also felt at pin 9 of "and" gate MC76C. The output of STEP 2 FF is transferred to input pin 2 of "nor" gate MC87A causing its output pin 13 to go false. This false output is felt at input pin 7 of "and" gate MC76C causing its output pin 10 to go false. This action results in a 1.4 μs pulse being generated at the output pin 10 of MC76C. This pulse from pin 10 of MC76C is transferred to the phase logic and to A106MC74-14 (RUN FF 2) MC74 and at time T7S the output pin 13 of MC74 goes true causing the RUN indicator to go on for 1.6 μs and enabling "and" gate MC27A. The reset output pin 10 of MC74 goes false at the same time the set output goes true. This false output causes the HALT indicator to go out for 1.6 μs and the SINGLE CYCLE SWITCH GATE MC103C on the front panel coupler card to be disabled thereby disabling the switch for 1.6 μs.

4-128. The output from pin 14 of MC27 is transferred to the phase logic and allows the currently active phase flip-flops output to be transferred throughout the computer for 1.6 μs (one machine cycle).

4-129. Thus the SINGLE CYCLE switch, when pressed, allows the currently active phase to be operated for only one machine cycle.

4-130. Test procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-10, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pins 1 and 2 of A502S100. If normal, proceed to step "c". If abnormal, check the connection between A502S100-1,2 and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 1.0 μs.

(4) Channel B volts/cm: 0.1 (if using 10:1 probe).

(5) Channel B input: A106-56.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

f. At the computer front panel, turn off power. Press and hold the SINGLE CYCLE switch and check the oscilloscope display for a logic 1 level. Then release the SINGLE CYCLE switch and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check A101MC125, A101MC103C, SINGLE CYCLE switch A502S100, and A106MC74 as the most probable cause of trouble.

g. Place the channel B oscilloscope probe on A106MC86-2.

h. At the computer front panel, press and hold the SINGLE CYCLE switch and check the oscilloscope display for a logic 1 level. Then release the SINGLE CYCLE switch and check the oscilloscope display for a logic 0 level.

i. Place the channel B oscilloscope probe on A106MC76-10, and set triggering source to channel B.

j. At the computer front panel, repeatedly press and release the SINGLE CYCLE switch and check the oscilloscope display for a 1.4 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "k". If the oscilloscope display is abnormal, check A106MC94, and A106MC87 as the most probable cause of trouble.

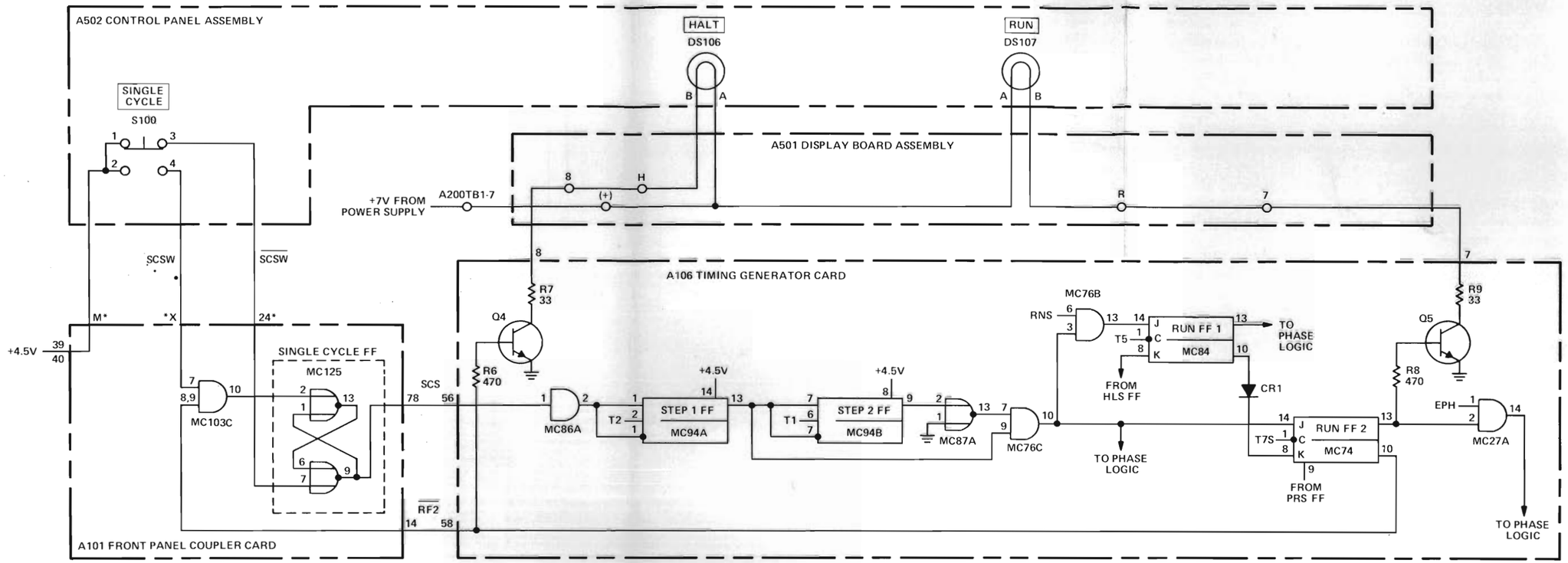
k. Place the channel B oscilloscope probe on A106MC74-13.

l. At the computer front panel, repeatedly press and release the SINGLE CYCLE switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed. If the oscilloscope display is normal, proceed to step "m". If the oscilloscope display is abnormal, check A106MC74-1 for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. If this display is abnormal, refer to paragraph 4-153 and troubleshoot the basic timing circuits.

m. Place the channel B oscilloscope probe on A106MC27-14.

n. At the computer front panel, repeatedly press and release the SINGLE CYCLE switch and check the oscilloscope display for a 1.6 μs pulse every time the switch is pressed.

o. If all indications of the above test procedure are normal, the SINGLE CYCLE switch and circuits are operating normally.



NOTE:
1. ASTERISK (*) DENOTES A PIN ON A 48-PIN CONNECTOR.

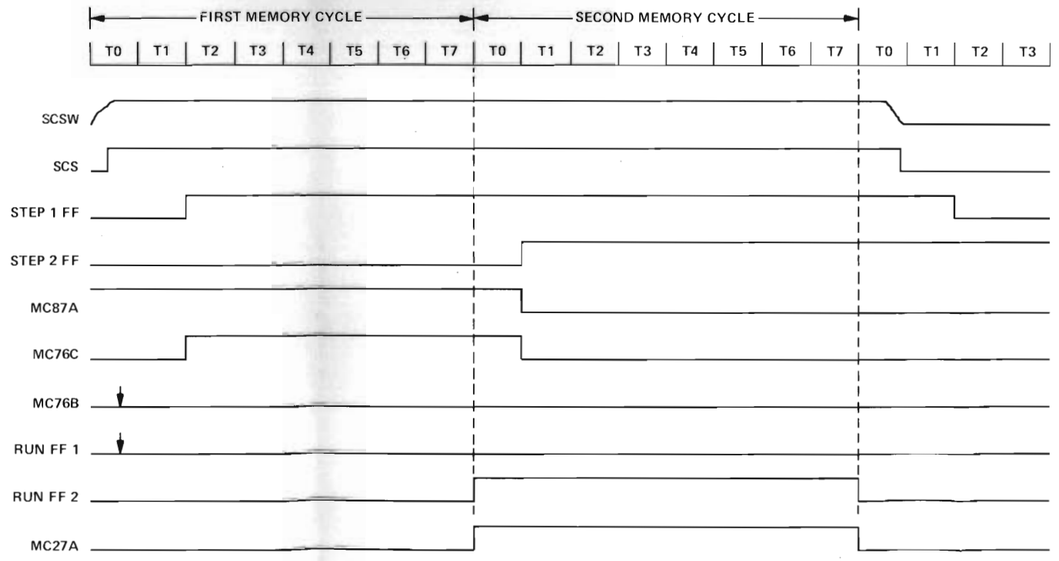


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Figure 4-10. SINGLE CYCLE Switch Circuit, Servicing Diagram

4-131. LOADER SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the LOADER switch S110 which is located on the control panel assembly A502.

4-132. Description. The circuits associated with the LOADER switch are shown in figure 4-11. In the following description it is assumed that the LOADER switch is in the PROTECTED position as shown.

4-133. The LOADER switch is a toggle type switch. When placed in the PROTECTED position, +4.5 volts is transferred through the switch and pin Y of front panel coupler card A101 as signal LPS. Signal LPS is transferred to pin 14 of "and" gate U54A. The other input pins of U54A are tied to the Memory Address Decoding signals that carry the uppermost 64 locations of memory. If signal LPS is true at pin 14 and one of these 64 locations is addressed, output signal MPT at pin 10 goes true. Signal MPT is transferred to pin 3 of U106, and to parity error card A15 via output pin 25. A true MPT signal disables U106 causing its output signals to go false. This disables all memory timing functions at the X-Y driver switch cards and sense amplifier cards and inhibits data transfer to or from memory.

4-134. Thus when the LOADER switch is in the PROTECTED position, data cannot be transferred into or out of the uppermost 64 locations of memory.

4-135. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-11, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check the +4.5-volt dc supply at pin 3 of A502S110. If normal, proceed to step "c". If abnormal, check the connection between A502S110-3 and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216), extend memory address decoder card A14 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

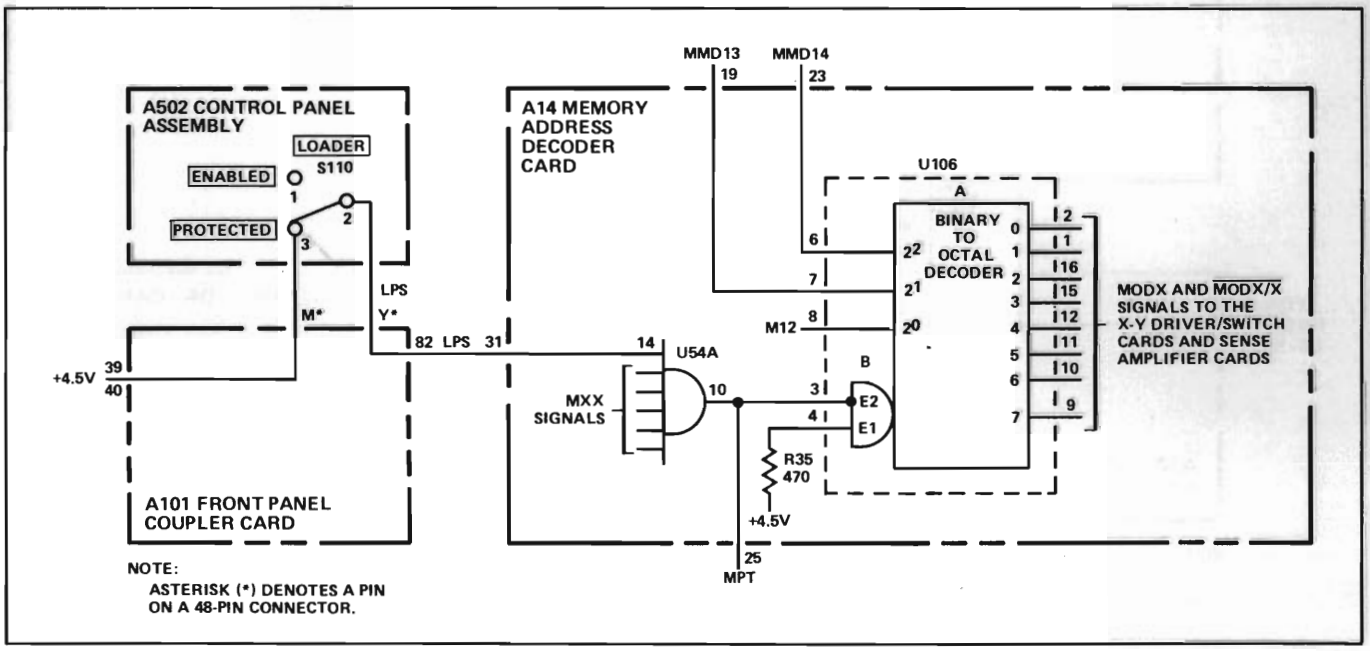
(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A14-31.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

f. At the computer front panel, turn on power. Assure that the LOADER switch is in the PROTECTED position and check the oscilloscope display for a +4.5-volt level. Then place the LOADER switch in the ENABLED position



2107-119

Figure 4-11. LOADER Switch Circuit, Servicing Diagram

and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A14-31 to A502S110-2 for continuity and check the LOADER switch for proper wiring and operation.

g. Place the channel A oscilloscope probe on pin 25 of the memory address decoder card.

h. At the computer front panel, assure that the LOADER switch is in the PROTECTED position and that the M-register is not addressing any of the uppermost 64 locations of memory. Then check the oscilloscope display for a logic 0 level.

i. Address any of the uppermost 64 locations of memory by placing the address in the switch register and pressing the LOAD ADDRESS switch. Check the oscilloscope display for a logic 1 level.

j. If the oscilloscope displays for steps "h" and "i" were abnormal, check A14U54A as the most probable cause of trouble. If the oscilloscope displays were normal, refer to paragraphs 4-458 and 4-474 and troubleshoot the memory address decoder card.

k. If all indications of the above test procedure are normal, the LOADER switch and circuits are operating normally.

4-136. MEMORY SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the MEMORY switch S111 located on display board assembly A501.

4-137. Description. The circuits associated with the MEMORY switch are shown in figure 4-12. In the following description it is assumed that the MEMORY switch is in the NORM position as shown.

4-138. The MEMORY switch is a slide type switch. When placed in the NORM position, it transfers the signal PON from power fail card A6, through front panel coupler card A101, and through the MEMORY switch and pin 17 of the front panel coupler card as signal MNS. Signal MNS is transferred from pin 22 of the front panel coupler card through the backplane wiring to pin 12 of timing generator card A106, to pin 7 of "and" gate MC27C which is the controlling gate for the signal MTE. When all inputs to MC27C are true the signal MTE will be generated and allow the transfer of data into and out of memory.

4-139. Thus when the MEMORY switch is in the NORM position, data can be transferred into or out of memory. When the switch is in the OFF position all memory data transfers are disabled.

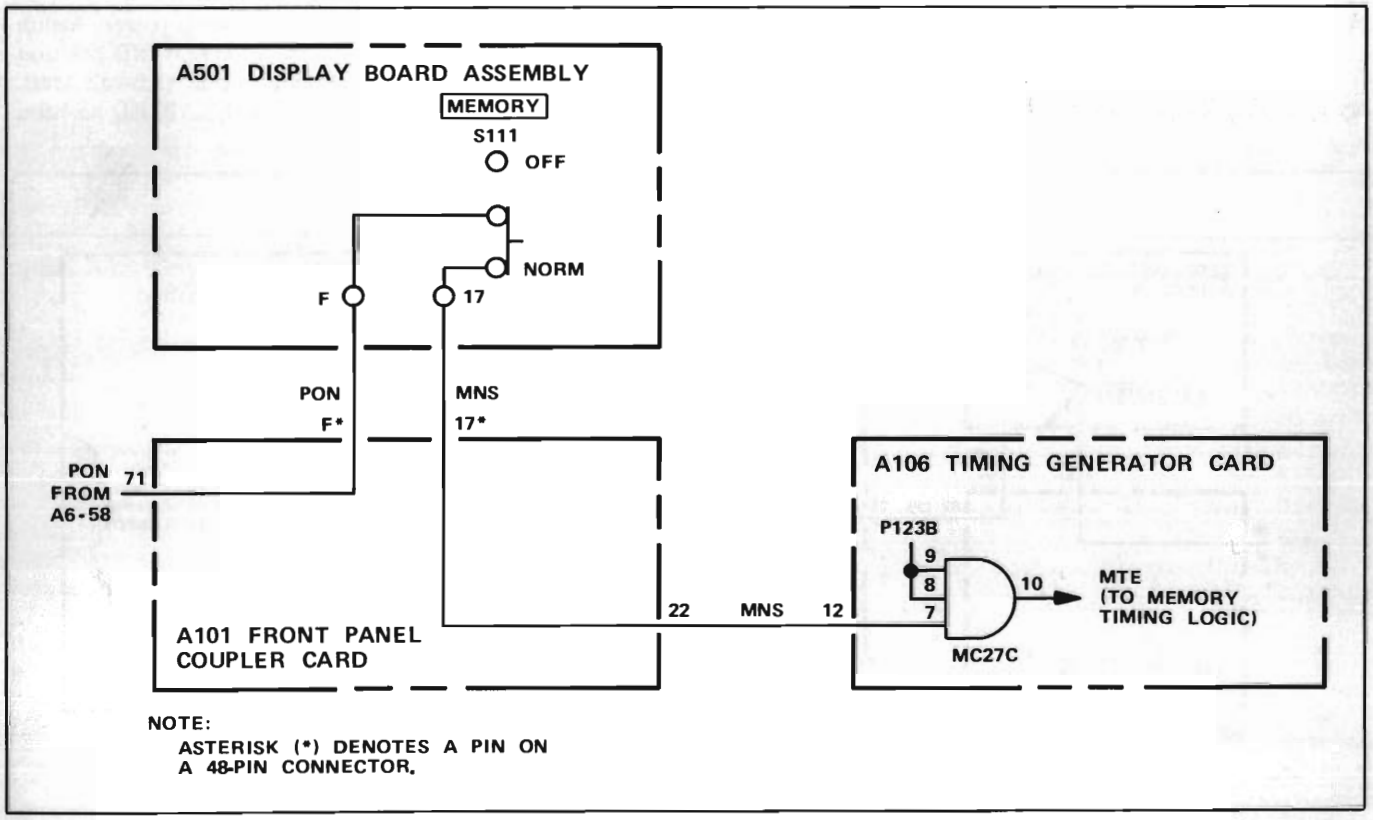


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Figure 4-12. MEMORY Switch Circuit, Servicing Diagram

4-140. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-12, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check for a +4.5-volt level at A501-F. If normal, proceed to step "c". If abnormal, check the connection between A501-F and A1-58 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216) and extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-12.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

f. At the computer display board assembly, turn on power. Assure that the MEMORY switch is in the NORM position and check the oscilloscope display for a +4.5-volt level. Then place the MEMORY switch in the OFF position and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A106-12 to A501-17 for continuity and check the MEMORY switch as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on pin 10 of A106MC27.

h. At the computer display board assembly, assure that the MEMORY switch is in the NORM position and check the oscilloscope display for a logic 1 level. Then place the MEMORY switch in the OFF position and check the oscilloscope for a logic 0 level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A106MC27 and the phase logic circuitry as the most probable cause of trouble.

i. If all indications of the above test procedure are normal, the MEMORY switch and circuits are operating normally.

4-141. PHASE SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the PHASE switch S112 located on display board assembly A501.

4-142. Description. The circuits associated with the PHASE switch are shown in figure 4-13. In the following description it is assumed that the PHASE switch is in the NORM position as shown.

4-143. The PHASE switch is a slide type switch. When placed in the NORM position, it transfers +4.5 volts through front panel coupler card A101, and through the PHASE switch and pin E of the front panel coupler card as signal PNS. Signal PNS is transferred from pin 18 of the front panel coupler card through the backplane wiring through pin 43 of timing generator card A106, to pin 7 of "and" gate MC35C. When the signal PNS goes false (The PHASE switch is placed in the LOOP position.) it disables MC35C and inhibits its output at pin 10, which is the clock pulse to the phase logic flip-flops. This causes the currently active phase to remain set.

4-144. Thus when the PHASE switch is in the NORM position, the phase flip-flops are clocked normally and change according to the computer logic. When the switch is in the LOOP position the clock pulse is inhibited and the phase logic cannot change.

4-145. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-13, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check for a +4.5-volt level at A501-M. If normal, proceed to step "c". If abnormal, check the connection between A501-M and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02116-6047), extend timing generator card A106 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

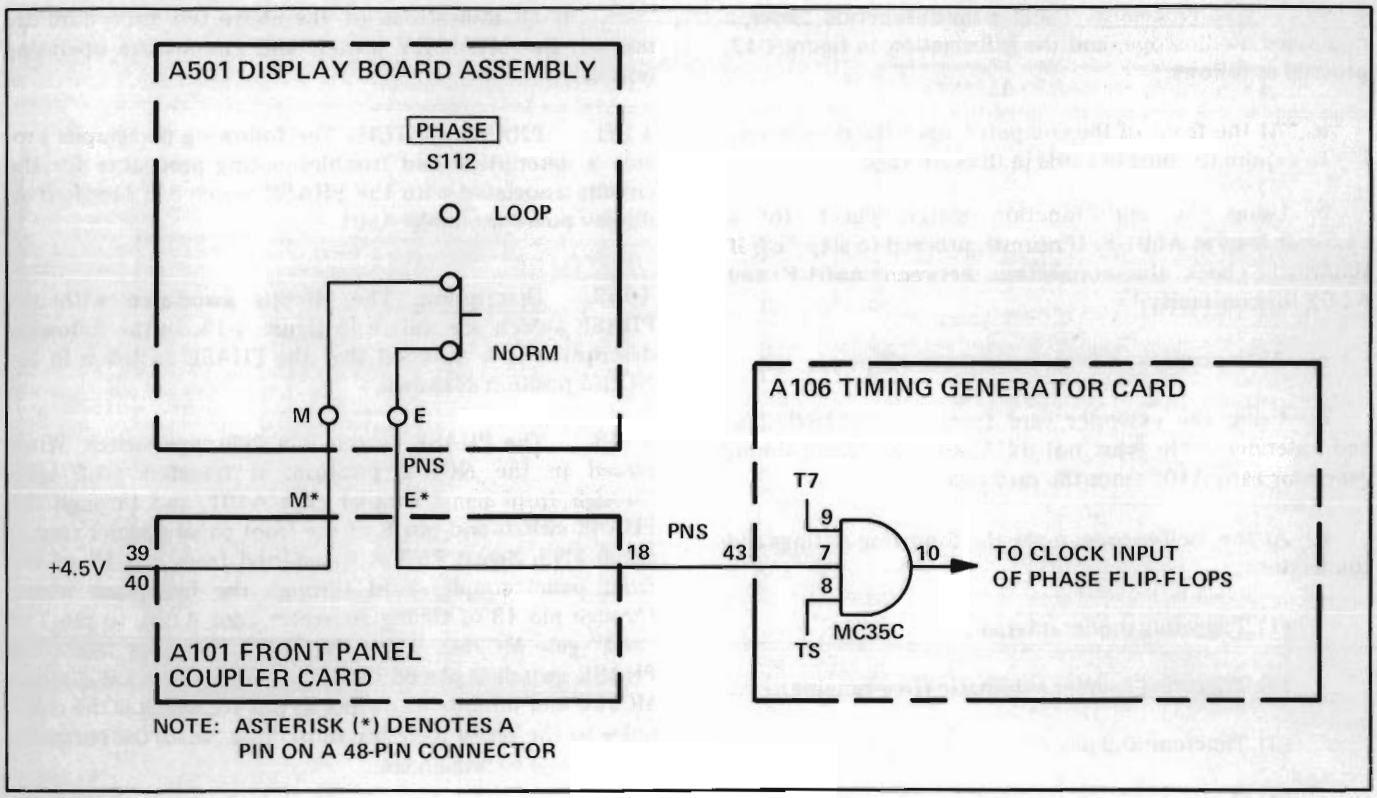

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Figure 4-13. PHASE Switch Circuit, Servicing Diagram

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-43.

f. At the computer display board assembly, turn on power. Assure that the PHASE switch is in the NORM position and check the oscilloscope display for a +4.5-volt level. Then place the PHASE switch in the LOOP position and check the oscilloscope for a 0-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A106-43 to A501-E for continuity and check the PHASE switch as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on A106MC35-10.

h. At the computer display board assembly, assure that the PHASE switch is in the NORM position and check the oscilloscope display for a 45 ηs to 55 ηs pulse occurring every 1.6 μs. Then place the PHASE switch in the LOOP position and check the oscilloscope display for a logic 0 level. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A106-MC35 as the most probable cause of trouble and refer to paragraph 4-153 and troubleshoot the basic timing circuits.

i. If all indications of the above test procedure are normal, the PHASE switch and circuits are operating normally.

4-146. INSTRUCTION SWITCH. The following paragraphs provide a description and troubleshooting procedure for the circuits associated with the INSTRUCTION switch S113 located on display board assembly A501.

4-147. Description. The circuits associated with the INSTRUCTION switch are shown in figure 4-14. In the following description it is assumed that the INSTRUCTION switch is in the NORM position as shown.

4-148. The INSTRUCTION switch is a slide type switch. When placed in the NORM position, it transfers 0-volts from the INSTRUCTION switch and pin H of the front panel coupler card A101 as signal ILS. Signal ILS is transferred from pin 26 of the front panel coupler card through the backplane wiring to pin 73 of instruction decoder card A107, to pin 7 of "and" gate MC106C. When the signal ILS goes true (the INSTRUCTION switch is placed in the LOOP position) it enables MC106C and causes its output at pin 10 to go true. This true output is transferred to pin 1 of "nor" gate MC96A and causes its output at pin 13 to go false. This false output is transferred to pin 14 of "and" gate MC97A and disables this gate which is the controlling gate for the signal SB0. By disabling MC97A the signal SB0 is inhibited and the P- and M-registers will remain in their current configuration.

4-149. Thus when the INSTRUCTION switch is in the NORM position, the signal SB0 can be generated and the normal incrementing of the P- and M-registers can take

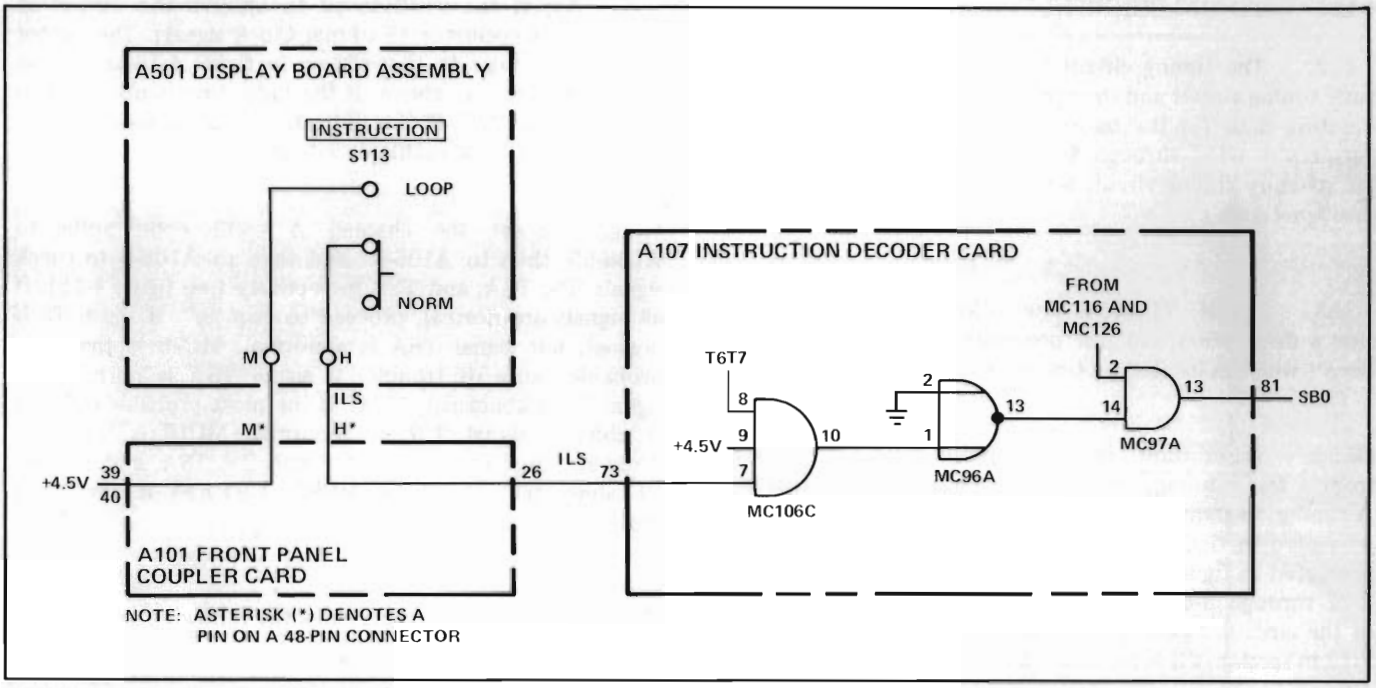

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Figure 4-14. INSTRUCTION Switch Circuit, Servicing Diagram

place. When the switch is in the LOOP position, signal SB0 cannot be generated and the P- and M-registers cannot be incremented.

4-150. Test Procedure. Using a multi-function meter, a dual-trace oscilloscope, and the information in figure 4-14, proceed as follows:

a. At the front of the computer, open the door assembly to expose the plug-in cards in the card cage.

b. Using the multi-function meter, check for a +4.5-volt level at A501-M. If normal, proceed to step "c". If abnormal, check the connection between A501-M and A101-39,40 for continuity.

c. At the computer front panel, turn off power.

d. Using the extender card (part no. 02116-63216), extend instruction decoder card A107 from the card cage.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 μs.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A107-73.

Note

Refer to section VII for the logic voltage levels required to drive a specific logic circuit. Refer to paragraph 4-51 and table 4-7 for additional information concerning waveforms and oscilloscope settings.

f. At the computer display board assembly, turn off power. Assure that the INSTRUCTION switch is in the NORM position and check the oscilloscope display for a 0-volt level. Then place the INSTRUCTION switch in the LOOP position and check the oscilloscope for a +4.5-volt level. If the oscilloscope display is normal, proceed to step "g". If the oscilloscope display is abnormal, check the connection from A107-73 to A501-M for continuity and check the INSTRUCTION switch as the most probable cause of trouble.

g. Place the channel A oscilloscope probe on A107MC96-13.

h. At the computer display board assembly, assure that the INSTRUCTION switch is in the NORM position and check the oscilloscope display for a +4.5-volt level. Place the INSTRUCTION switch in the LOOP position and check the oscilloscope display for a 400 ηs negative-going pulse occurring every 1.6 μs. If the oscilloscope display is normal, proceed to step "i". If the oscilloscope display is abnormal, check A107MC96 and A107MC106 as the most probable cause of trouble and refer to paragraph 4-153 and troubleshoot the basic timing circuits.

i. If all indications of the above test procedure are normal, the INSTRUCTION switch and circuits are operating normally.

4-151. TIMING CIRCUITS.

4-152. The timing circuit function is comprised of the basic timing circuit and the memory timing circuit. Troubleshooting data for the basic timing circuit is presented in paragraphs 4-153 through 4-155. Troubleshooting data for the memory timing circuit is presented in paragraphs 4-156 through 4-163.

4-153. BASIC TIMING. The following paragraphs provide a description and test procedure for the basic timing circuit which is located on timing generator card A106.

4-154. Description. Basic computer timing is derived from a free-running, crystal-controlled, 10-MHz oscillator. A timing diagram showing the basic timing signal outputs is presented in figure 4-15, and typical signal waveforms are presented in figures 4-16 through 4-20. Refer to paragraphs 3-27 through 3-31 in section III for a detailed description of the circuits used in generating these signals, and to figure 7-13 in section VII for a detailed logic diagram.

4-155. Test Procedure. Using a dual-trace oscilloscope and the diagrams referenced in the preceding paragraph, proceed as follows:

a. Place the POWER switch in the OFF position.

b. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

c. Place the POWER switch in the ON position.

d. Using the information provided in figure 4-16, check the 10-MHz oscillator output and time TO waveforms. (The 10-MHz waveform must have an overall amplitude of 2 to 7 volts peak-to-peak, with the positive-going peak reaching the +1.5-volt level or higher, and the negative-going peak reaching the +1-volt level or lower.) If both waveform indications are normal, proceed to step "j". If the waveforms cannot be displayed on the oscilloscope, perform steps "e" through "i" following.

e. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: automatic (free-running).

(3) Time/cm: 0.2 us.

(4) Channel A volts/cm: 0.2 (if using 10:1 probe).

(5) Channel A input: A106-3 (External Clock signal).

f. Adjust the oscilloscope to observe the output of the 10-MHz oscillator (External Clock signal). The output should be similar to that shown in figure 4-16 and as described in step "d" above. If the indication is normal, proceed to step "g". If the indication is abnormal, troubleshoot the 10-MHz oscillator circuit.

g. Connect the channel A oscilloscope probe to A106-55, then to A106-67 and then to A106-5 to check signals TS, TSA, and TSB respectively (see figure 4-15). If all signals are normal, proceed to step "h". If signal TS is normal, but signal TSA is abnormal, MC75 is the most probable cause of trouble. If signal TSA is normal, but signal TS is abnormal, MC42 is the most probable cause of trouble. If signal TSB is abnormal, MC16 is the most probable cause of trouble. If signals TS, TSA, and TSB are all abnormal, MC52 or MC82 (CF1 FF) is the most probable cause of trouble.

h. At the oscilloscope, make the following settings and connections:

(1) Triggering mode: internal.

(2) Triggering source: channel B.

(3) Time/cm: 0.2 us.

(4) Channel A and channel B volts/cm: 0.2 (if using 10:1 probes).

(5) Channel A input: MC62-14 (signal CL1).

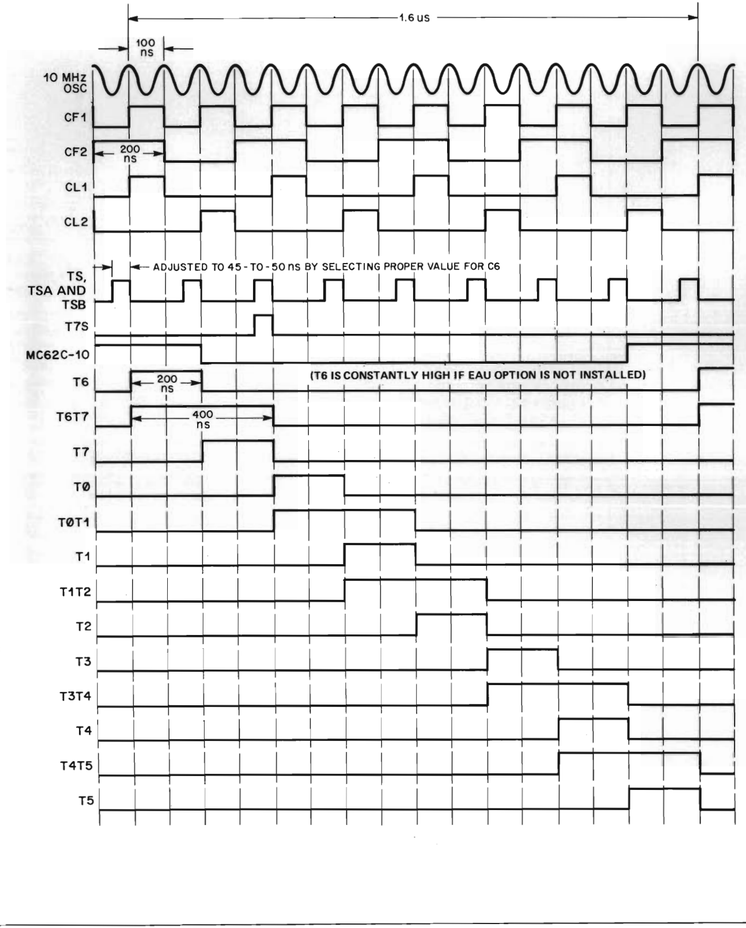
(6) Channel B input: A106-55 (signal TS).

i. Adjust the oscilloscope to observe signal CL1 on channel A (see figure 4-15). Then connect the channel A input to MC62-13 to observe signal CL2. If both signals are normal, troubleshoot the ring counter and the associated output and control gates. If both signals are abnormal, MC72 (CF2 FF) is the most probable cause of trouble. If one signal or the other is abnormal, but not both, MC62 is the most probable cause of trouble.

j. Using the information provided in figures 4-15 and 4-17 through 4-20, check the remaining signal outputs from the basic timing circuit. If all waveform indications are normal, the basic timing circuit is operating properly. If an abnormal waveform indication is observed, troubleshoot accordingly.

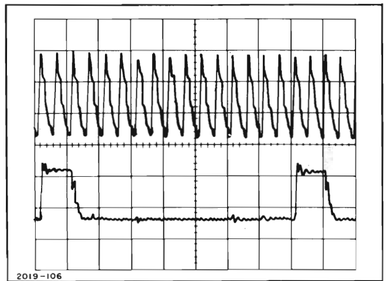
Note

To check the operation of the basic timing circuits during a 2.0-microsecond machine cycle, refer to the test procedure presented in paragraph 4-163 (steps "f" and "g").



2019-95A

Figure 4-15. Basic Timing Circuit, Timing Diagram



2019-106

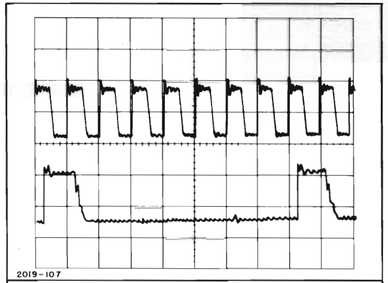
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (10 MHz):
Input A106-3
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-16. 10-MHz Oscillator Output and Time T0 Waveforms



2019-107

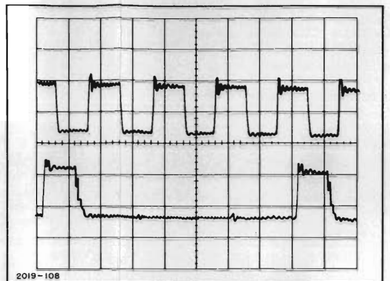
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (CF1):
Input A106MC82-13
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-17. Signal CF1 and Time T0 Waveforms



2019-108

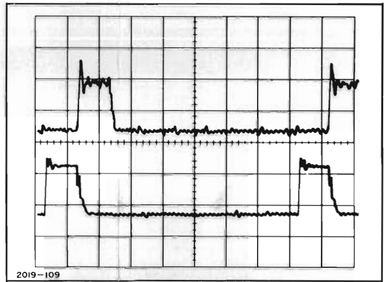
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (CF2):
Input A106MC72-13
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-18. Signal CF2 and Time T0 Waveforms



2019-109

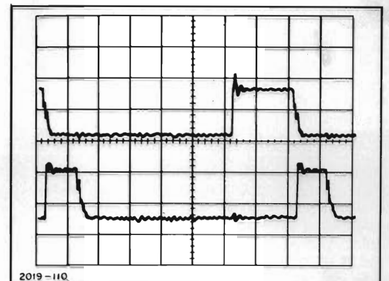
OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (T1):
Input A106-53
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-19. Time T1 and Time T0 Waveforms



2019-110

OSCILLOSCOPE CONNECTIONS AND SETTINGS

Channel A (T6T7):
Input A106-30
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-20. Time T6T7 and Time T0 Waveforms

UNFOLD FOR FIGURES 4-15 THRU 4-20

4-156. MEMORY TIMING. The following paragraphs provide a description and test procedure for the memory timing circuit which is located on timing generator card A106.

4-157. Description. The memory timing circuit is shown in detail in figure 7-13. Memory timing signals MRT1, MRT2, MST, MWT1, MWT2, and MIT control the read and write operations performed in the memory section of the computer. Memory timing signal MWL is a status signal used for control by the memory protect option and memory parity check option (refer to the applicable operating and service manuals for these options if installed in the computer).

4-158. The memory timing signals are derived from basic timing signal inputs which include $\overline{CF1}$, CF2, $\overline{CF2}$, T0, T0T1, T1T2, T2, T4T5, T5T6, and T6T7. The generation of the memory timing signals is controlled by signal inputs from the phase logic circuits (PH3 and P123B signals), A- and B-register addressing circuits (AAF and BAF signals), instruction decoding logic (JSB, STRX, and ISZ signals), MEMORY switch A501S111 and LOAD MEMORY switch A502S105 at the front panel (MNS and LMS signals), and the extended arithmetic unit option (ISG signal; refer to the operating and service manual for this option if installed in the computer).

4-159. Figures 4-21 through 4-32 show timing and waveforms for the memory read and write cycles occurring during a normal 1.6-microsecond machine cycle. In order for the memory timing signals to be generated as shown in figure 4-21, the state of the control signal inputs specified in the preceding paragraph must be such that gates MC27C and MC77C are enabled and providing true outputs, and gate MC104B is disabled and providing a false output. Under these circuit conditions, memory timing enable signal MTE is true, and the basic timing circuit generates a 1.6-microsecond machine cycle. (If gate MC27C is disabled, signal MTE will be false and all memory timing signal outputs will be inhibited during the machine cycle. If gate MC104B is enabled, the basic timing circuit will generate a 2.0-microsecond machine cycle and the memory timing signals will be generated as explained in paragraphs 4-160 through 4-162 which follow.) During the memory read cycle (time T0TS through T2), signals MRT1 and MRT2 are generated at the output of gates MC57A and MC17B, signal MSG is generated at the output of gate MC85A, and signal MST is generated at the output of gate MC57B. As noted in figure 4-21, the position of the leading edge of MRT1 ia controlled by the output of gate MC56D which is controlled by resistor R22 and capacitor C11. (Also note that if gate MC77C is disabled during the memory read cycle, signal MST will not be generated and signal MSG will be lengthened.) During the memory write cycle (time T3TS through T5), gate MC37B generates signal MIT. Note that the output from gate MC62C controls the length of the machine cycle (1.6-microsecond or 2.0-microsecond). This output is also connected to the gating structure for signals MWT1 and MWT2 to allow the memory write cycle to be delayed 400 nanoseconds during a 2.0-microsecond machine cycle. During a 1.6-microsecond machine cycle, signal MWL is inhibited and remains false (if the parity error option is installed), unless circuit conditions are such that gate MC77C is inhibited and causes gate MC55B to produce a true output. This signal is used in special cases to inhibit memory protect and parity error indications. During a 2.0-microsecond machine cycle, signal MWL is true and the memory protect and parity error indications are inhibited.

4-160. Figures 4-33 through 4-41 show timing and waveforms for a memory read and memory write cycle occurring when an ISZ instruction is processed and the machine cycle is stretched by an additional 0.4 microseconds. In order for the memory timing signals to be generated as shown in figure 4-33, the state of the control signal inputs specified in paragraph 4-158 must be such that gates MC27C, MC77C, and MC104B are enabled and providing true outputs. This circuit condition will exist only when an ISZ instruction is processed, and is the only condition under which the basic timing circuit will generate a 2.0-microsecond machine cycle. During the read portion of this machine cycle, the MRT, MSG, and MST signals are generated in exactly the same manner as described in the preceding paragraph. However, with the ISZ signal true, the operation of the basic timing circuit and the generation of the MIT, MWT1, and MWT2 signals is modified, as explained in the following paragraphs, due to the true signal output at gate MC104B.

4-161. The gating network consisting of gates MC124A, MC104A, MC124B, and MC62C controls the operation of the T6T7 FF in the basic timing circuit. During a normal 1.6-microsecond machine cycle, the output at MC62C is true during time T5T6, as shown in figures 4-15 and 4-33. This permits two consecutive CL1 clocking pulses to set the T6T7 FF at the 1.2-microsecond point in the machine cycle, and to reset the T6T7 FF at the 1.6-microsecond point in the machine cycle. With the output from gate MC104B true, however, the operation of the gating network is modified so that the output of MC62C is false during the time that the T6T7 FF is normally clocked. As shown in figure 4-33, this delays the clocking of the T6T7 FF by two time periods, or 0.4 microseconds, and a 2.0-microsecond machine cycle results.

4-162. Signal T6 is not generated during a 2.0-microsecond machine cycle because the T5T6 FF and the T6T7 FF are not set during the same time period as they normally are during a 1.6-microsecond machine cycle. This is shown in figure 4-33.

4-163. Test Procedure. Using a dual-trace oscilloscope and the diagrams referenced in the preceding description, proceed as follows:

a. At the computer front panel, turn off power.

b. Using the extender card (part no. 02116-63216) and the extender cable (part no. 02115-6047), extend timing generator card A106 from the card cage.

c. At the computer front panel, turn on power.

d. Proceed as follows:

Note

Steps (1) through (6) below contain a step-by-step procedure for manually loading a test program into the computer's memory. These instructions can be stored in any two consecutive memory locations in a memory page (other than protected, reserved, or unaccessible areas of memory). The locations specified below for these instructions are typical, and may be changed to any suitable area in memory not being used to prevent destroying program data or instructions already stored in the specified locations. If a starting address other than 001000 is used, modify the octal values accordingly for the SWITCH REGISTER settings given in steps (1), (3), and (5).

(1) Set the SWITCH REGISTER to 001000 (typical address for the first instruction) and press and release the LOAD ADDRESS switch.

(2) Set the SWITCH REGISTER to 003000 (CMA) and press and release the LOAD MEMORY switch.

(3) Set the SWITCH REGISTER to 027000 (JMP) and press and release the LOAD MEMORY switch.

(4) Set the SWITCH REGISTER to 177777 and press and release the LOAD A switch.

(5) Set the SWITCH REGISTER to 001000 (starting address) and press and release the LOAD ADDRESS switch.

(6) Press and release the RUN switch and proceed to step "e".

e. Using the information provided in figures 4-22 through 4-32, check the MRT1, MRT2, MSG, MST, MIT, MWT1, and MWT2 signal waveforms. If all waveform indications are normal, proceed to step "f". If one or more waveform indications are abnormal, refer to the timing information provided in figure 4-21, and to the applicable equations in table 7-37, and check the related timing and control input signals. If all input signals are normal, the trouble is in the memory timing circuit. (Check signal MTE as the first step of troubleshooting.) If one or more input signals are abnormal, troubleshoot the circuit functions providing the faulty input signal.

f. At the front panel of the computer, proceed as follows:

Note

Any three consecutive locations in a memory page can be used to store the program instructions specified in the following procedure. If a starting address other than 001000 is used, modify the octal values accordingly for the SWITCH REGISTER settings given in steps (1), (3), and (4).

(1) Set the SWITCH REGISTER to 001000 (typical address for the first instruction) and press and release the LOAD ADDRESS switch.

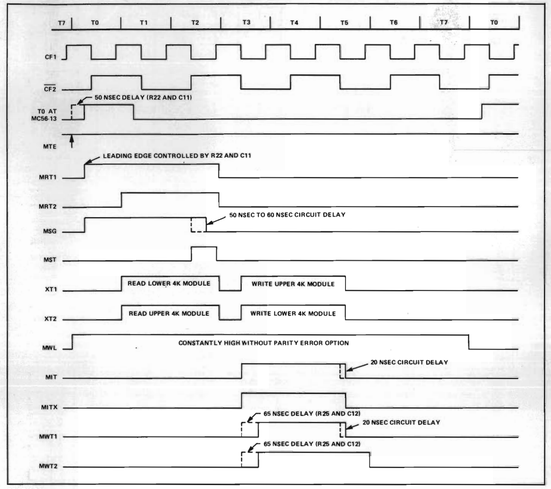
(2) Set the SWITCH REGISTER to 036006 (ISZ) and press and release the LOAD MEMORY switch.

(3) Set the SWITCH REGISTER to 027000 (JMP) and press and release the LOAD MEMORY switch twice.

(4) Set the SWITCH REGISTER to 001000 (starting address) and press and release the LOAD ADDRESS switch.

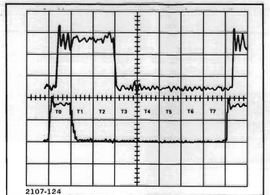
(5) Press and release the RUN switch. Then proceed to step "g".

g. Using the information provided in figures 4-34 through 4-41, check the MRT1, MRT2, MSG, MST, MIT, MWT1, MWT2, and MWL signal waveforms. If all waveform indications are normal, the memory timing circuit is operating properly. If one or more waveform indications are abnormal, refer to the timing information provided in figure 4-33, and to the applicable equations in table 7-37, and check the related timing and control input signals. If all input signals are normal, the trouble is in the memory timing circuit. (Check the signal output at gate MC104B as the first step of troubleshooting.) If one or more input signals are abnormal, troubleshoot the circuit functions providing the faulty input signal.



2107-121

Figure 4-21. Memory Timing Circuit (1.6 Microsecond Machine Cycle), Timing Diagram



2107-124

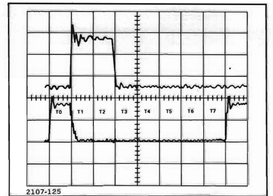
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MRT1)
Input A21-54
Volts/cm . . . . . .0.2 (if using 10:01 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-22. Signal MRT1 and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2107-125

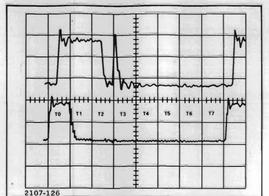
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MRT2):
Input A106-26
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-23. Signal MRT2 and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2107-126

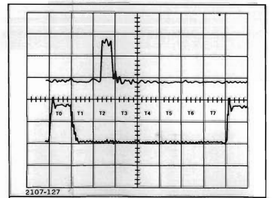
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MSG):
Input A106-19
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-24. Signal MSG and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2107-127

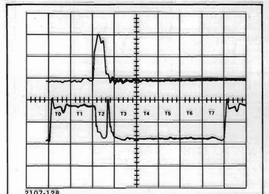
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MST)
Input A106-35
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-25. Signal MST and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2107-128

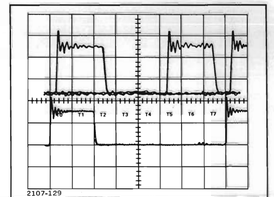
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MST)
Input A13-86
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (MSG):
Input A10-6
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-26. Signals MST and MSG Waveforms During 1.6 Microsecond Machine Cycle (Using LDA Instruction)



2107-129

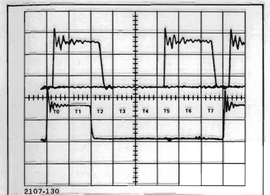
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (XT1):
Input A21-38
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (MITX):
Input A22-4
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-27. Signals XT1 and MITX Waveforms During 1.6 Microsecond Machine Cycle



2107-130

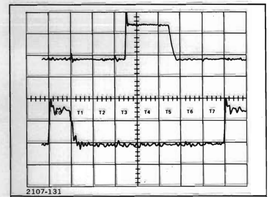
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (XT2):
Input A21-34
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (MITX):
Input A22-4
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-28. Signals XT2 and MITX Waveforms During 1.6 Microsecond Machine Cycle



2107-131

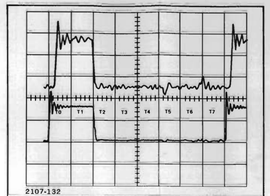
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MIT)
Input A106-25
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-29. Signal MIT and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2107-132

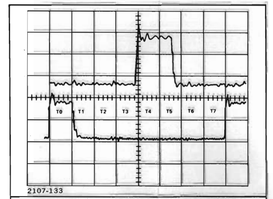
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWT1):
Input A21-50
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (MITX):
Input A22-4
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-30. Signals MWT1 and MITX Waveforms During 1.6 Microsecond Machine Cycle



2107-133

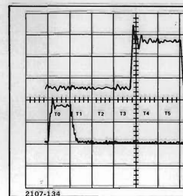
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWT1):
Input A106-35
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-31. Signal MWT1 and Time T0 Waveforms During 1.6 Microsecond Machine Cycle



2107-134

OSCILLOSCOPE CONNECTIONS

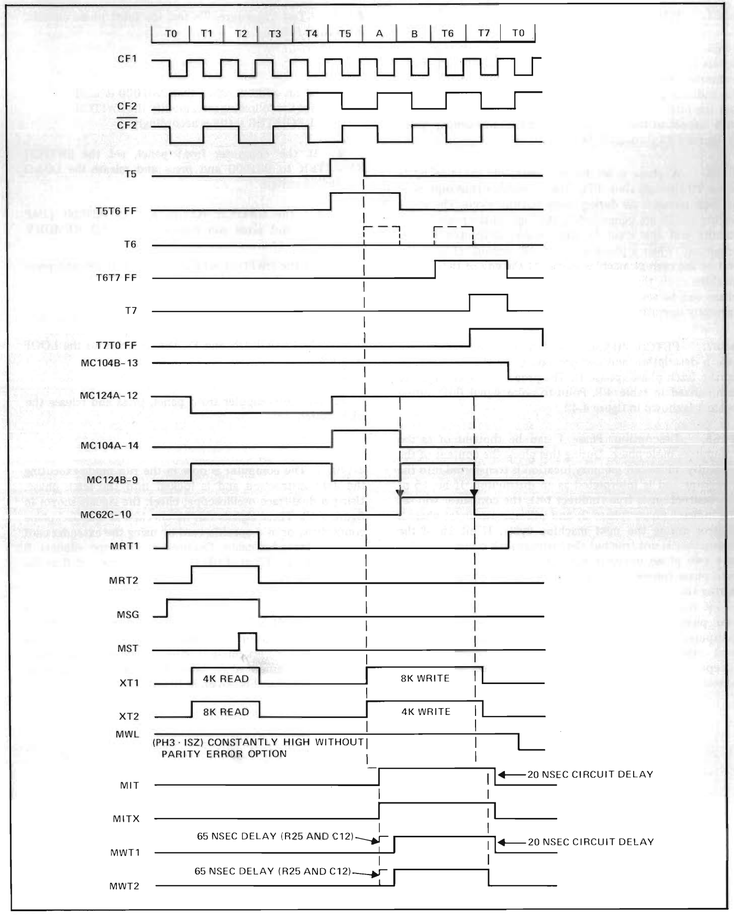
Channel A (MWT2):
Input . . . . . .
Volts/cm . . . . . .0.2 (if usi

Channel B (T0):
Input . . . . . .
Volts/cm . . . . . .0.2 (if usi

Time/cm . . . . . .

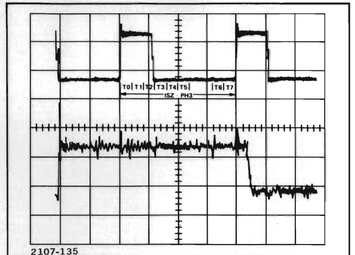
Figure 4-32. Signal MWTL and Time
During 1.6 Microsecon

UNFOLD FOR FIGU



2107-122

Figure 4-33. Memory Timing Circuit (2.0 Microsecond Machine Cycle), Timing Diagram



2107-135

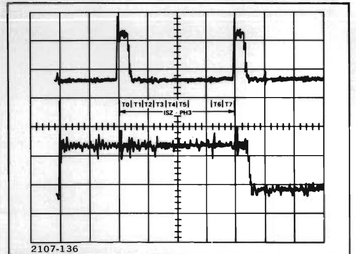
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MRT1):
Input A106-29
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-34. Signals MRT1 and ISZ Waveforms During 2.0 Microsecond Machine Cycle



2107-136

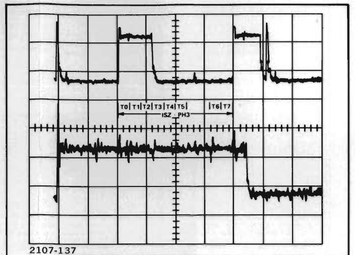
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MRT2):
Input A106-26
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-35. Signals MTR2 and ISZ Waveforms During 2.0 Microsecond Machine Cycle



2107-137

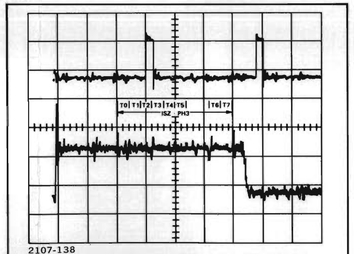
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MSG):
Input A106-19
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-36. Signals MSG and ISZ Waveforms During 2.0 Microsecond Machine Cycle



2107-138

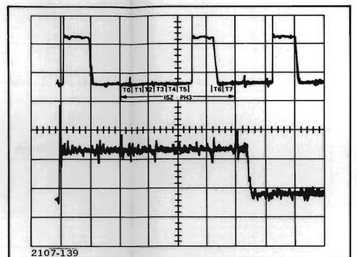
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MST):
Input A106-32
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-37. Signals MST and ISZ Waveforms During 2.0 Microsecond Machine Cycle



2107-139

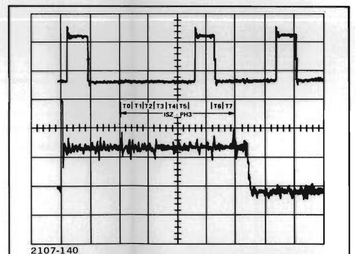
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MIT):
Input A106-25
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-38. Signals MIT and ISZ Waveforms During 2.0 Microsecond Machine Cycle



2107-140

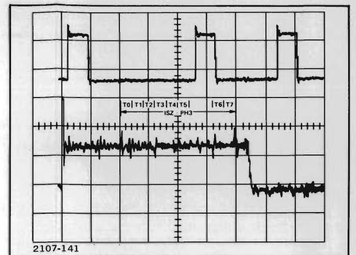
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWT1):
Input A106-35
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-39. Signals MWT1 and ISZ Waveforms During 2.0 Microsecond Machine Cycle



2107-141

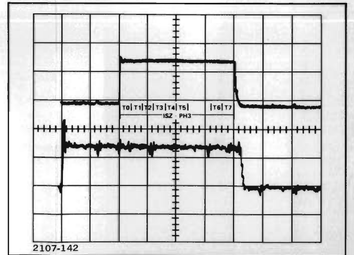
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWT2):
Input A106-20
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-40. Signals MWT2 and ISZ Waveforms During 2.0 Microsecond Machine Cycle



2107-142

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (MWL):
Input A106-33
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (ISZ):
Input A106-24
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.5 us

Figure 4-41. Signals MWL and ISZ Waveforms During 2.0 Microsecond Machine Cycle

UNFOLD FOR FIGURES 4-33 THRU 4-41

4-164. PHASE LOGIC CIRCUITS.

4-165. The phase logic circuits generate the control signals that provide the four machine phases for the basic computer. The four phases are the fetch phase (phase 1), the indirect phase (phase 2), the execute phase (phase 3), and the interrupt phase (phase 4). These phases are shown with respect to the basic timing and memory timing cycles in figures 4-42 through 4-44.

4-166. A phase is set for one complete machine cycle (time T0 through time T7). One or another (but only one) of these phases is set during every machine cycle. The phase setting signals are generated by the logic of the basic timing circuits and the logic of the various instructions being processed. When a phase is set, it will remain set until the end of the current machine cycle. At the end of the current machine cycle the same phase can remain set or a different phase can be set. But, a new phase cannot be set during a currently operating phase.

4-167. FETCH PHASE. The following paragraphs provide a description and test procedure for the circuits used by the fetch phase (phase 1). The processing operations are summarized in table 4-8. Point-to-point signal flow during phase 1 is shown in figure 4-42.

4-168. Description. Phase 1 can be thought of as the computers basic phase. During this phase the content of the currently addressed memory location is transferred into the T-register and is interpreted as an instruction. If bit 15 of the instruction is true (indirect bit), the computer will set the indirect phase (phase 2) and will operate under phase 2 control during the next machine cycle. If bit 15 of the instruction is not true but the instruction has been decoded as a two phase instruction, the computer will set the execute phase (phase 3) and will operate under phase 3 control during the next machine cycle. If bit 15 of the instruction is not true and the instruction has not been decoded as a two phase instruction, phase 1 will remain set and the computer will operate under phase 1 control during the next machine cycle. Phase 4 (interrupt) constitutes an exception to the above in that it takes precedence over the operation of all other phases upon their completion.

4-169. Test Procedure. To test the fetch phase circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board A501, set the INSTRUCTION and PHASE switches to the LOOP position.

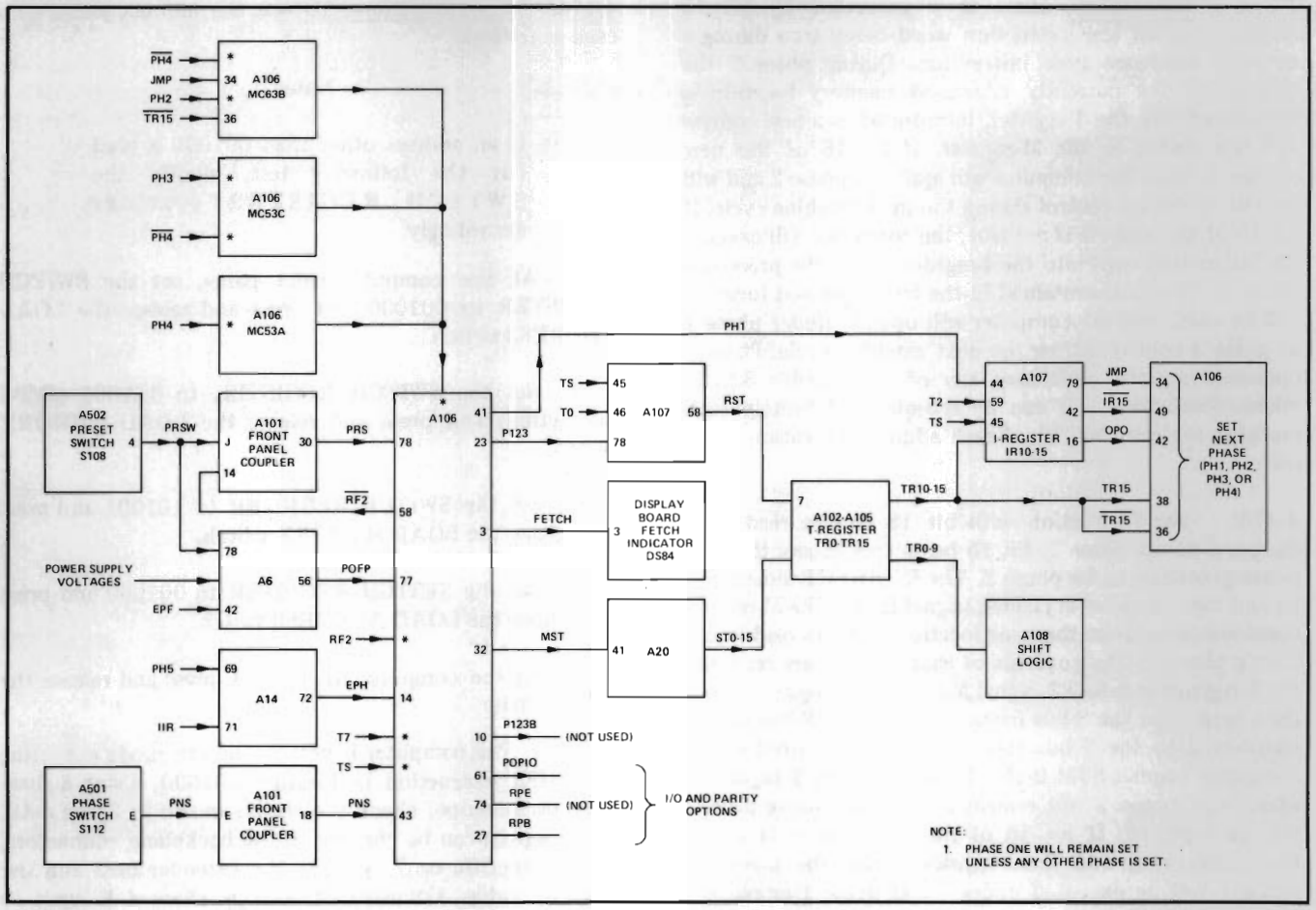
e. At the computer front panel, press and release the RUN switch.

4-170. The computer is now in the run mode executing the JMP instruction and is locked into the fetch phase. Using a dual-trace oscilloscope, check the signals shown in figure 4-42. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

4-171. INDIRECT PHASE. The following paragraphs provide a description and test procedure for the circuits used by the indirect phase (phase 2). The processing operations are summarized in table 4-9. Point-to-point signal flow during phase 2 is shown in figure 4-43.

Table 4-8. Fetch Phase Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear IR	Clear TR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 in M (10-15) If I: Set PH2 If D: Set PH3	



2107-165

Figure 4-42. Fetch Phase Circuit, Servicing Diagram

4-172. Description. Phase 2 is generated by bit 15 (indirect bit) of the instruction word being true during a memory reference type instruction. During phase 2 the content of the currently addressed memory location is transferred into the T-register, interpreted as a new address and transferred to the M-register. If bit 15 of this new address is true, the computer will again set phase 2 and will operate under its control during the next machine cycle. If bit 15 of the address is not true, the computer will execute the instruction read into the I-register during the preceding phase 1. The data contained in the last addressed location will be used, and the computer will operate under phase 1 or phase 3 control during the next machine cycle. Phase 2 operation permits addressing any of the possible 32,768 memory locations and can be repeated indefinitely each machine cycle by bit 15 of each addressed location being true.

4-173. The instruction with bit 15 true is read from memory during phase 1. Bit 15 being true causes the next phase generated to be phase 2. The INDIRECT indicator is lit and the T-register is cleared (signal RST). The M-register continues to address the same location that was read into it during phase 1. The contents of that location are read into the T-register at time T2 (signal MST). The T-register data is then read onto the S-bus (signal RTSB). The S-bus data is transferred to the T-bus (signal $\overline{\text{EOF}}$) and stored in the M-register (signals STM 0-15). If bit 15 of the T-register is again true, phase 2 will remain set and the above process will be repeated. If bit 15 of the T-register is false, the instruction read into the I-register during the preceding phase 1 will be executed under either phase 1 or phase 3 control using the data contained in the last addressed location.

4-174. Test Procedure. To test the indirect phase, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 127001 (JMP-I instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 101001 and press and release the LOAD MEMORY switch.

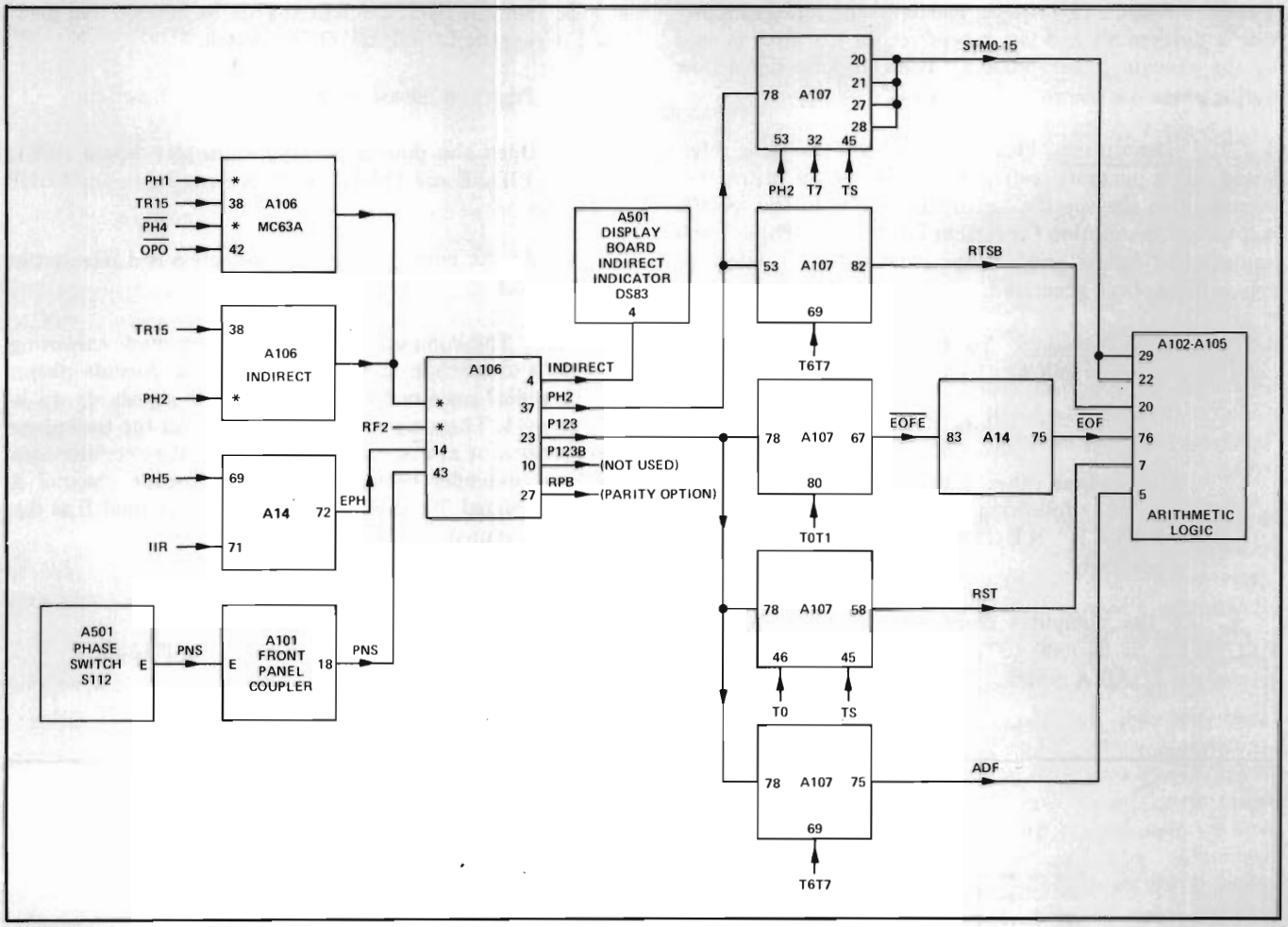
d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. At the computer front panel, press and release the RUN switch.

4-175. The computer is now in the run mode executing the JMP-I instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-43. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Table 4-9. Indirect Phase Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
INDIRECT	2	Clear TR						TR to M If I: Set PH2 If D: Set PH3	
JMP-I	2	Clear TR						If D: TR to P, M and set PH1 If I: TR to M and set PH2	



2107-166

Figure 4-43. Indirect Phase Circuit, Servicing Diagram

4-176. EXECUTE PHASE. The following paragraphs provide a description and test procedure for the circuits used by the execute phase (phase 3). Point-to-point signal flow during phase 3 is shown in figure 4-44.

4-177. Description. Phase 3 processes the data referenced by a memory reference or two-phase instruction according to the specific instruction. Refer to the specific instruction description for further information. Phase 1 will immediately follow phase 3 operation unless an interrupt (phase 4) has been generated.

4-178. Test Procedure. To test the EXECUTE phase circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 070000 (STA instruction) and press and release the LOAD A switch.

b. Set the SWITCH REGISTER to 000000 and press and release the LOAD ADDRESS switch.

c. Press and release the SINGLE CYCLE switch.

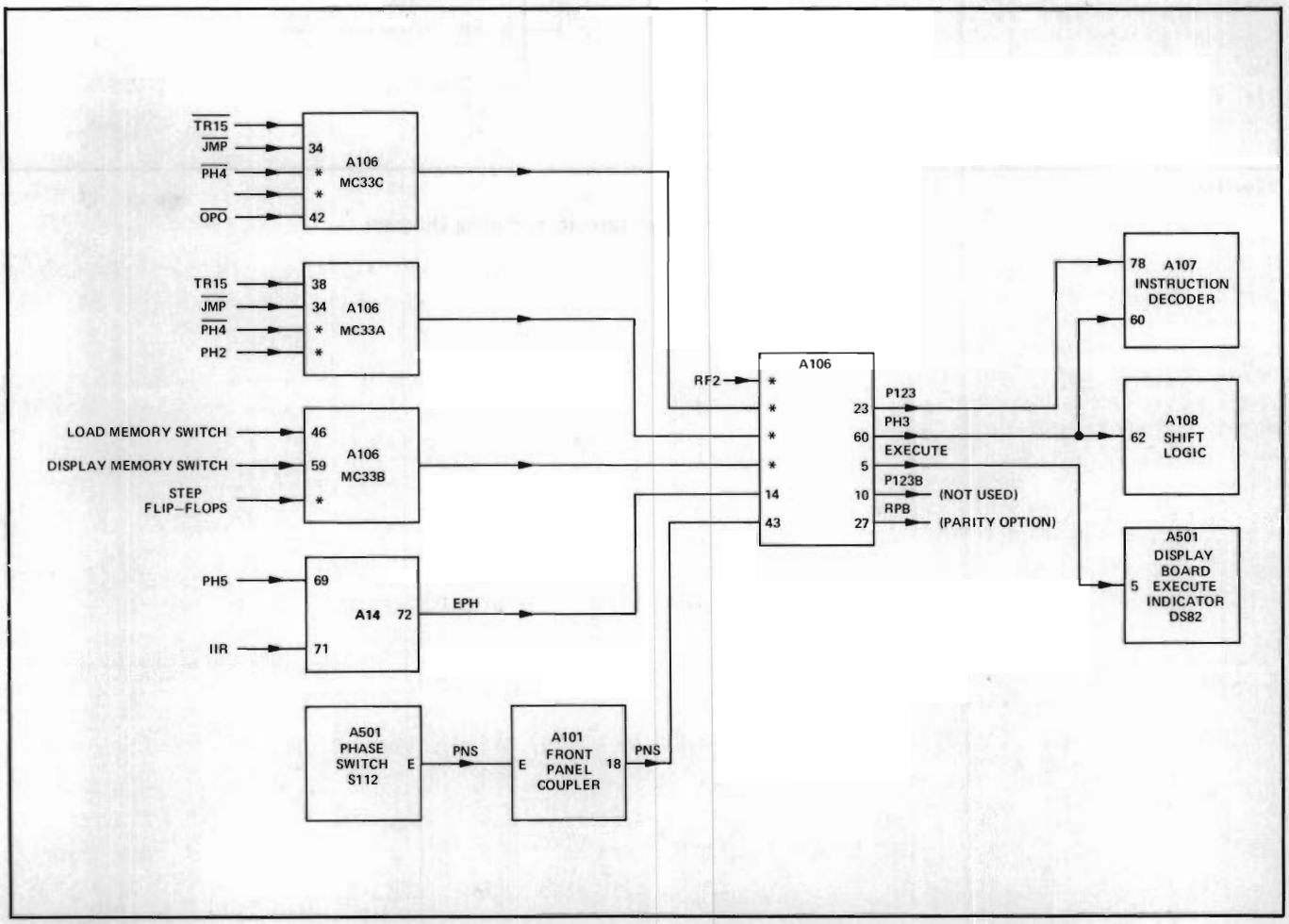
d. Open the door assembly. At display board A501, set the PHASE and INSTRUCTION switches to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

4-179. The computer is now in the run mode executing the STA instruction and is locked into the execute phase. Using a dual-trace oscilloscope, check the signals shown in figure 4-44. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Note

Signal PNS is inhibited when the PHASE switch is in the LOOP position.



2107-167

Figure 4-44. Execute Phase Circuit, Servicing Diagram

4-180. INTERRUPT PHASE. The following paragraphs provide a description and test procedure for the circuits used by the interrupt phase (phase 4). The processing operations are summarized in table 4-10. Point-to-point signal flow during phase 4 is shown in figure 4-45.

Note

If the PRESET indicator is on, the INTERRUPT PHASE is inoperative. The priority chain is broken by PRESET. Refer to paragraph 4-81 for a description of this indicator and related circuits.

4-181. Description. Any input/output device attached to the computer can interrupt computer operation by requesting to be serviced. The power-fail interrupt feature of the basic computer and the direct memory access, memory protect, and parity error optional feature can also generate the interrupt phase. When service is requested by a device, phase 4 is generated. At the end of the currently operating phase, phase 4 will be activated (exceptions to this are the JMP-I and JSB instructions). Phase 4 causes the P-register to be decremented by one and the select code of the interrupting device to be forced into the M-register forming the address of the next instruction. Phase 1 is then set and the computer is ready to process the instruction in the interrupt location. Phase 4 cannot occur again until phase 1 is complete (exceptions to this are the JMP-I instruction which must complete phase 1 and phase 2, and the JSB instruction which must complete two phase-one operations).

4-182. During times T1 through T5 of phase 4, the P-register number is read onto the R-bus (signal RPRB), complemented and transferred to the T-bus (signal CMF), stored back into the P-register (signal STP 0-15), read onto the R-bus again (signal RPRB), incremented and transferred to the T-bus (signals SBO and ADF), stored back into the P-register (signal STP 0-15), read for the third time onto the R-bus (signal RPRB), complemented and transferred to the T-bus (signal $\overline{\text{CMF}}$), and stored in the P-register (signal STP 0-15). Thus the P-register is decremented by one.

4-183. During time T7 bits 6 through 15 of the M-register are cleared (signal RSM 6-15), the interrupt address is read directly onto the T-bus from the central interrupt register which is located on the I/O Address card (part no. 02116-6194), signals TB0 through TB5, and stored into the M-register (signal STM 0-5). Phase one is set and the computer is ready to process the instruction in the interrupt address.

4-184. Test Procedure. To test the interrupt phase circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly. The following test requires that an input/output device interface card be plugged into slot 203 of the computer. The I/O device must be connected and in the ready state.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 103100 (CLF-0 instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 102100 (STF-0 instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 102700 (STC-0 instruction) and press and release the LOAD MEMORY switch.

e. Set the SWITCH REGISTER to 102110 (STF-10 instruction) and press and release the LOAD MEMORY switch.

Table 4-10. Interrupt Phase Processing Operations

TIME PERIODS	T0	T1	T2	T3	T4	T5	T6	T7
INTERRUPT 4		Read P to R Bus CMF Store T Bus in P		Read P to R Bus Read "1" to S Bus ADF Store T Bus in P		Read P to R Bus CMF Store T Bus in P		Reset M (6-15) Store T Bus (0-5) in M Set PH1

f. Set the SWITCH REGISTER to 102710 (STC-10 instruction) and press and release the LOAD MEMORY switch.

g. Set the SWITCH REGISTER to 102000 (HLT instruction) and press and release the LOAD MEMORY switch.

h. Set the SWITCH REGISTER to 000000 (NOP instruction) and press and release the LOAD MEMORY switch.

i. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

j. Set the SWITCH REGISTER to 000010 (interrupt location) and press and release the LOAD ADDRESS switch.

k. Set the SWITCH REGISTER to 002004 (INA instruction) and press and release the LOAD MEMORY switch.

l. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

m. Continuously press and release the RUN switch. The A-register will increment by one if the interrupt circuits are operating correctly.

Note

Refer to Section III of this manual and to Volume Three for additional input/output section information.

4-185. If the A-register does not increment by one, indicating the interrupt circuits are not operating properly, proceed as follows:

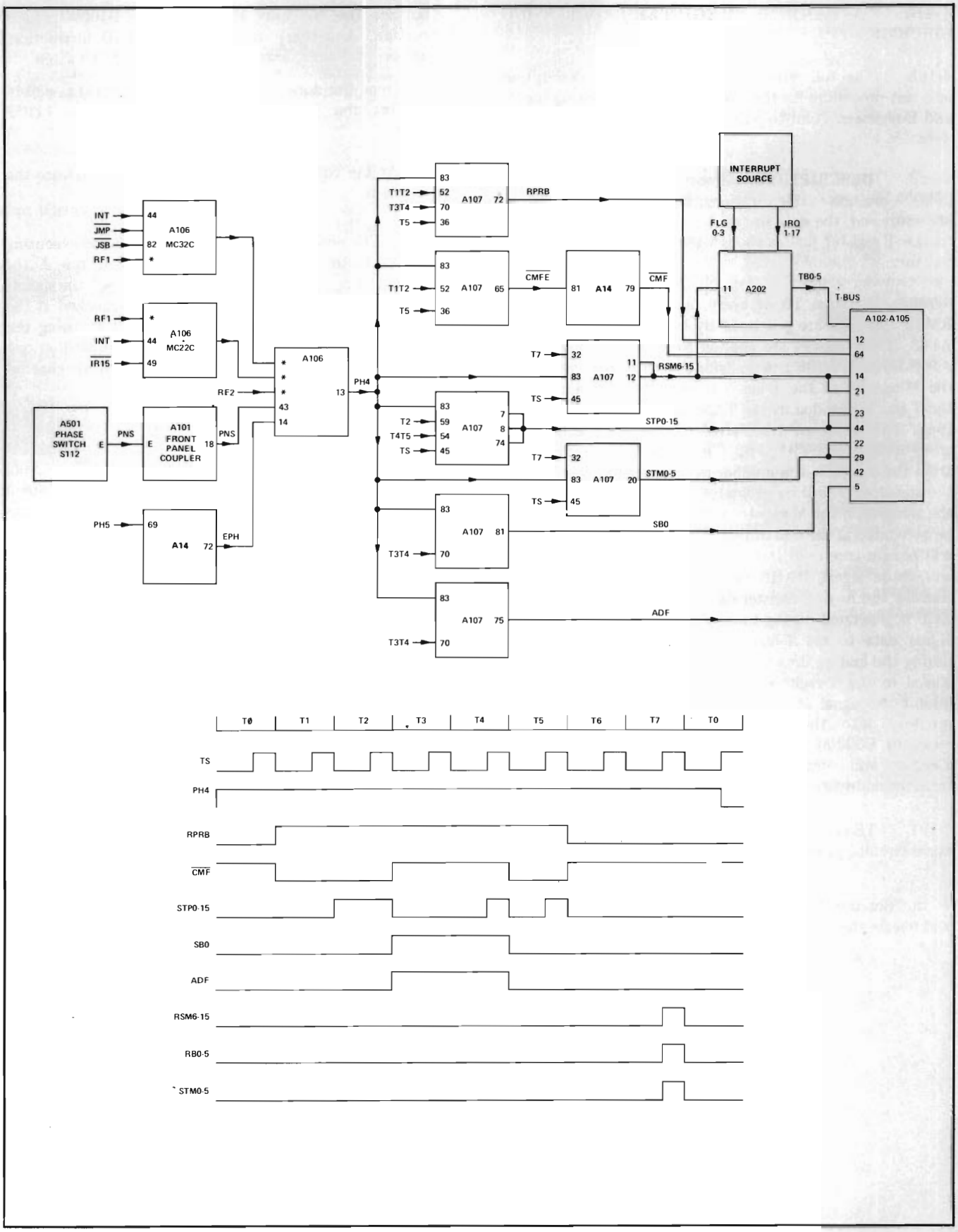
a. Set the SWITCH REGISTER to 001005 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 000000 (NOP instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Press and release the RUN switch.

4-186. The computer is now in the run mode continuously looping the program beginning at location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-45. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source. Set oscilloscope time/cm for 2 μs per division.



2107-168

Figure 4-45. Interrupt Phase Circuit, Servicing Diagram

4-187. A- AND B- REGISTER ADDRESSING CIRCUITS.

4-188. The following paragraphs provide a description and test procedure for the circuits used in addressing the A- and B-registers. Point-to-point signal flow is shown in figure 4-46.

4-189. DESCRIPTION. Memory locations 000000 and 000001 are non-usable locations. Whenever these locations are addressed, the data in the A- or B-register is transferred to the T-register just as though the data was coming from memory.

4-190. At time T0 of every machine cycle the signals RMSB and $\overline{EOF}$ are generated by instruction decoder card A108. These signals are applied to arithmetic logic cards A102 through A105 and transfer the number contained in the M-register to the T-bus via the S-bus. The number on the T-bus is decoded by the TAN gates and the signals from these TAN gates are transferred to shift logic card A108 along with signals TB1, TB2, TB3, TB12, TB13, and TB14 from the T-bus. If the number in the M-register is 000000, the signal AAF will be generated at the end of time T0. If the number in the M-register is 000001, the signal BAF will be generated at the end of time T0. The signal AAF or BAF will remain true until the following time T0. AAF or BAF will cause signal RARB or RBRB to be generated and transfer the A- or B-register data onto the R-bus. The signal $\overline{EOF}$ is generated during times T0 and T1 and transfers the R-bus data to the T-bus. The signal STBT is generated during the end of time T1 and causes the T-bus data to be stored in the T-register. Either signal AAF or BAF will inhibit the signal MST and prevent data being read from memory into the T-register. Thus, when addressing locations 000000 or 000001, the data displayed in the T-register will come from either the A- or B-register and not from the addressed memory location.

4-191. TEST PROCEDURE. To test the AAF or BAF signal circuits, proceed as follows:

a. Set the SWITCH REGISTER to 000000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 010000 (AND instruction, A-register) or to 010001 (AND instruction, B-register) and press and release the LOAD A switch.

c. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

d. At the computer front panel, press and release the RUN switch.

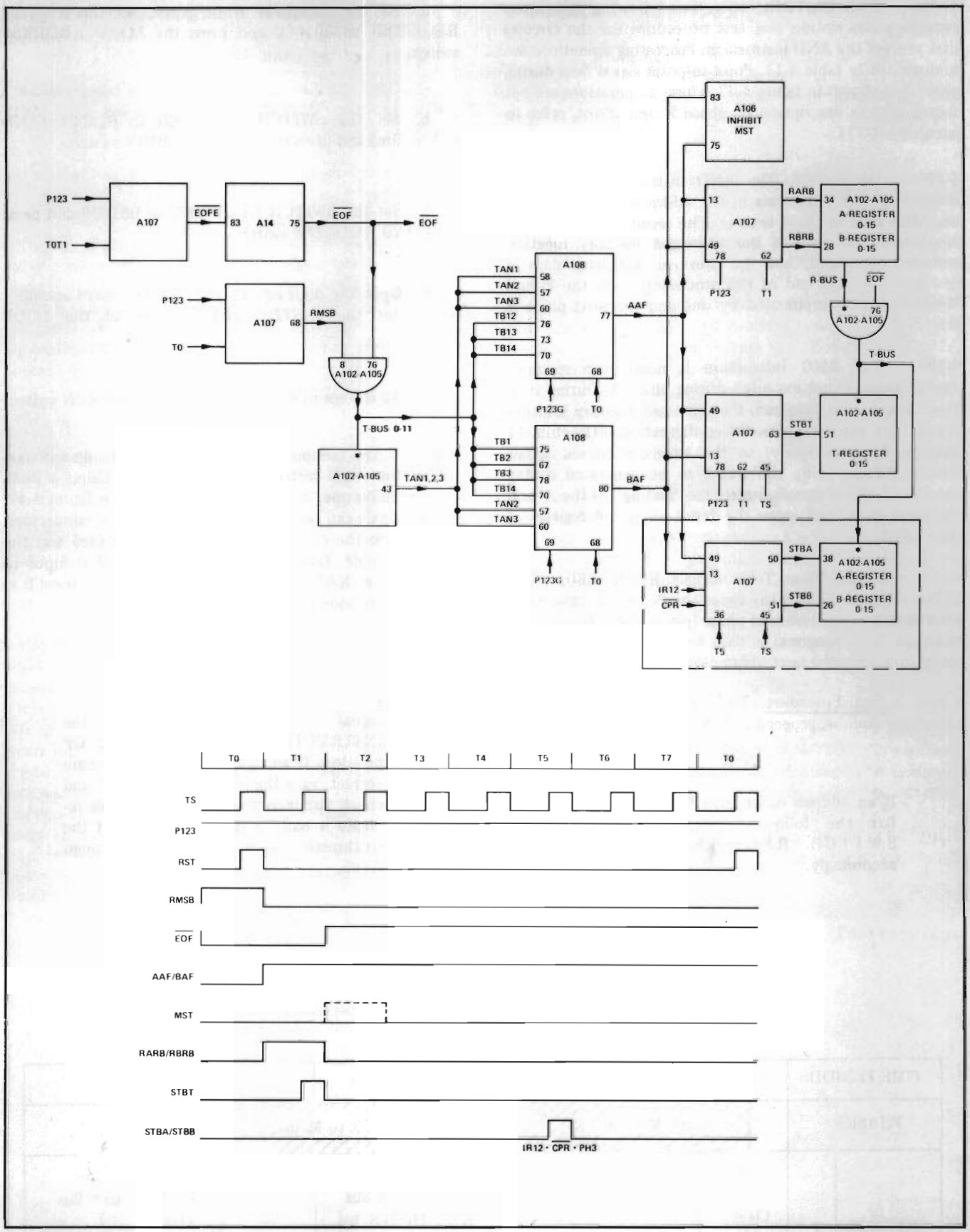
4-192. The computer is now in the run mode executing the AND instruction and referencing either the A- or B-register. Using a dual-trace oscilloscope, check the signals shown in figure 4-46. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

4-193. MEMORY REFERENCE INSTRUCTION PROCESSING CIRCUITS.

4-194. The circuits that process the 14 memory reference instructions are shown in figures 4-47 through 4-56. Memory reference instructions are used in the computer program to address a selected memory location and specify a desired arithmetic or control operation involving the memory location which is addressed. The format for these instructions is shown in figure 4-1. The paragraphs which follow describe the purpose and use of each instruction and explain how the processing circuits implement and execute the instructions. Tables summarizing the processing operations, and servicing diagrams showing signal flow and timing within the processing circuits, are included for reference during explanation and troubleshooting. Suggested troubleshooting test procedures are presented for each instruction.



2107-169

Figure 4-46. A- and B-Register Addressing Circuits, Servicing Diagram

4-195. AND INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the AND instruction. Processing operations are summarized in table 4-11. Point-to-point signal flow during phase 3 is shown in figure 4-47. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-196. Description. The AND instruction is used to combine ("and") the data in the addressed memory location with data in the A-register. The result is stored in the A-register. The data in the addressed memory location remains unchanged, but the previous A-register data is destroyed. At the end of the processing cycle the P- and M-registers are incremented by one and the next phase is set.

4-197. The AND instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the data from the addressed memory location is read into the T-register. Bit configuration 0010 (bits 14 through 11 respectively) in the I-register causes signals RARB, RTSB, ANF, and STBA to be generated during time T3T4. These signals control the "anding" of the A- and T-register data, and store the result in the A-register at time T4TS.

4-198. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-199. Test Procedure. To test the AND instruction processing circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 013001 (AND instruction) and press the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press the RUN switch.

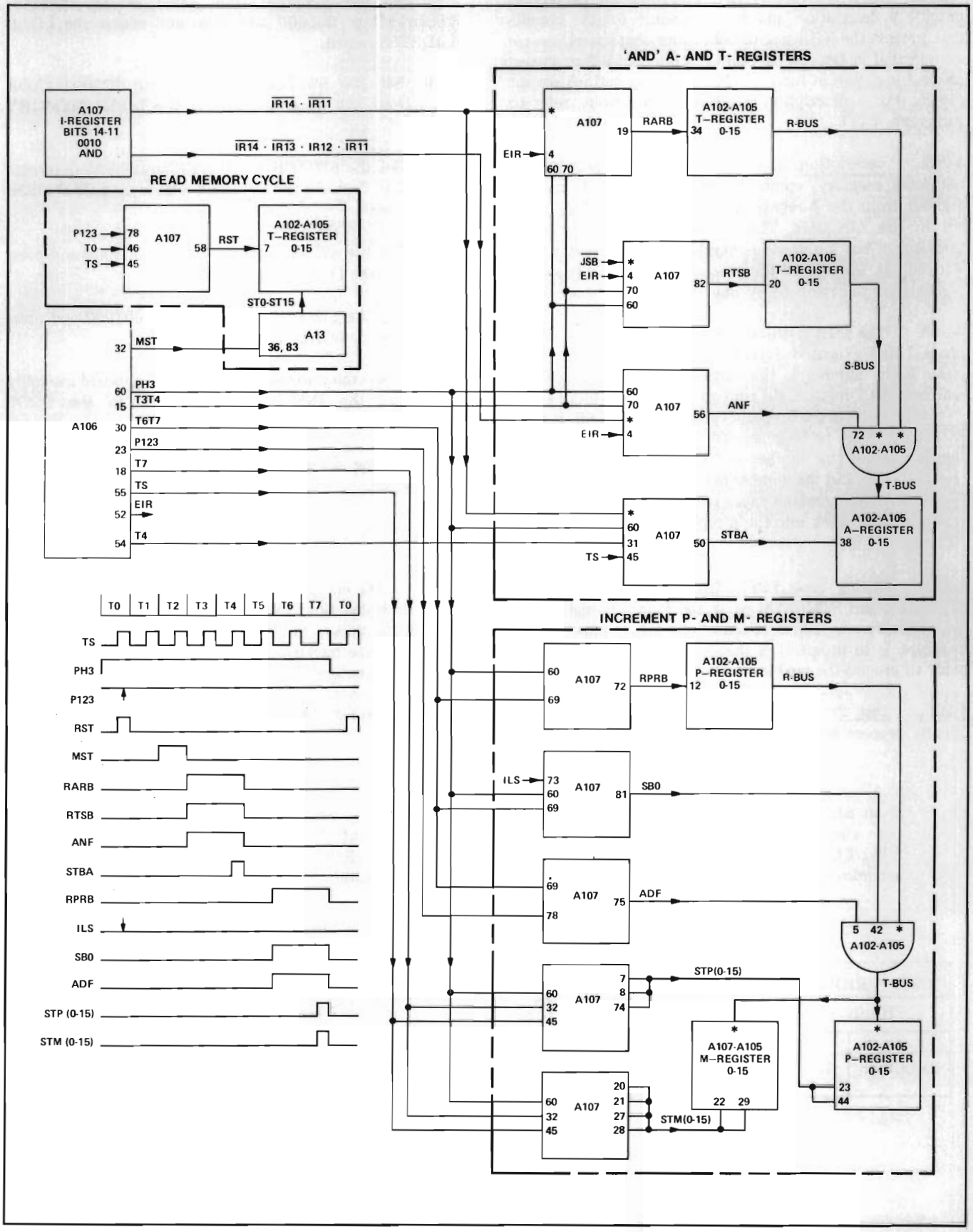
4-200. The computer is now in the run mode and executing the AND instruction continuously. Using a dual-trace oscilloscope, check the signals shown in figure 4-47. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position. If all signals indicated above are correct, vary the data being "anded" and check for incorrect results. This will indicate a bad "and" gate on one of the Arithmetic Logic cards, A102 through A105.

Table 4-11. AND Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASES			READ (Mem to TR)			WRITE (TR to Mem)			
EXECUTE	3	Clear TR			Read A to R Bus Read TR to S Bus ANF Store T Bus in A			Read P to R Bus Read "1" to S Bus ADF Store T Bus in P, M Set next phase	



2107-170

Figure 4-47. AND Instruction Processing Circuits, Servicing Diagram

4-201. XOR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the XOR instruction. Processing operations are summarized in table 4-12. Point-to-point signal flow during phase 3 is shown in figure 4-48. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-202. Description. The XOR instruction reads a number from memory, combines that number with another number from the A-register, and stores the resulting number in the A-register. The number in memory remains unchanged, but the previous number in the A-register is destroyed. At the end of the processing cycle the P- and M-registers are incremented by one and the next phase is set.

4-203. The XOR instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 0100 (bits 14 thru 11 respectively) in the I-register causes signals RTSB, RARB, $\overline{EOF}$, and STBA to be generated during time T3T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), and the number in the A-register to the R-bus (signal RARB), combine these numbers (signal $\overline{EOF}$), and read the result back into the A-register via the T-bus (signal STBA).

4-204. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-205. Test Procedure. To test the XOR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 023001 (XOR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the RUN switch.

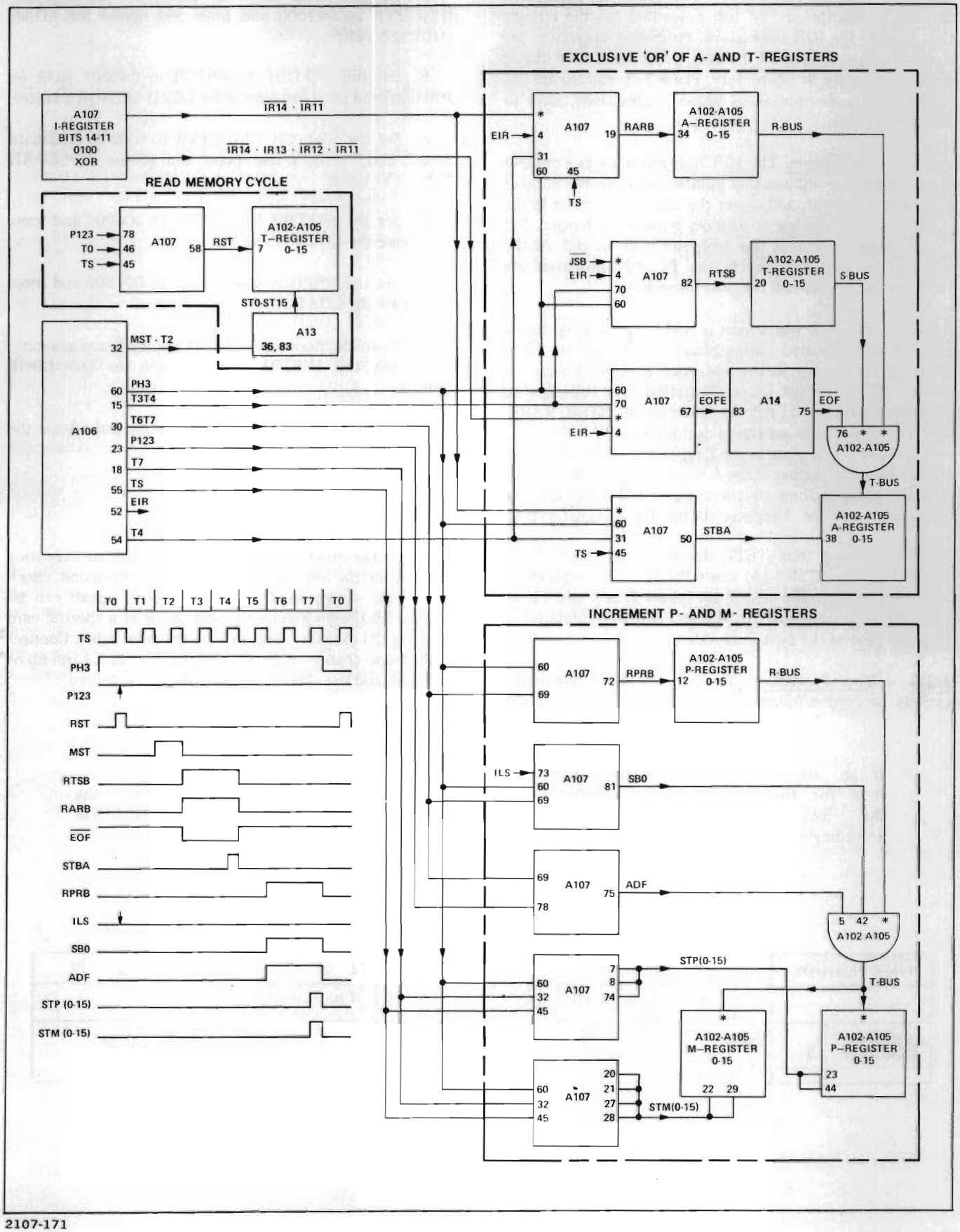
4-206. The computer is now in the run mode executing the XOR instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-48. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-12. XOR Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
EXECUTE	3	Clear TR			EOF A, TR to A			P + 1 to P, M Set next phase	



2107-171

Figure 4-48. XOR Instruction Processing Circuits, Servicing Diagram

4-207. IOR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the IOR instruction. Processing operations are summarized in table 4-13. Point-to-point signal flow during phase 3 is shown in figure 4-49. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-208. Description. The IOR instruction reads a number from memory, combines that number with another number from the A-register, and stores the resulting number in the A-register. The number in memory remains unchanged, but the previous number in the A-register is destroyed. At the end of the processing cycle the P- and M-registers are incremented by one and the next phase is set.

4-209. The IOR instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 0110 (bits 14 thru 11 respectively) in the I-register causes signals RTSB, RARB, IOF, and STBA to be generated during time T3T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), and the number in the A-register to the R-bus (signal RARB), combine these numbers (signal $\overline{\text{IOF}}$), and read the result back into the A-register via the T-bus (signal STBA).

4-210. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-211. Test Procedure. To test the IOR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 033001 (IOR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the RUN switch.

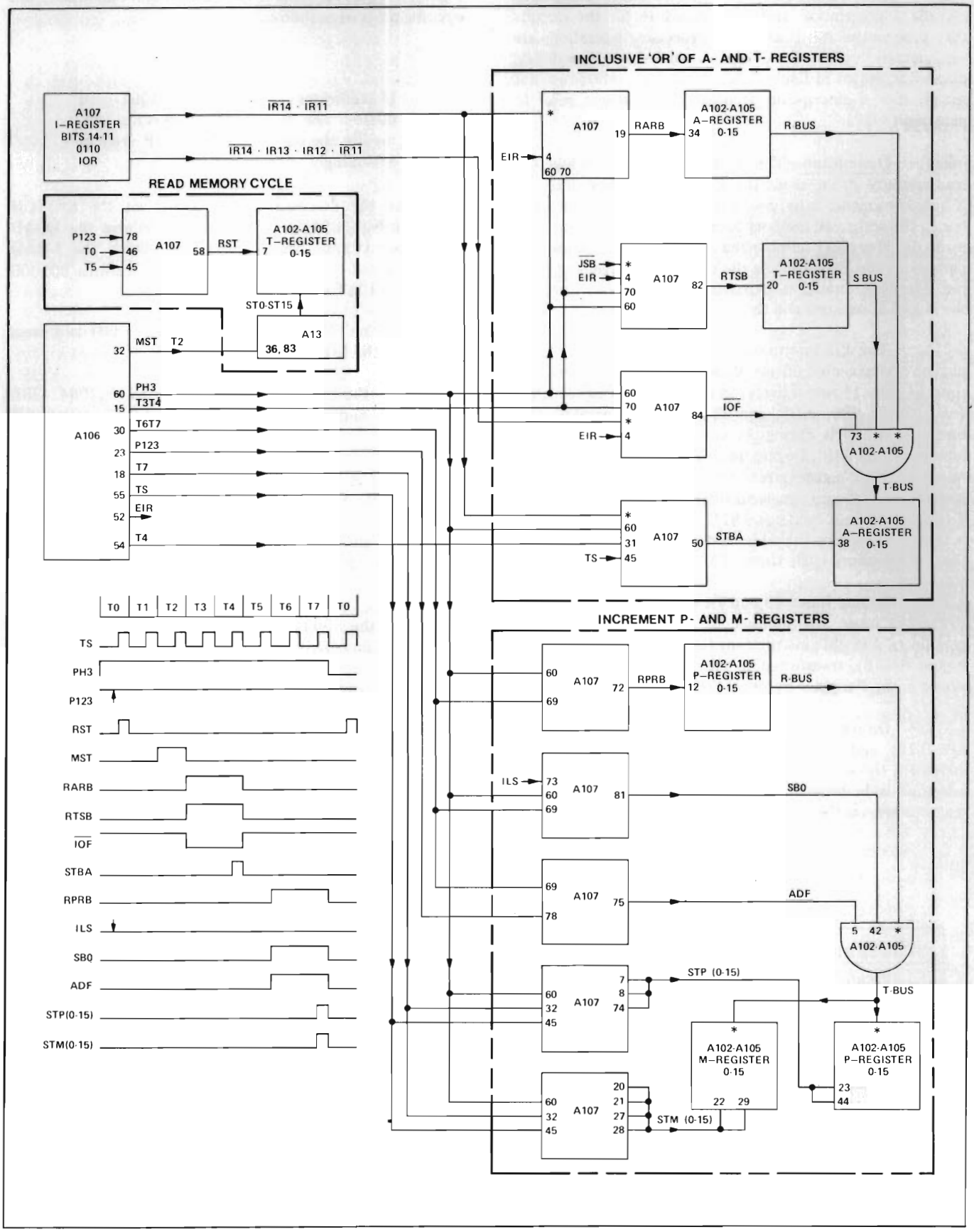
4-212. The computer is now in the run mode executing the IOR instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-49. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-13. IOR Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
			READ (Mem to TR)			WRITE (TR to Mem)			
EXECUTE	3	Clear TR			IOF A, TR to A			P + 1 to P, M Set next phase	



2107-172

Figure 4-49. IOR Instruction Processing Circuits, Servicing Diagram

4-213. JSB INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the JSB instruction. Processing operations are summarized in table 4-14. Point-to-point signal flow during phase 3 is shown in figure 4-50. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-214. Description. The JSB instruction inhibits the read-memory cycle, reads the P-register number onto the R-bus, increments it by one, and stores the resulting number in the addressed memory location. The instruction then reads the M-register number onto the S-bus, and stores this number in the P-register. At the end of the processing cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-215. The JSB instruction is read from memory during phase 1 and executed during phase 3. Bit configuration 0011 (bits 14 thru 11 respectively) in the I-register causes signals JSB, RPRB, SB0, ADF, and STBT to be generated. The read-memory cycle during phase 3 of this instruction is inhibited (signal JSB). During times T1 and T2 of phase 3 the number in the P-register is read onto the R-bus (signal RPRB), incremented by one (signals SB0 and ADF), and stored in the T-register via the T-bus (signal STBT). The T-register number is then written into the addressed memory location during the write-memory cycle (times T3 thru T5).

4-216. During times T3 and T4 signals RMSB, $\overline{\text{EOF}}$, and STP(0-15) cause the number in the M-register (address portion of the JSB instruction) to be read onto the S-bus (signal RMSB), transferred to the T-bus (signal $\overline{\text{EOF}}$), and stored in the P-register by signal STP(0-15).

4-217. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-218. Test Procedure. To test the JSB instruction circuits, proceed as follows:

Note

If addresses other than 001001 and 001005 are used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch. Then, press and release the LOAD MEMORY switch ten times (This sets locations 001000 through 001012 to 001000).

b. Set the SWITCH REGISTER to 001001 and press and release the LOAD ADDRESS switch.

c. Set the SWITCH REGISTER to 017004 (JSB instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001005 and press and release the LOAD ADDRESS switch.

e. Set the SWITCH REGISTER to 017000 (JSB instruction) and press and release the LOAD MEMORY switch.

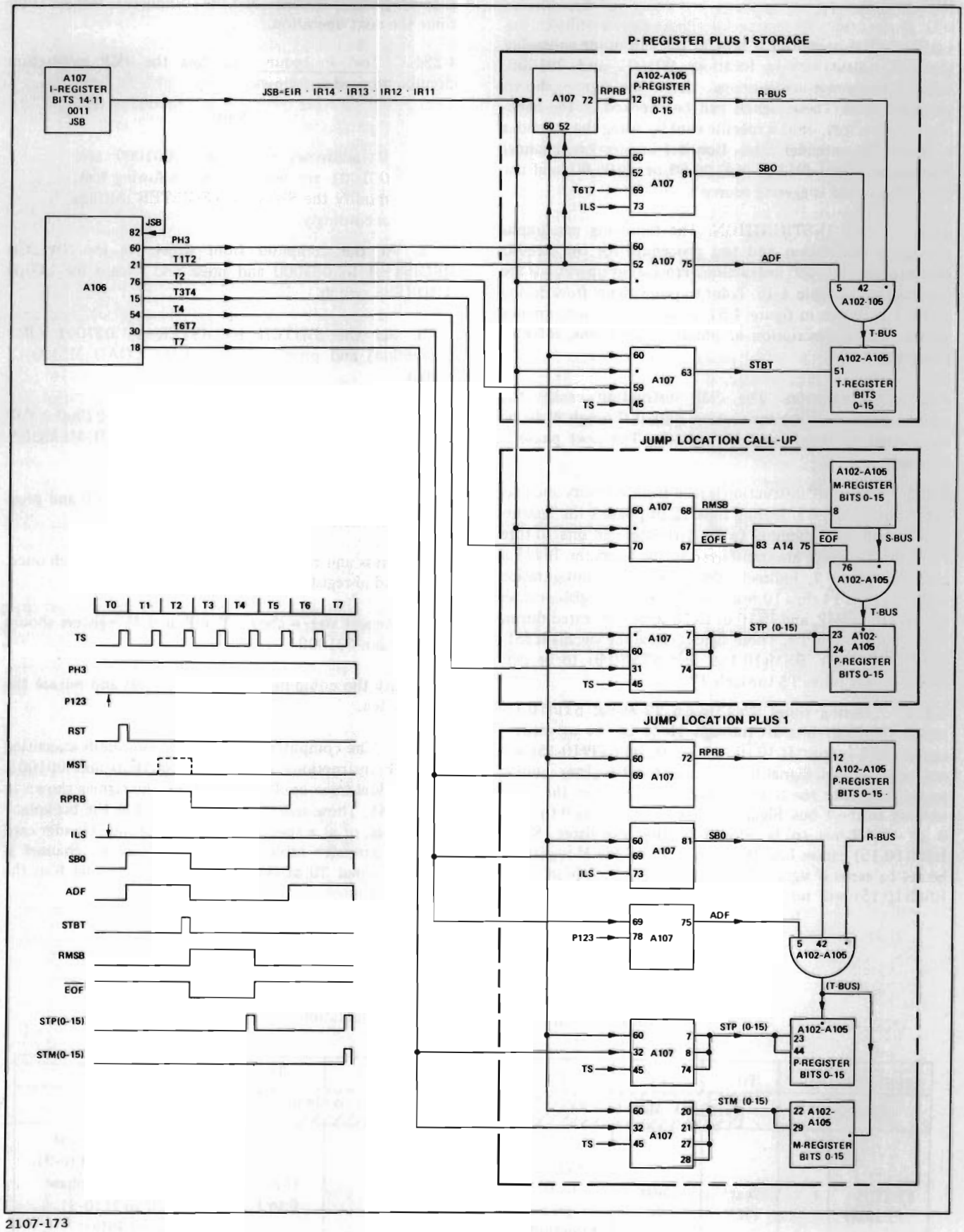
f. Set the SWITCH REGISTER to 001001 and press and release the LOAD ADDRESS switch.

g. Press and release the SINGLE CYCLE switch twice. Location 001004 should contain 001002, and the P- and M-registers should contain 001005.

h. Repeat step g above. Location 001000 should contain 001006, and the P- and M-registers should contain 001001.

Table 4-14. JSB Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
EXECUTE	3	Clear TR Inhibit Mem. Data	P + 1 to TR		M to P			P + 1 to P, M Set next phase	



2107-173

Figure 4-50. JSB Instruction Processing Circuits, Servicing Diagram

i. At the computer front panel, press and release the RUN switch.

4-219. The computer is now in the run mode executing the JSB instructions in locations 001001 and 001005. Using a dual-trace oscilloscope, check the signals shown in figure 4-50. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

4-220. JMP INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the JMP instruction. Processing operations are summarized in table 4-15. Point-to-point signal flow during phase 1 is shown in figure 4-51. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-221. Description. The JMP instruction causes the address portion of the instruction (bits 0 through 9) to be transferred to the P- and M- registers. The next phase is then set.

4-222. The JMP instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction is read from memory to the T-register and bits 10 thru 15 of the T-register are transferred to the I-register. Bit 15 is used for phase 2, indirect addressing.) Bit configuration 0101 0/1 (bits 14 thru 10 respectively) in the I-register causes signals $\overline{OPO}$, JMP, and $\overline{IR10}$ or IR10 to be generated during times T0 through T3. These signals cause the signals RTSB, ADF, STP(0-15), RSM(10-15), and STM(0-9) to be generated during times T5 through T7.

4-223. During times T5 through T7 signal STP(10-15) causes P-register bits 10 through 15 to be set to zeros if signal $\overline{IR10}$ is true. If $\overline{IR10}$ is false, signal STP(10-15) will not be generated. Signal RTSB causes the T-register number to be read onto the S-bus. Signal ADF transfers the S-bus number to the T-bus. Signal STM(0-9) causes bits 0 through 9 of the T-bus to be stored in the M-register. Signal RSM(10-15) causes bits 10 through 15 of the M-register to be set to zeros if signal $\overline{IR10}$ is true. If $\overline{IR10}$ is false, signal RSM(10-15) will not be generated. The next phase (phase 1, phase 2 if bit 15 is a logic "1", or phase 4 if an interrupt is in progress) is then set, and the computer is ready to continue the next operation.

4-224. Test Procedure. To test the JMP instruction circuits, proceed as follows:

Note

If addresses other than 001000 and 001001 are used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 027001 (JMP instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Press and release the SINGLE CYCLE switch once. The P- and M-registers should contain 001001.

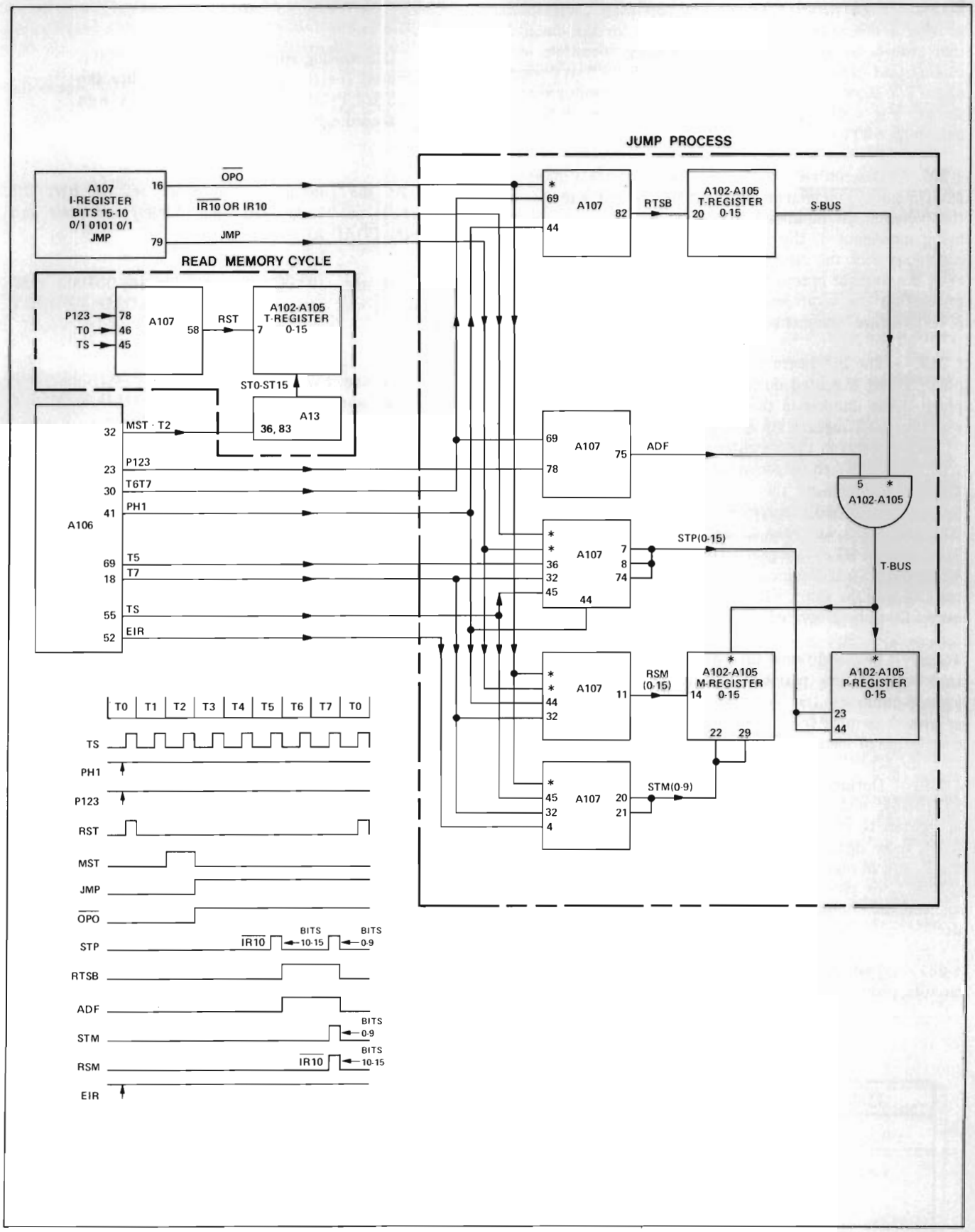
f. Repeat step e above. The P- and M-registers should now contain 001000.

g. At the computer front panel, press and release the RUN switch.

4-225. The computer is now in the run mode executing the JMP instructions in locations 001000 and 001001. Using a dual-trace oscilloscope, check the signals shown in figure 4-51. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Table 4-15. JMP Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH (JMP)	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)			If Z: 0 to P	If Z: 0 to M (10-15) If D: TR to P, M (0-9) and set next phase If I: TR to M (0-9) and set PH2	



2107-174

Figure 4-51. JMP Instruction Processing Circuits, Servicing Diagram

4-226. ISZ INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ISZ instruction. Processing operations are summarized in table 4-16. Point-to-point signal flow during phase 3 is shown in figure 4-52. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-227. Description. The ISZ instruction reads a number from memory, increments the number by one, and stores the incremented number in its original location. If, after being incremented, the number is not zero, the program continues with the next instruction in sequence. If, however, the number is zero after being incremented, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one).

4-228. The ISZ instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 0111 (bits 14 thru 11 respectively) in the I-register causes signals RTSB, RB0, ADF, and STBT to be generated during times T3 thru T5. These signals transfer the number in the T-register to the S-bus (signal RTSB), increment the number by one (signals RB0 and ADF), and read it back into the T-register via the T-bus (signal STBT). Signal C16 is generated during times T3 through T5 if the incremented number equals zero. Signal C16 sets the Carry FF (CFF) at time T4TS. Signal CFF causes C0 to be generated at time T6T7.

4-229. Two additional time periods (0.4 μsec) are generated between time periods T5 and T6 to allow the incremented number in the T-register to be written back into the addressed memory location. Refer to paragraph 4-160 for a description of memory timing for the ISZ instruction.

4-230. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-231. Test Procedure. To test the ISZ instruction circuits, proceed as follows:

Note

If a starting address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 (starting address) and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 037003 (ISZ instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch twice.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD MEMORY switch. (This initializes the number in the memory location addressed by the ISZ instruction.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. At the computer front panel, press and release the RUN switch.

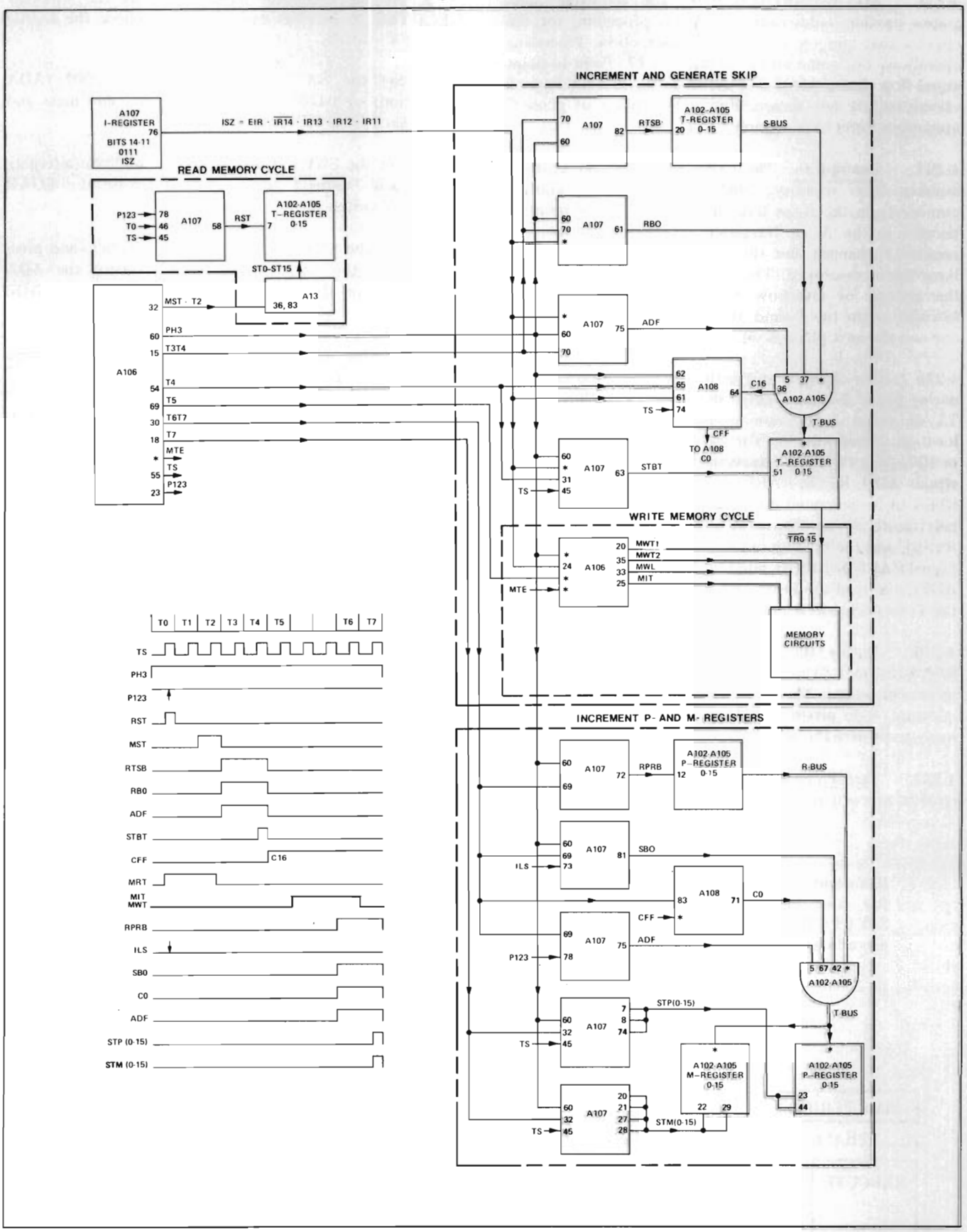
4-232. The computer is now in the run mode executing the ISZ instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-52. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-16. ISZ Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	A	B	T6	T7
PHASE		READ (Mem to TR)						WRITE (TR to Mem)			
EXECUTE	3	Clear TR			TR + 1 to TR If C16: Set Carry Inhibit Write			Machine Cycle Expanded 400 nsec.		P + 1 + Carry to P, M Set next phase	



2107-175

Figure 4-52. ISZ Instruction Processing Circuits, Servicing Diagram

4-233. ADA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ADA/B instruction. Processing operations are summarized in table 4-17. Point-to-point signal flow during phase 3 is shown in figure 4-53. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-234. Description. The ADA/B instruction reads a number from memory, adds that number to another number from the A- or B-register, and stores the resulting number in the A- or B-register. The number in memory remains unchanged, but the previous number in the A- or B-register is destroyed. The result of the addition may set the Extend or Overflow registers. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-235. The ADA/B instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 1000 or 1001 (bits 14 thru 11 respectively) in the I-register causes signals ADD, RTSB, RARB or RBRB, ADF, and STBA or STBB to be generated during times T3 thru T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), and the number in the A- or B-register to the R-bus (signal RARB or RBRB), add these numbers together (signal ADF), and read the result back into the A- or B-register via the T-bus (signal STBA or STBB).

4-236. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-237. Test Procedure. To test the ADA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 043001 (ADA instruction) or 047001 (ADB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 052525 and press and release the LOAD A switch, if testing the ADA instruction, or the LOAD B switch if testing the ADB instruction.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch twice. The A-register should now contain 125252.

h. At the computer front panel, press and release the RUN switch.

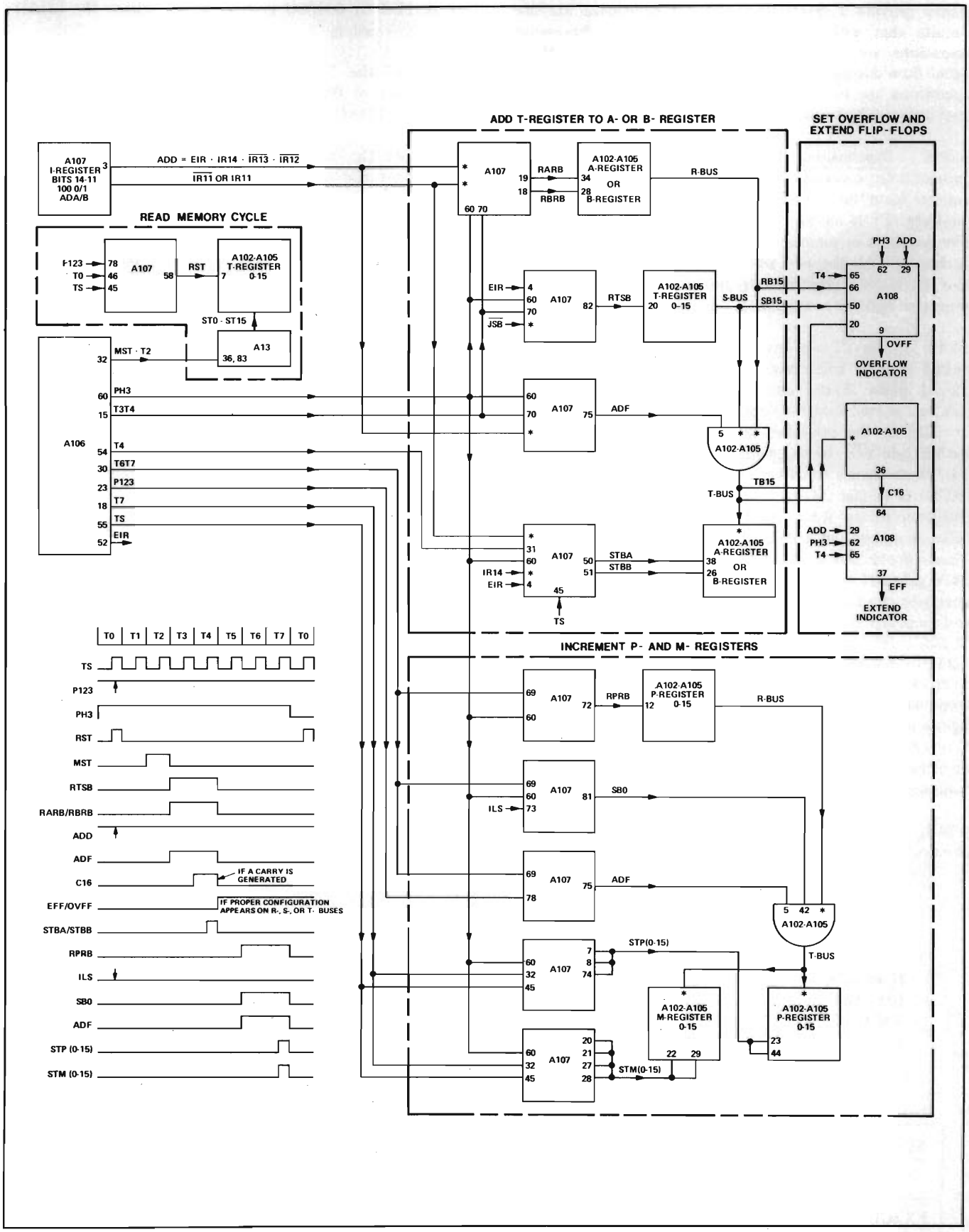
4-238. The computer is now in the run mode executing the ADA or ADB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-53. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-17. ADA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
EXECUTE	3	Clear TR			If A: ADF A, TR to A IF B: ADF B, TR to B If C16: Set E			P + 1 to P, M Set next phase	



2107-176

Figure 4-53. ADA/B Instruction Processing Circuits, Servicing Diagram

4-239. CPA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CPA/B instruction. Processing operations are summarized in table 4-18. Point-to-point signal flow during phase 3 is shown in figure 4-54. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-240. Description. The CPA/B instruction reads a number from memory, compares that number with another number from the A- or B-register. If the compare is unequal the Carry FF is set which causes signal C0 to be generated. The numbers in memory and the A- or B-register remain unchanged. At the end of the machine cycle the P- and M-registers are incremented by one or by two if signal C0 is generated and the next phase is set.

4-241. The CPA/B instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 1010 or 1011 in the I-register causes signals RTSB, RARB or RBRB, and $\overline{EOF}$ to be generated during times T3 through T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), transfer the number in the A- or B-register to the R-bus (signal RARB or RBRB), combine these numbers and transfer the resultant number to the T-bus (signal $\overline{EOF}$), and check the T-bus for zero via the TAN gates. If the T-bus is not zero (S-bus and R-bus are unequal), the Carry FF will be set at the end of time T4TS and cause signal C0 to be generated during time T6T7.

4-242. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-243. Test Procedure. To test the CPA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 053003 (CPA instruction) or 057003 (CPB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the CPA instruction, or the LOAD B switch if testing the CPB instruction.

e. Set the SWITCH REGISTER to 001003 and press and release the LOAD ADDRESS switch.

f. Set the SWITCH REGISTER to 077777 (for unequal compare) or to 000000 (for equal compare) and press and release the LOAD MEMORY switch.

g. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

h. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

i. At the computer front panel, press and release the SINGLE CYCLE switch twice. The P- and M-registers should increment by one and contain 01001 if using an unequal compare, or 01000 if using an equal compare.

j. At the computer front panel, press and release the RUN switch.

2-244. The computer is now in the run mode executing the CPA or CPB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-54. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-18. CPA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
EXECUTE	3	Clear TR			If A: EOF A, TR to T Bus If B: EOF B, TR to T Bus If T Bus not zero, set Carry			P + 1 + Carry to P, M Set next phase	

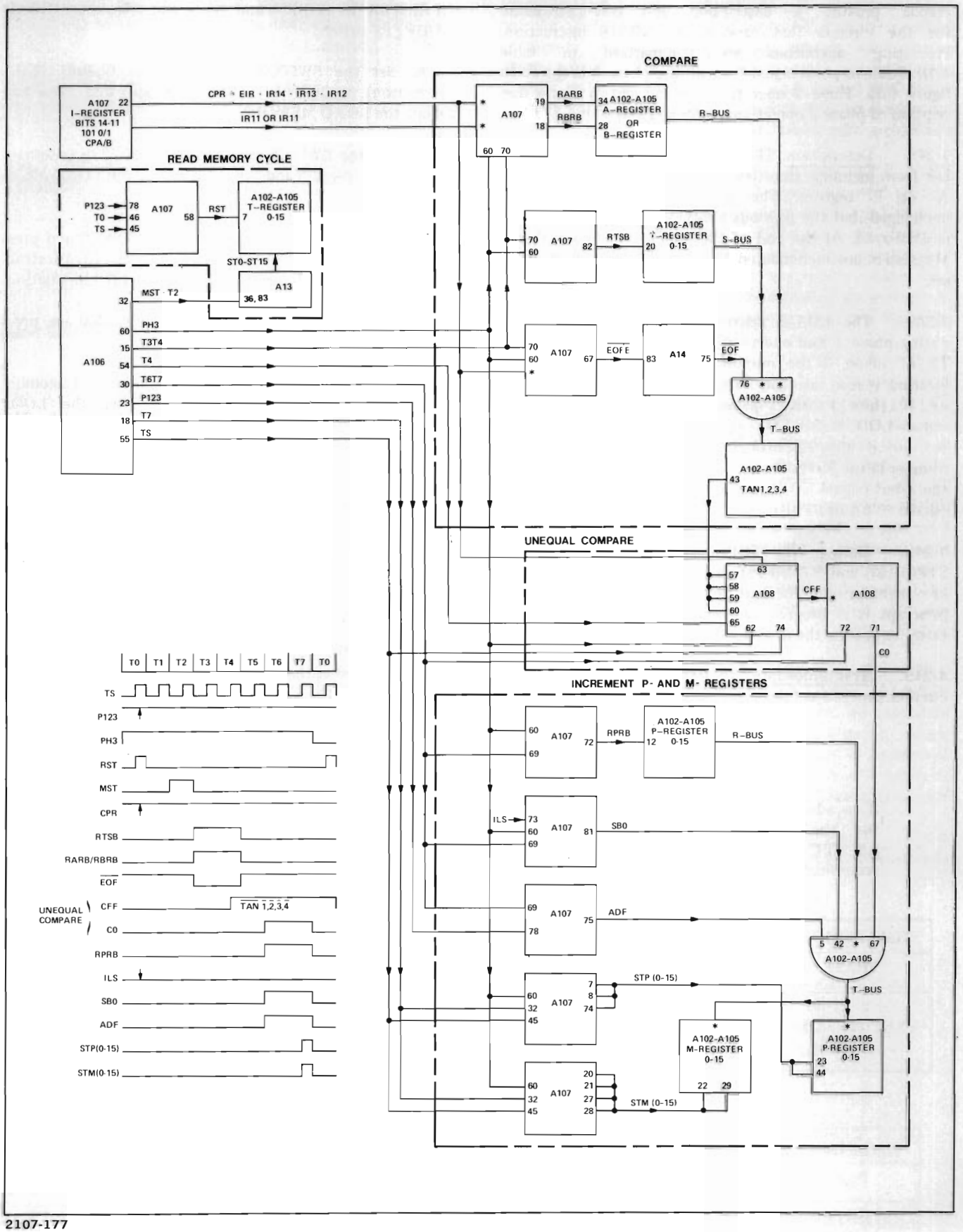


Figure 4-54. CPA/B Instruction Processing Circuits, Servicing Diagram

4-245. LDA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the LDA/B instruction. Processing operations are summarized in table 4-19. Point-to-point signal flow during phase 3 is shown in figure 4-55. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-246. Description. The LDA/B instruction reads a number from memory, transfers and stores that number in the A- or B- register. The number in memory remains unchanged, but the previous number in the A- or B-register is destroyed. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-247. The LDA/B instruction is read from memory during phase 1 and executed during phase 3. During time T2 of phase 3 the number in the addressed memory location is read into the T-register. Bit configuration 1100 or 1101 (bits 14 thru 11 respectively) in the I-register causes signals LOD, RTSB, $\overline{EOF}$, and STBA or STBB to be generated during times T3 through T4. These signals transfer the number in the T-register to the S-bus (signal RTSB), then to the T-bus (signal $\overline{EOF}$), and store it in the A- or B-register (signal STBA or STBB).

4-248. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-249. Test Procedure. To test the LDA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 063001 (LDA instruction) or 067001 (LDB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the LDA instruction, or the LOAD B switch if testing the LDB instruction.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch twice. The A-register should now contain 052525.

h. At the computer front panel, press and release the RUN switch.

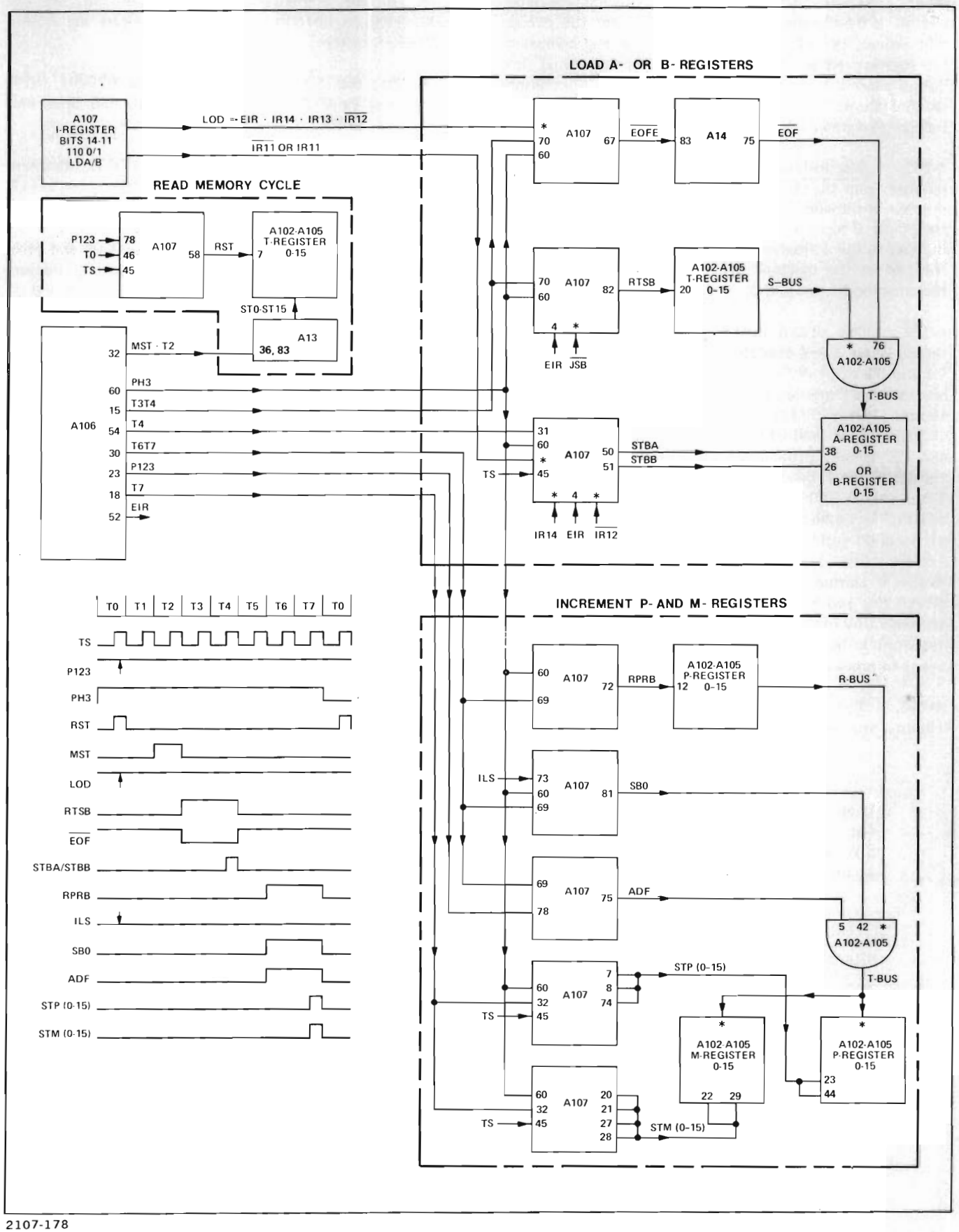
4-250. The computer is now in the run mode executing the LDA or LDB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-55. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-19. LDA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
EXECUTE	3	Clear TR			If A: TR to A If B:TR to B			P + 1 to P, M Set next phase	



2107-178

Figure 4-55. LDA/B Instruction Processing Circuits, Servicing Diagram

4-251. STA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the STA/B instruction. Processing operations are summarized in table 4-20. Point-to-point signal flow during phase 3 is shown in figure 4-56. Phase 2 operations are not shown. For a description of phase 2 operations, refer to paragraph 4-171.

4-252. Description. The STA/B instruction reads a number from the A- or B-register, and stores the resulting number in the addressed memory location. The number in the A- or B-register remains unchanged, but the previous number in the addressed memory location is destroyed. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-253. The STA/B instruction is read from memory during phase 1 and executed during phase 3. During times T1 and T2 of phase 3 the number in the A- or B-register is read into the T-register. Bit configuration 1110 or 1111 (bits 14 thru 11 respectively) in the I-register causes signals RARB or RBRB, $\overline{EOF}$, and STBT to be generated during times T1 and T2. These signals transfer the number in the A- or B-register to the R-bus (signal RARB or RBRB), then to the T-bus (signal $\overline{EOF}$), and store it in the T-register (signal STBT). The number is then written into the addressed memory location during the write-memory cycle.

4-254. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-255. Test Procedure. To test the STA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 073001 (STA instruction) or 077001 (STB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the STA instruction, or the LOAD B switch if testing the STB instruction.

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch twice. Location 001001 should now contain 000000.

h. At the computer front panel, press and release the RUN switch.

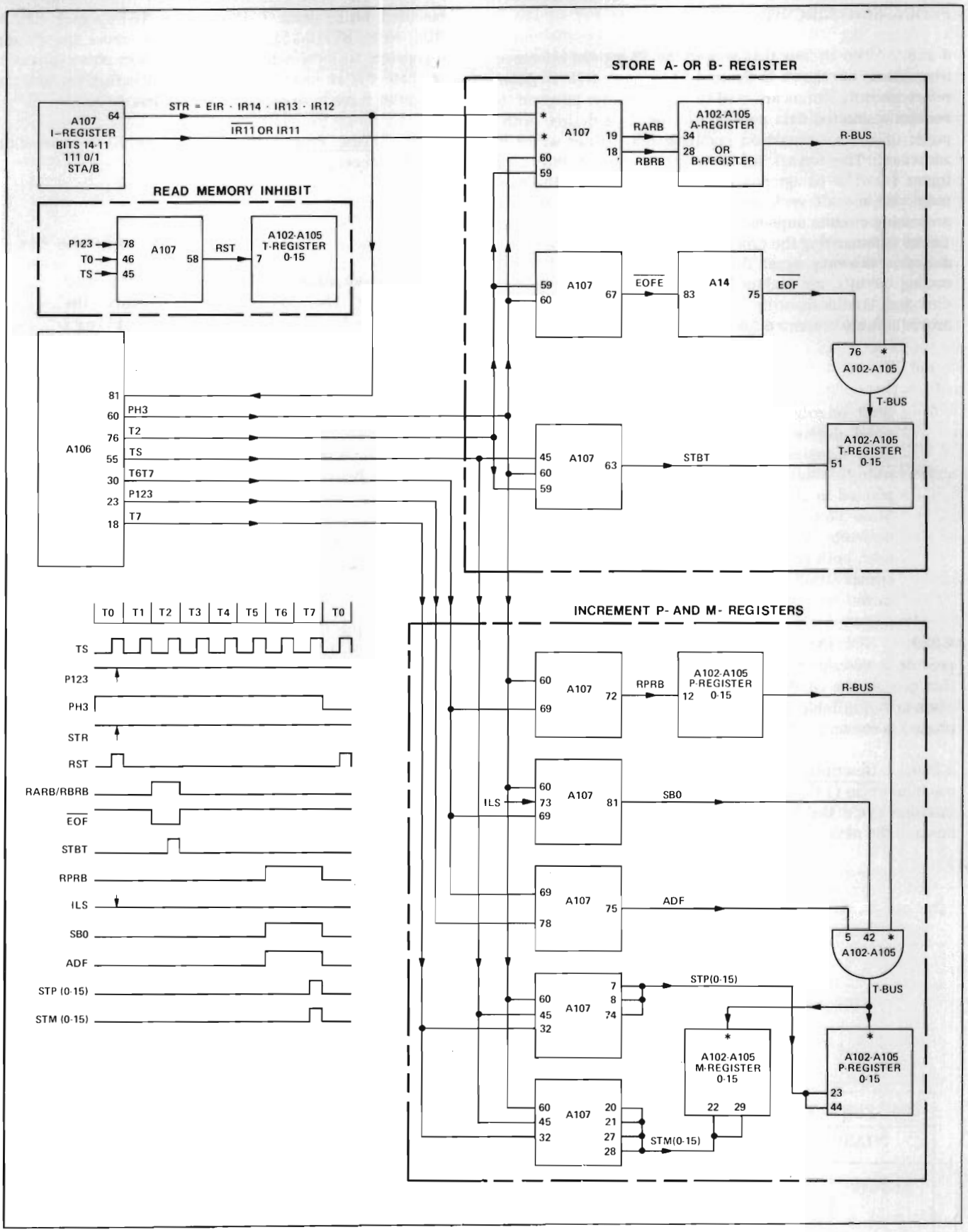
4-256. The computer is now in the run mode executing the STA or STB instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-56. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal PH3 at XA106-60 or A106-60, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-20. STA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
EXECUTE	3	Clear TR Inhibit Mem. Data	If A: A to TR If B: B to TR					P + 1 to P, M Set next phase	



2107-179

Figure 4-56. STA/B Instruction Processing Circuits, Servicing Diagram

4-257. REGISTER REFERENCE INSTRUCTION PROCESSING CIRCUITS.

4-258. The circuits that process the 39 register reference instructions are shown in figure 4-57 through 4-78. Register reference instructions are used in the computer program to address a selected data register and specify a desired arithmetic or control operation involving the register which is addressed. The format for these instructions is shown in figure 4-1. The paragraphs which follow describe the purpose and use of each instruction and explain how the processing circuits implement and execute the instructions. Tables summarizing the processing operations, and servicing diagrams showing signal flow and timing within the processing circuits, are included for reference during explanation and troubleshooting. Suggested troubleshooting test procedures are presented for each instruction.

Note

Shift or rotate instructions can be processed during times T3 and T5 of the same machine cycle. Only time T3 processing is illustrated in the figures and explained in the text of these instructions. Time T5 processing uses identical signals between the various circuit cards. However, both processes should be checked as circuit structure varies within the circuit cards.

4-259. NOP INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the NOP instruction. Processing operations are summarized in table 4-21. Point-to-point signal flow during phase 1 is shown in figure 4-57.

4-260. Description. The NOP instruction provides a one machine cycle (1.6 μsec) program delay. At the end of the machine cycle the P- and M-registers are incremented by one and the next phase is set.

4-261. The NOP instruction is read from memory and executed during phase 1. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-262. Test Procedure. To test the NOP instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 000000 and press and release the LOAD A switch and LOAD B switch.

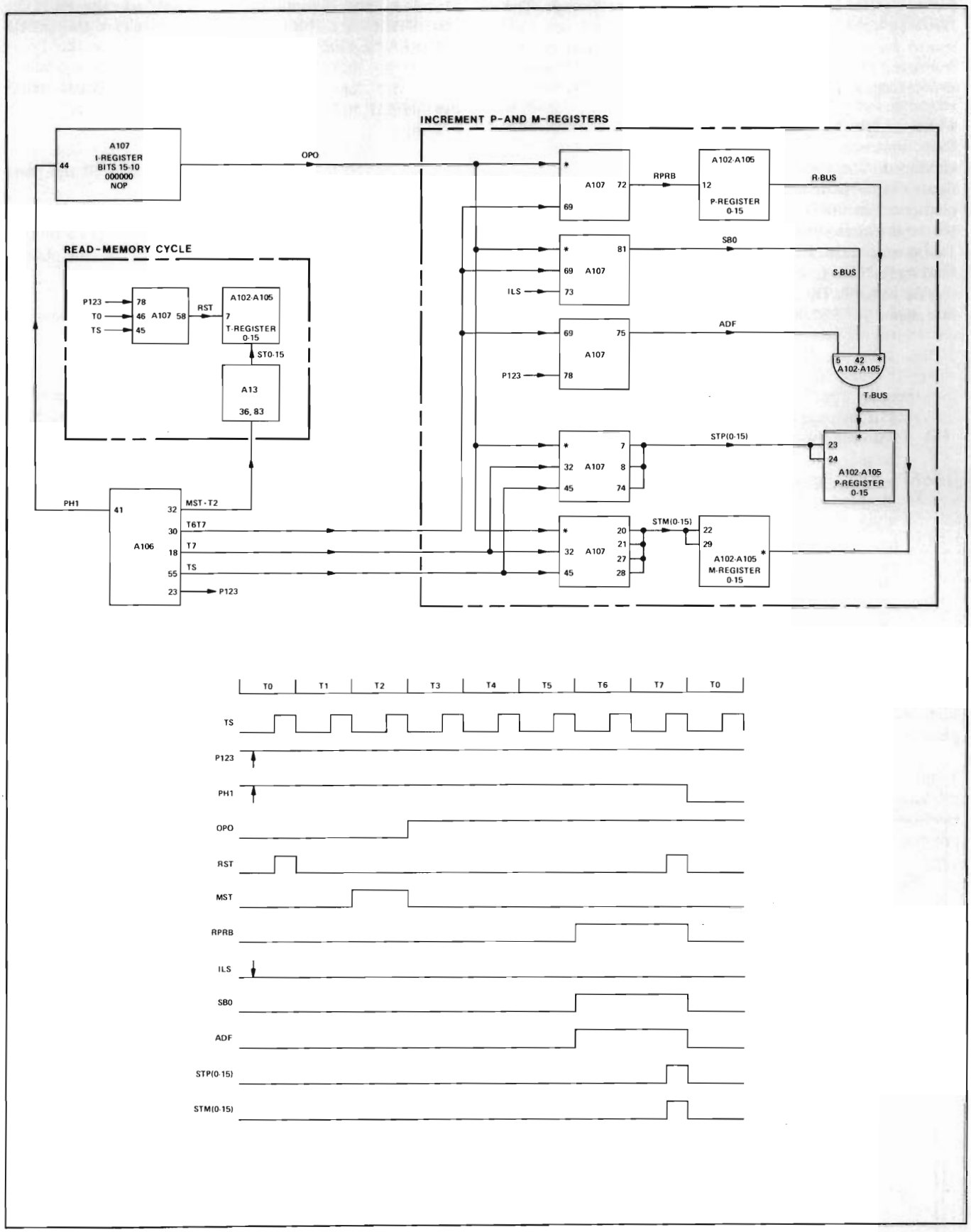
b. Open the door assembly. At display board assembly A501, set the MEMORY switch to the OFF position.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

4-263. The computer is now in the run mode executing the NOP instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-46. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Table 4-21. NOP Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR (Set Functions)				TR to M (0-9) If Z: 0 to M (10-15) Set next phase	



2107-180

Figure 4-57. NOP Instruction Processing Circuits, Servicing Diagram

4-264. CLE INSTRUCTION (Shift-Rotate Group). The following paragraphs provide a description and test procedure for the circuits that process the CLE instruction. Processing operations are summarized in table 4-22. Point-to-point signal flow during phase 1 is shown in figure 4-58.

4-265. Description. The CLE instruction resets the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 in the instruction code is read into the I-register. Bit configuration 000000 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPO, and RARB to be generated during times T3 and T4. These signals in combination with signal TR5 from the T-register cause the E-register to reset at time T4TS. The A-register data is read onto the R-bus (signal RARB) during times T3 thru T5 but is not used.

4-266. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-267. Test Procedure. To test the CLE instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 000040 (CLE instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

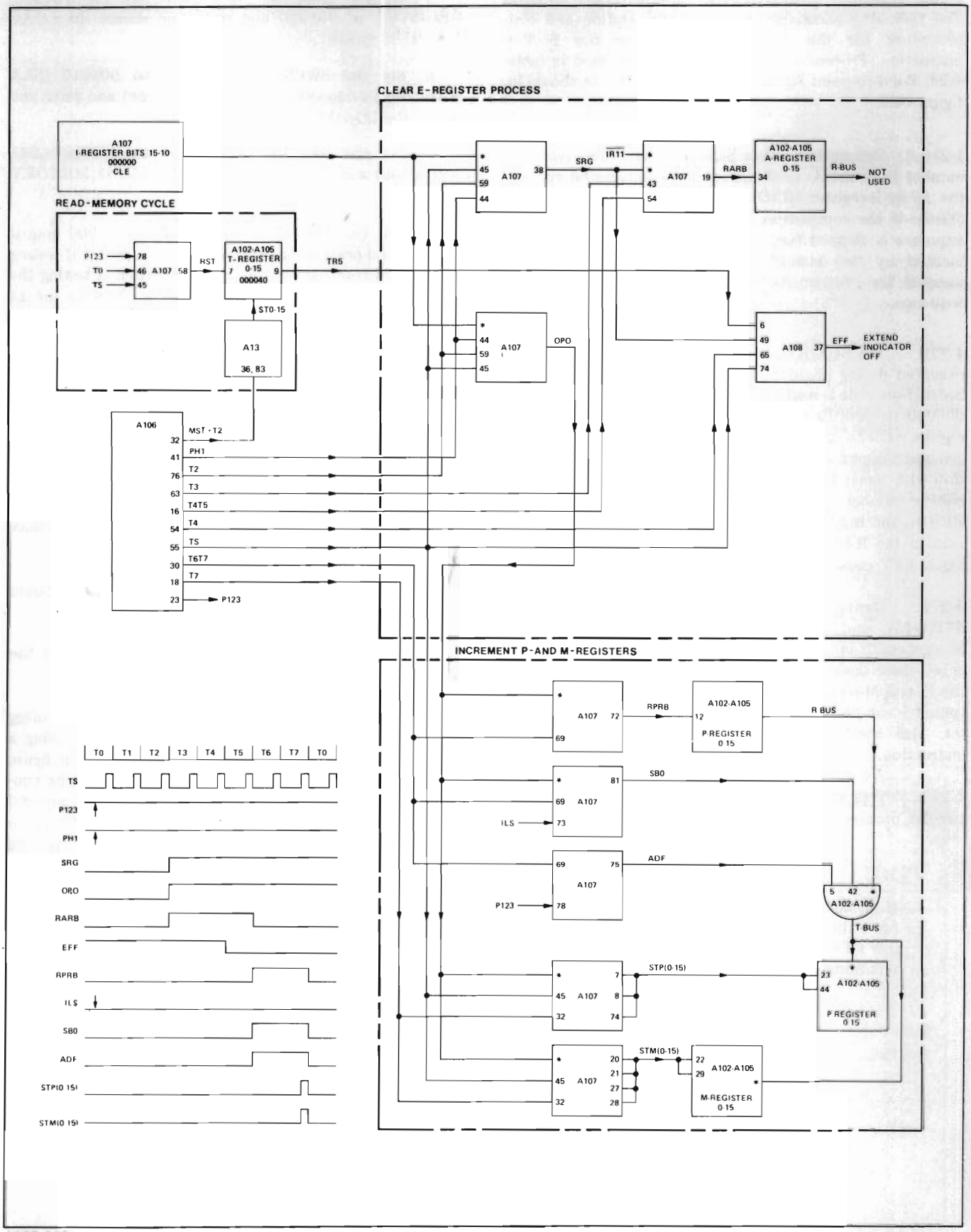
4-268. The computer is now in the run mode executing the CLE instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-58. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-22. CLE Instruction (Shift Rotate Group) Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B Reset E Flip-flop	T4 Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	T5 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		



2107-181

Figure 4-58. CLE Instruction (Shift-Rotate Group) Processing Circuits, Servicing Diagram

4-269. SLA/B INSTRUCTION (Shift-Rotate Group). The following paragraphs provide a description and test procedure for the circuits that process the SLA/B instruction. Processing operations are summarized in table 4-23. Point-to-point signal flow during phase 1 is shown in figure 4-59.

4-270. Description. The SLA/B instruction reads a number from the A- or B-register and compares bit zero of the A- or B-register (RBO) with bit zero of the T-register (TR0). If the comparison is equal, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If the comparison is unequal, the program continues with the next instruction is sequence.

4-271. The SLA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000000 or 000010 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during times T3 and T4. These signals in combination with signal TR3 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), and the Carry FF (CFF) to set at time T4TS if bit zero of the R-bus and bit zero of the T-register are equal. Signal CFF causes signal C0 to be generated at time T6T7.

4-272. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-273. Test Procedure. To test the SLA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001010 (SLA instruction) or to 004010 (SLB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (equal compare and press and release the LOAD A switch if testing the SLA instruction, or the LOAD B switch if testing the SLB instruction.) (Substitute 000001 to 000000 for an unequal compare.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

4-274. The computer is now in the run mode executing the SLA or SLB instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-59. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

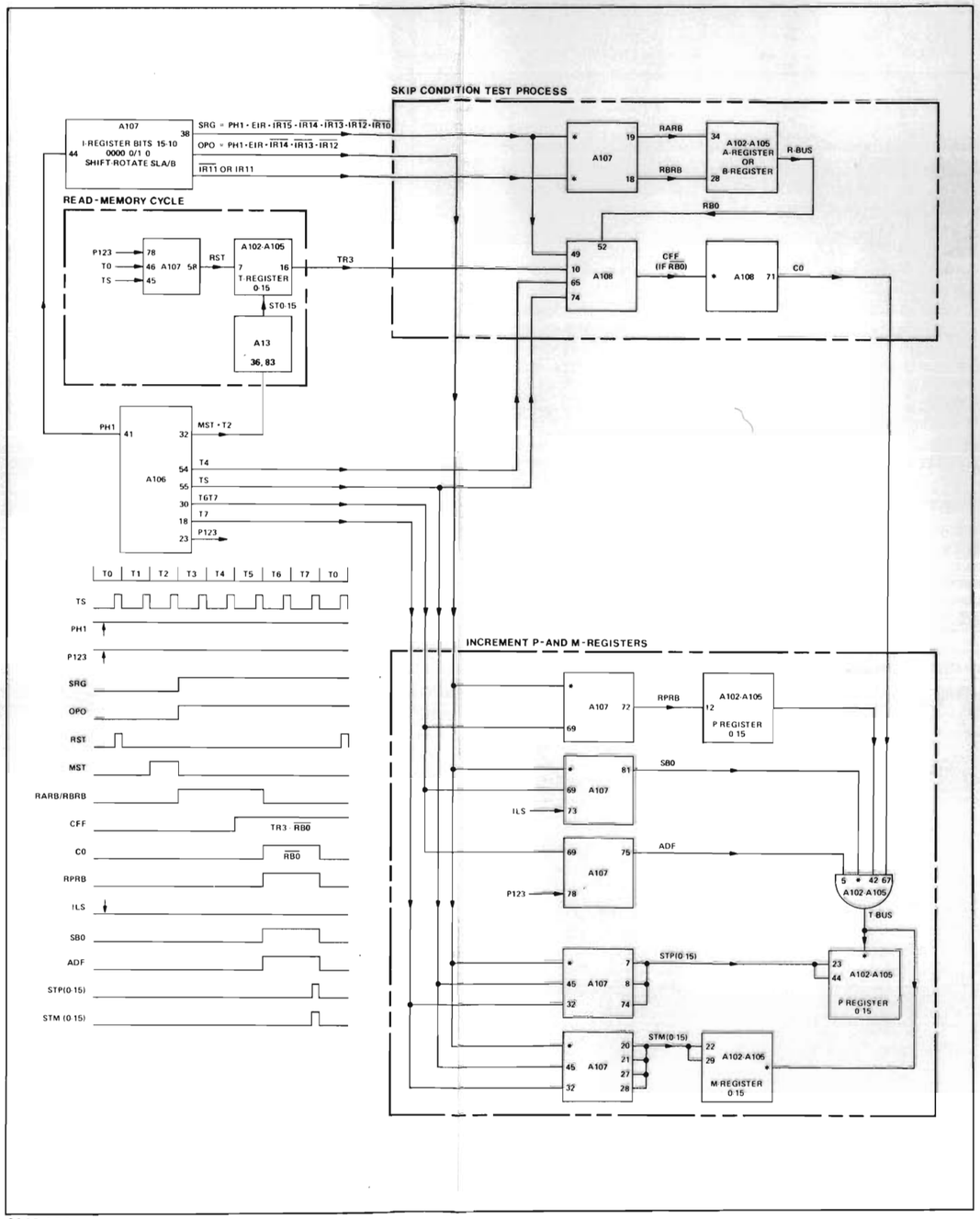
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-23. SLA/B Instruction (Shift Rotate Group) Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	*Execute			P + 1 + Carry to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	T4 Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry Read A/B to R Bus Set Carry if RB0 = 0 and TR0 = 0, or RB0 = 1 and TR0 = 1		T5 All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	

*Combination of SSA/B, SLA/B, and RSS is a special case; see paragraph 4-384.



2107-182

Figure 4-59. SLA/B Instruction (Shift-Rotate Group) Processing Circuits, Servicing Diagram

4-275. A/BLS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the A/BLS instruction. Processing operations are summarized in table 4-24. Point-to-point signal flow during phase 1 is shown in figure 4-60.

4-276. Description. The A/BLS instruction reads a number from the A- or B-register and moves all bits of that number except bit 15 one position to the left. Bit 14 is discarded; replaced by bit 13. Bit 15 remains unchanged (refer to table 4-27). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-277. The A/BLS instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 or 0010 in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, TR7, TR8, and TR9 from the T-register cause the signals SLM, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left (signal SLM), and the number stored back into the A- or B- register (signal STBA or STBB).

4-278. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-279. Test Procedure. To test the A/BLS instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Press and release the LOAD MEMORY switch (ALS instruction), or set the SWITCH REGISTER to 005000 (BLS instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ALS instruction, or the LOAD B switch if testing the BLS instruction. (To check bit 15, set the SWITCH REGISTER to 152525.)

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 025252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052524 in it.

h. At the computer front panel, press and release the RUN switch.

4-280. The computer is now in the run mode executing the ALS or BLS instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-60. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

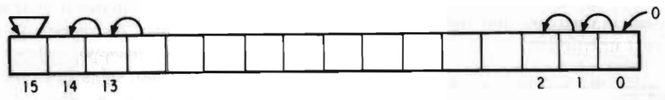
Note

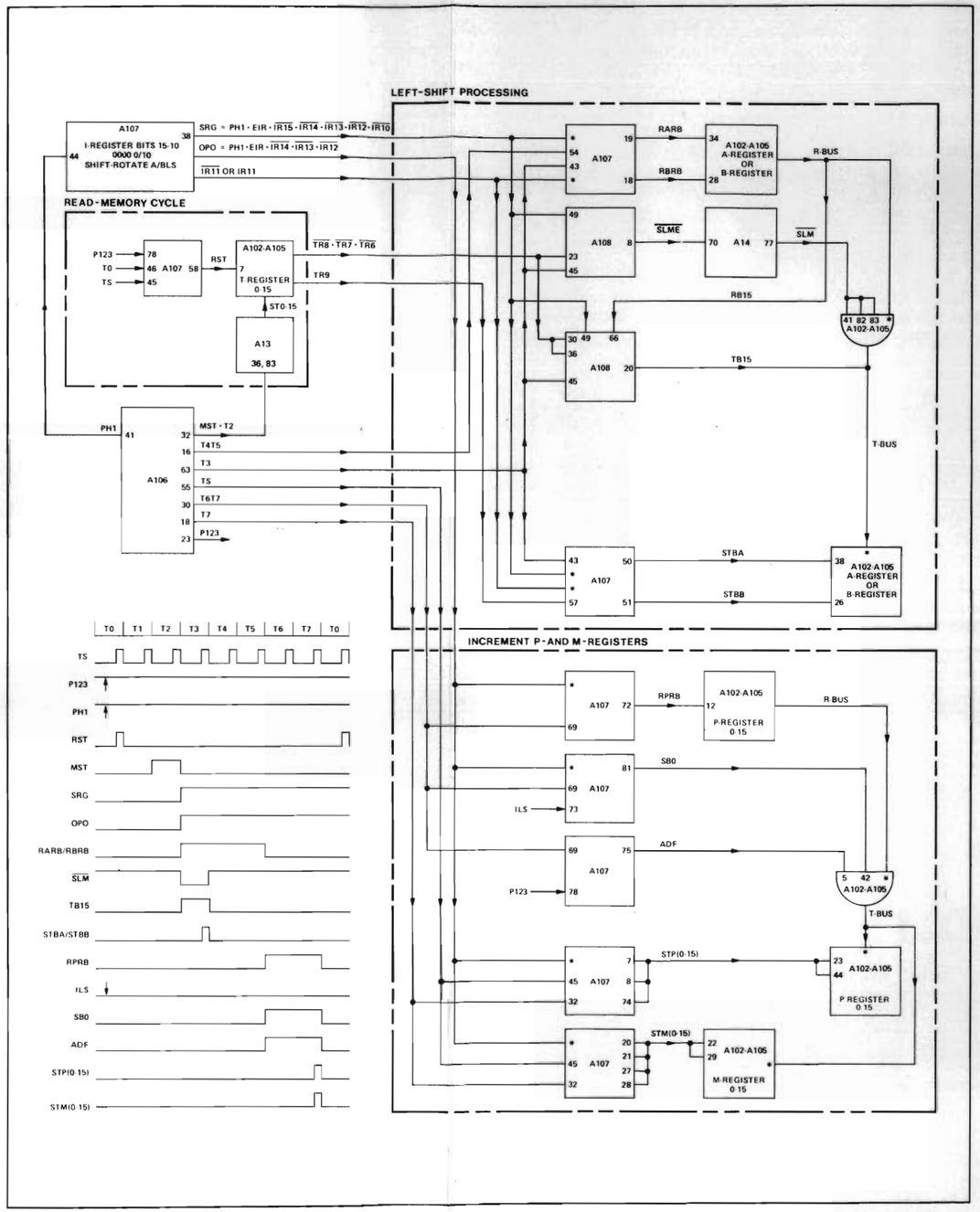
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-24. A/BLS Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus SLM Shift R Bus to T Bus Store T Bus in A or B				

Note: Data movement is as follows:





2107-183

Figure 4-60. A/BLS Instruction Processing Circuits, Servicing Diagram

4-281. A/BRS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits used by the A/BRS instruction. Processing operations are summarized in table 4-25. Point-to-point signal flow during phase 1 is shown in figure 4-61.

4-282. Description. The A/BRS instruction reads a number from the A- or B-register and moves all bits of that number one position to the right. Bit zero is discarded; replaced by bit one. Bit 15 remains unchanged (table 4-28). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-283. The A/BRS instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000000 or 000010 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, $\overline{TR7}$, $\overline{TR8}$, and TR9 from the T-register cause the signals $\overline{SRM}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the right (signal $\overline{SRM}$), and the number stored back into the A- or B-register (signal STBA or STBB).

4-284. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-285. Test Procedure. To test the A/BRS instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001100 (ARS instruction) or 005100 (BRS instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ARS instruction, or LOAD B switch if testing the BRS instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 025252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 012525 in it.

h. At the computer front panel, press and release the RUN switch.

4-286. The computer is now in the run mode executing the ARS or BRS instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-61. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

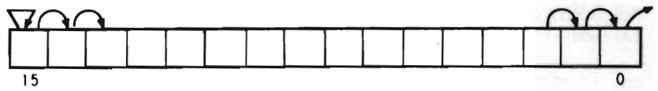
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-25. A/BRS Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B				

Note: Data movement is as follows:



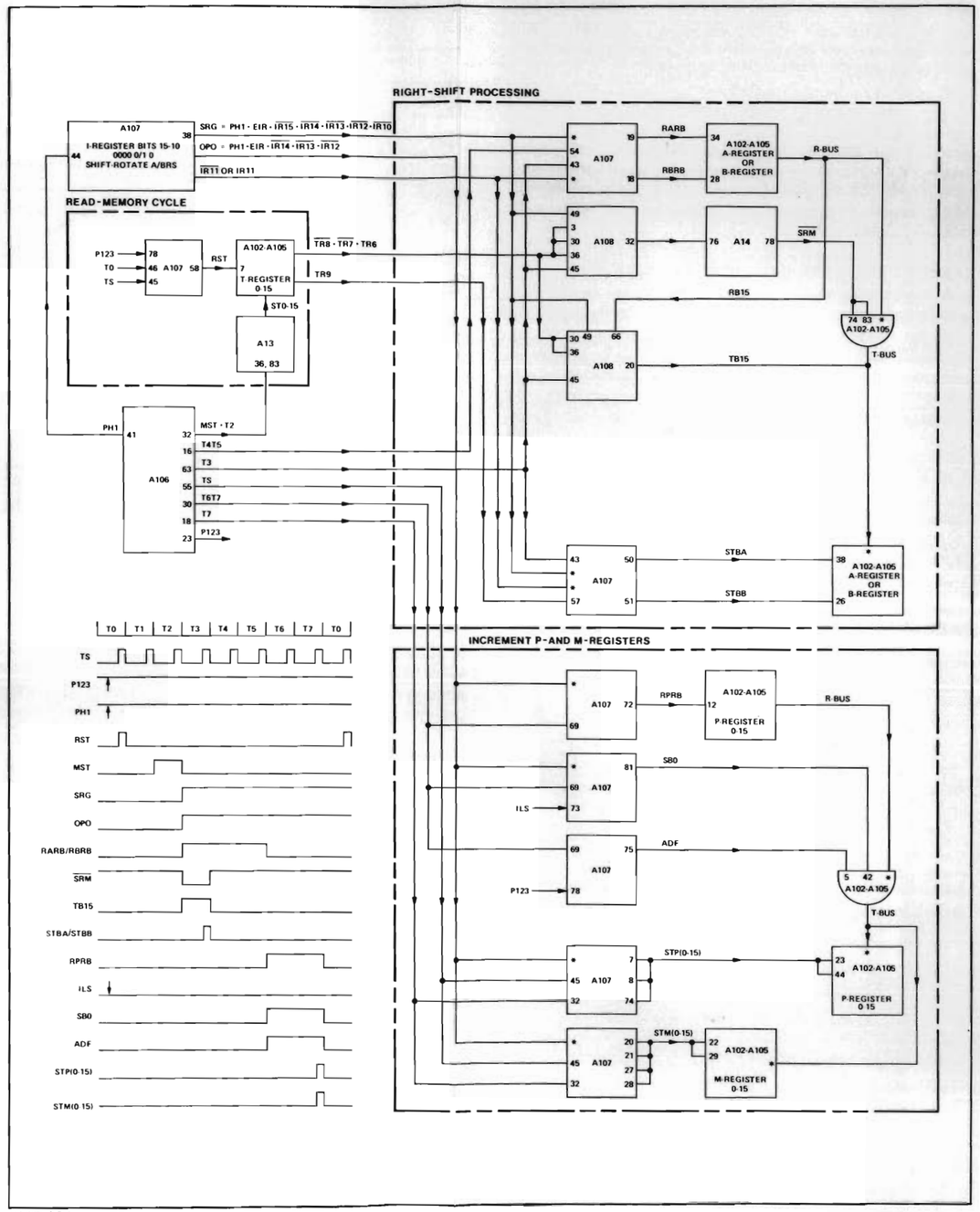


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Figure 4-61. A/BRS Instruction Processing Circuits, Servicing Diagram

4-287. RA/BL INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the RA/BL instruction. Processing operations are summarized in table 4-26. Point-to-point signal flow during phase 1 is shown in figure 4-62.

4-288. Description. The RA/BL instruction reads a number from the A- or B-register and moves all bits of that number one position to the left. Bit 15 is placed in bit position zero (see table 4-29). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-289. The RA/BL instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000000 or 000010 (bits 15 thru 10 respectively) in the I-register cause signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals $\overline{TR6}$, TR7, $\overline{TR8}$, and TR9 from the T-register cause the signals $\overline{SLM}$, $\overline{RLL}$, $\overline{SL14}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left (signals $\overline{SLM}$, $\overline{RLL}$, and $\overline{SL14}$), and the number stored back into the A- or B- register (signal STBA or STBB).

4-290. During time T6T7 signals RPRB, SB0, ADF, STP (0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-291. Test Procedure. To test the RA/BL instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001200 (RAL instruction) or 005200 (BAL instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the RAL instruction, or LOAD B switch if testing the BAL instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000, and the A-register should have 125252.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052525 in it.

h. At the computer front panel, press and release the RUN switch.

4-292. The computer is now in the run mode executing the RAL or BAL instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-62. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

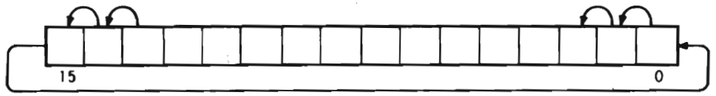
Note

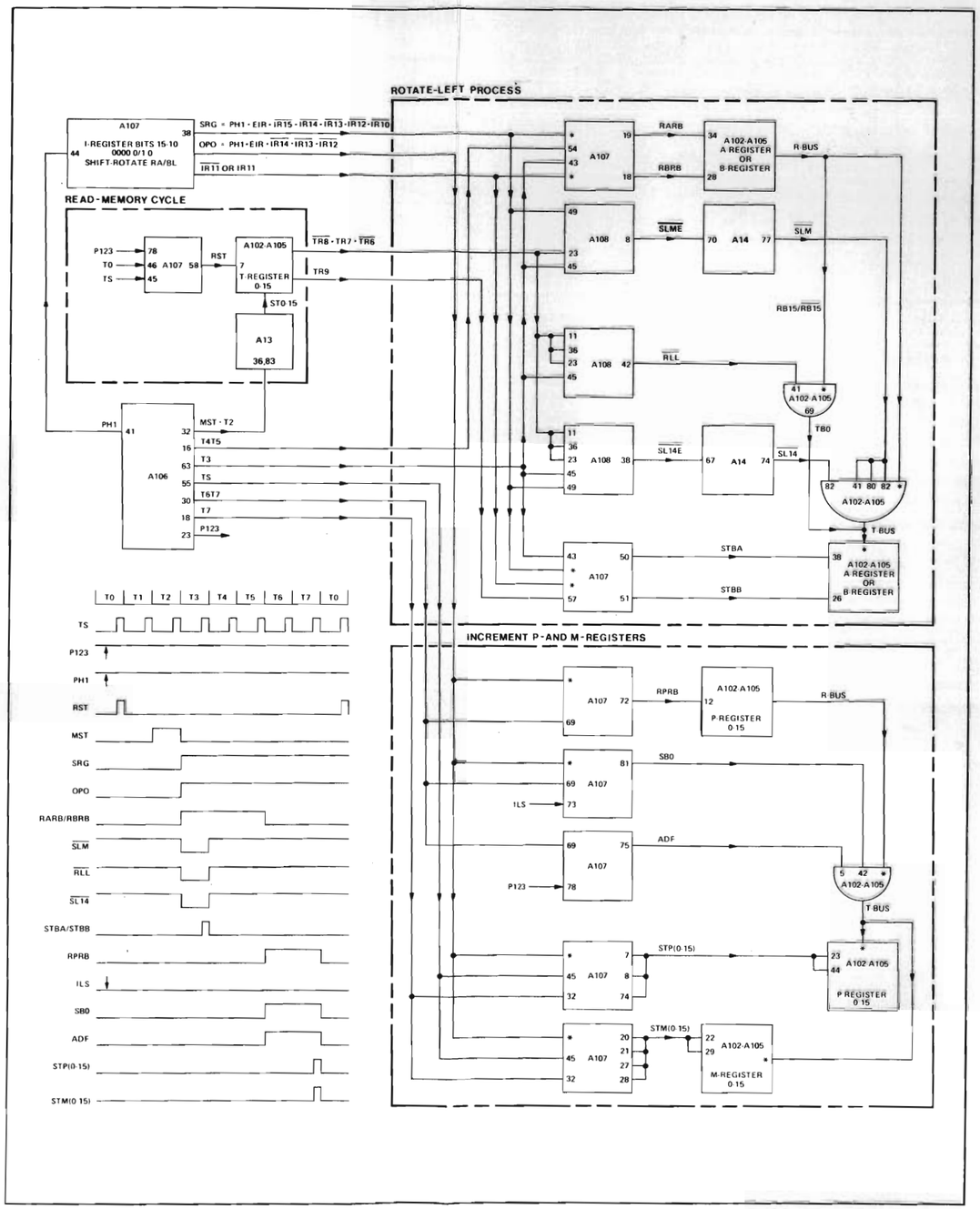
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-26. RA/BL Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus SLM, RLL, SL14 Store T Bus in A or B				

Note: Data movement is as follows:





2107-185

Figure 4-62. RA/BL Instruction Processing Circuits, Servicing Diagram

4-293. RA/BR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the RA/BR instruction. Processing operations are summarized in table 4-27. Point-to-point signal flow during phase 1 is shown in figure 4-63.

4-294. Description. The RA/BR instruction reads a number from the A- or B-register and moves all bits of that number one position to the right. Bit zero is placed in bit position 15 (see table 4-30). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-295. The RA/BR instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000000 or 000010 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPQ, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, TR7, $\overline{\text{TR8}}$, and TR9 from the T-register cause the signals $\overline{\text{SRM}}$, $\overline{\text{RRS}}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the right (signal $\overline{\text{SRM}}$ and $\overline{\text{RRS}}$), and the number stored back into the A- or B-register (signal STBA or STBB).

4-296. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-297. Test Procedure. To test the RA/BR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001300 (RAR instruction) or to 005300 (RBR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the RAR instruction, or LOAD B switch if testing the RBR instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 125252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052525 in it.

h. At the computer front panel, press and release the RUN switch.

4-298. The computer is now in the run mode executing the RAR or RBR instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-63. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

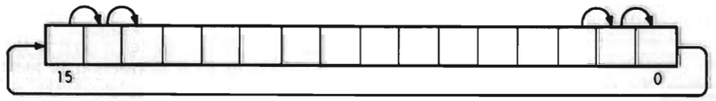
Note

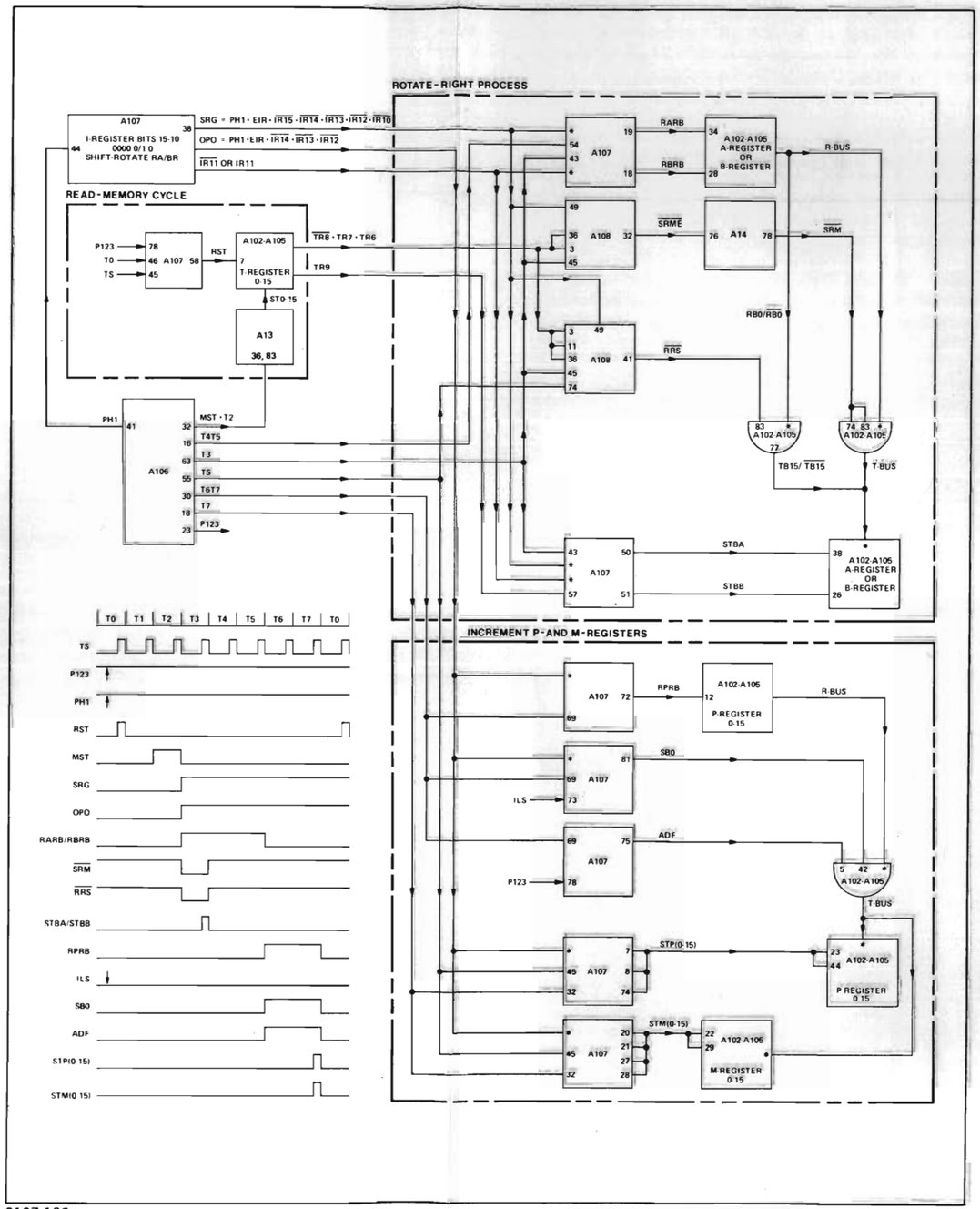
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-27. RA/BR Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus SRM, RRS Store T Bus in A or B				

Note: Data movement is as follows:





2107-186

Figure 4-63. RA/BR Instruction Processing Circuits, Servicing Diagram

4-299. A/BLR INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits used by the A/BLR instruction. Processing operations are summarized in table 4-28. Point-to-point signal flow during phase 1 is shown in figure 4-64.

4-300. Description. The A/BLR instruction reads a number from the A- or B-register and moves all bits of that number one position to the left. Bit 14 is discarded; replaced by bit 13. Bits 15 and 0 are cleared to "zero" (table 4-31). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-301. The A/BLR instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000000 or 000010 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals $\overline{TR6}$, $\overline{TR7}$, TR8, and TR9 from the T-register cause the signals $\overline{SLM}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left (signal $\overline{SLM}$), and the number stored back into the A- or B-register (signal STBA or STBB).

4-302. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-303. Test Procedure. To test the A/BLR instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001400 (ALR instruction) or 005400 (BLR instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ALR instruction, or the LOAD B switch if testing the BLR instruction. (To check bit 15, set the SWITCH REGISTER to 152525.)

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS SWITCH

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register will have 025252 in it.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052524 in it.

h. At the computer front panel, press and release the RUN switch.

4-304. The computer is now in the run mode executing the ALR or BLR instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-64. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

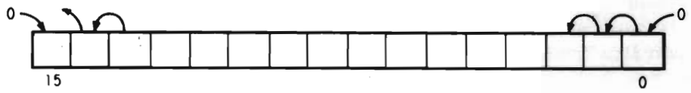
Note

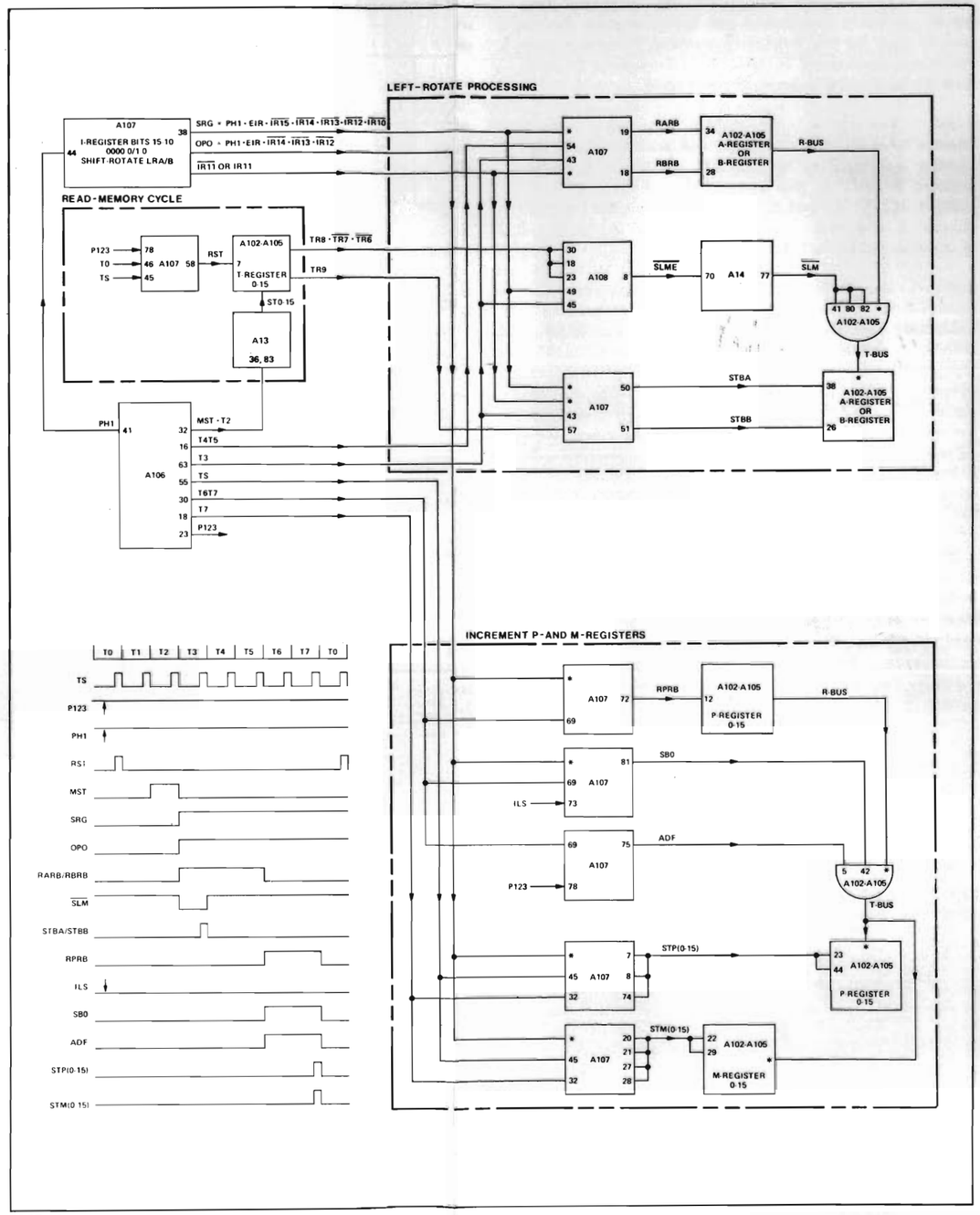
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-28. A/BLR Instruction Processing Operations

TIME PERIODS	T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)			
FETCH 1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M	
SHIFT-ROTATE INSTRUCTIONS				T3	T4	T5		
				All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
				Read A or B to R Bus Shift R Bus to T Bus SLM Store T Bus in A or B				

Note: Data movement is as follows:





2107-187

Figure 4-64. A/BLR Instruction Processing Circuits, Servicing Diagram

4-305. ERA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ERA/B instruction. Processing operations are summarized in table 4-29. Point-to-point signal flow during phase 1 is shown in figure 4-65.

4-306. Description. The ERA/B instruction reads a number from the A- or B-register and moves all bits of that number one position to the right. Bit zero is placed in the Extend register (E-register), and the E-register bit is placed in the bit 15 position (table 4-32). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-307. The ERA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000000 or 000010 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, TR7, TR8, and TR9 from the T-register cause the signals SRM, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the right and the E-register cleared or set depending on the state of signal RB0 (signal SRM). The number is then stored back into the A- or B-register (signal STBA or STBB).

4-308. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-309. Test Procedure. To test the ERA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001500 (ERA instruction) or 005500 (ERB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 052525 (alternate "ones" and "zeros") and press and release the LOAD A switch if testing the ERA instruction, or the LOAD B switch if testing the ERB instruction. (To check bit 15, set the SWITCH REGISTER to 152525.)

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them, the A-register should have 025252 or 125252 in it, and the E-register will be set (EXTEND indicator should go on).

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 112525 or 152525 in it, and the E-register will be cleared (EXTEND indicator should go out).

h. At the computer front panel, press and release the RUN switch.

4-310. The computer is now in the run mode executing the ERA or ERB instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-65. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

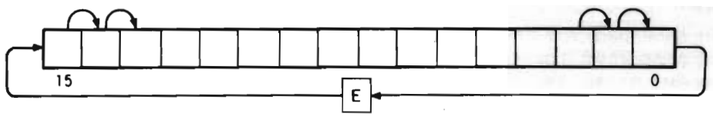
Note

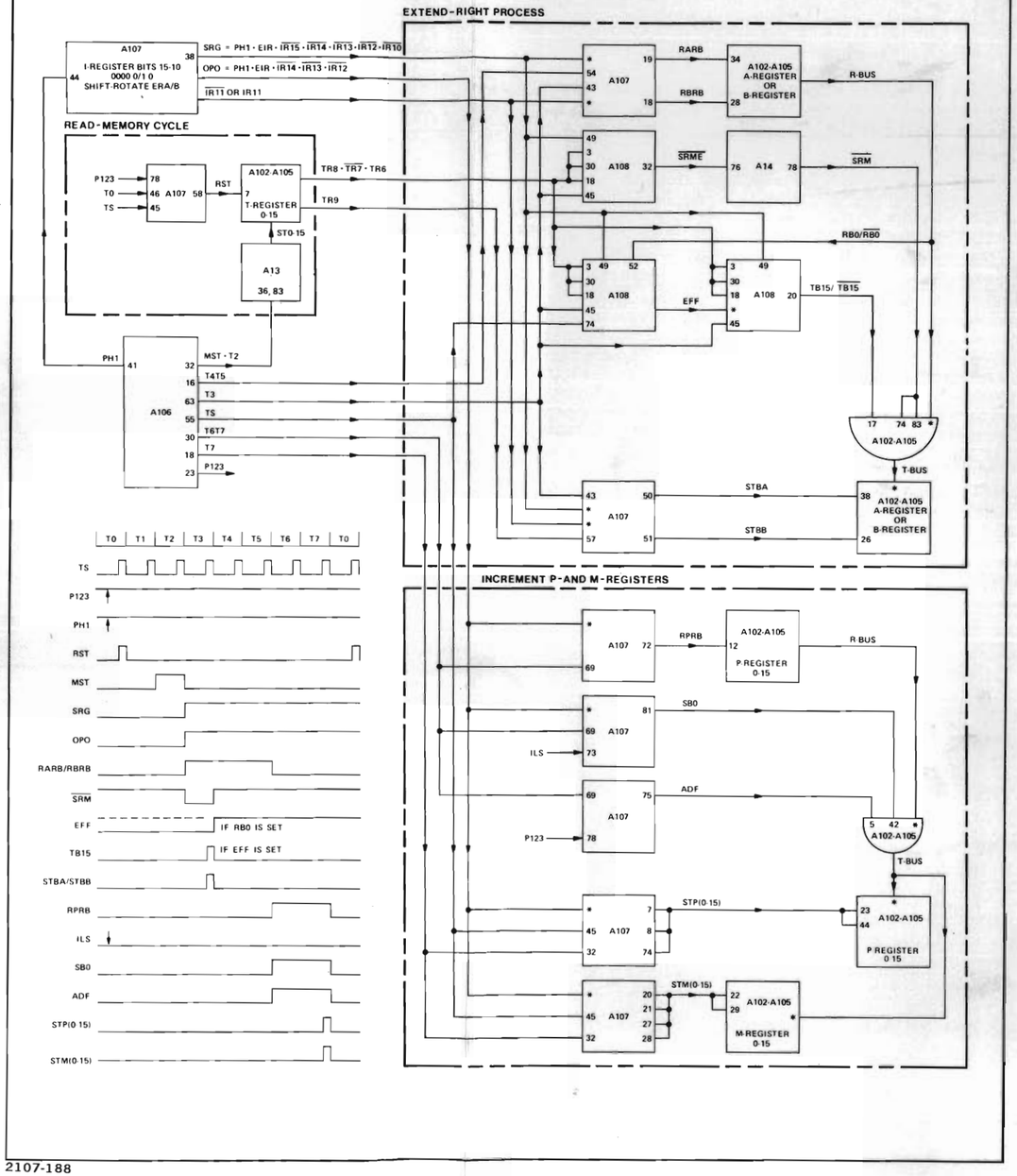
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-29. ERA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus SLM Store T Bus in A or B				

Note: Data movement is as follows:





2107-188

Figure 4-65. ERA/B Instruction Processing Circuits, Servicing Diagram

4-311. ELA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the ELA/B instruction. Processing operations are summarized in table 4-30. Point-to-point signal flow during phase 1 is shown in figure 4-66.

4-312. Description. The ELA/B instruction reads a number from the A- or B-register and moves all bits of that number one position to the left. Bit 15 is placed in the Extend register (E-register), and the E-register bit is placed in the bit zero position (see table 4-33). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-313. The ELA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000000 or 000010 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPO, RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, $\overline{TR7}$, TR8, and TR9 from the T-register cause the signals $\overline{SLM}$, $\overline{SL14}$, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved one position to the left and the E-register cleared or set depending on the state of signal RB0 (signal $\overline{SLM}$ and $\overline{SL14}$). The number is then stored back into the A- or B-register (signal STBA or STBB).

4-314. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-315. Test Procedure. To test the ELA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001600 (ELA instruction) or 005600 (ELB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 152525 and press and release the LOAD A switch if testing the ELA instruction, or LOAD B switch if testing the ELB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register should have 125252 or 125253 in it and the E-register should be set.

g. Repeat step f above. The P- and M-registers will have 001000 in them and the A-register should have 052525 or 052527 in it and the E-register should be cleared.

h. At the computer front panel, press and release the RUN switch.

4-316. The computer is now in the run mode executing the ELA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-66. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

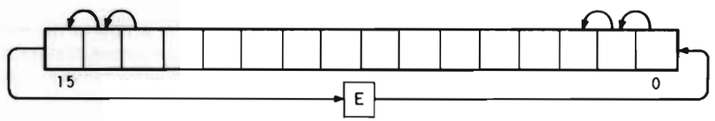
Note

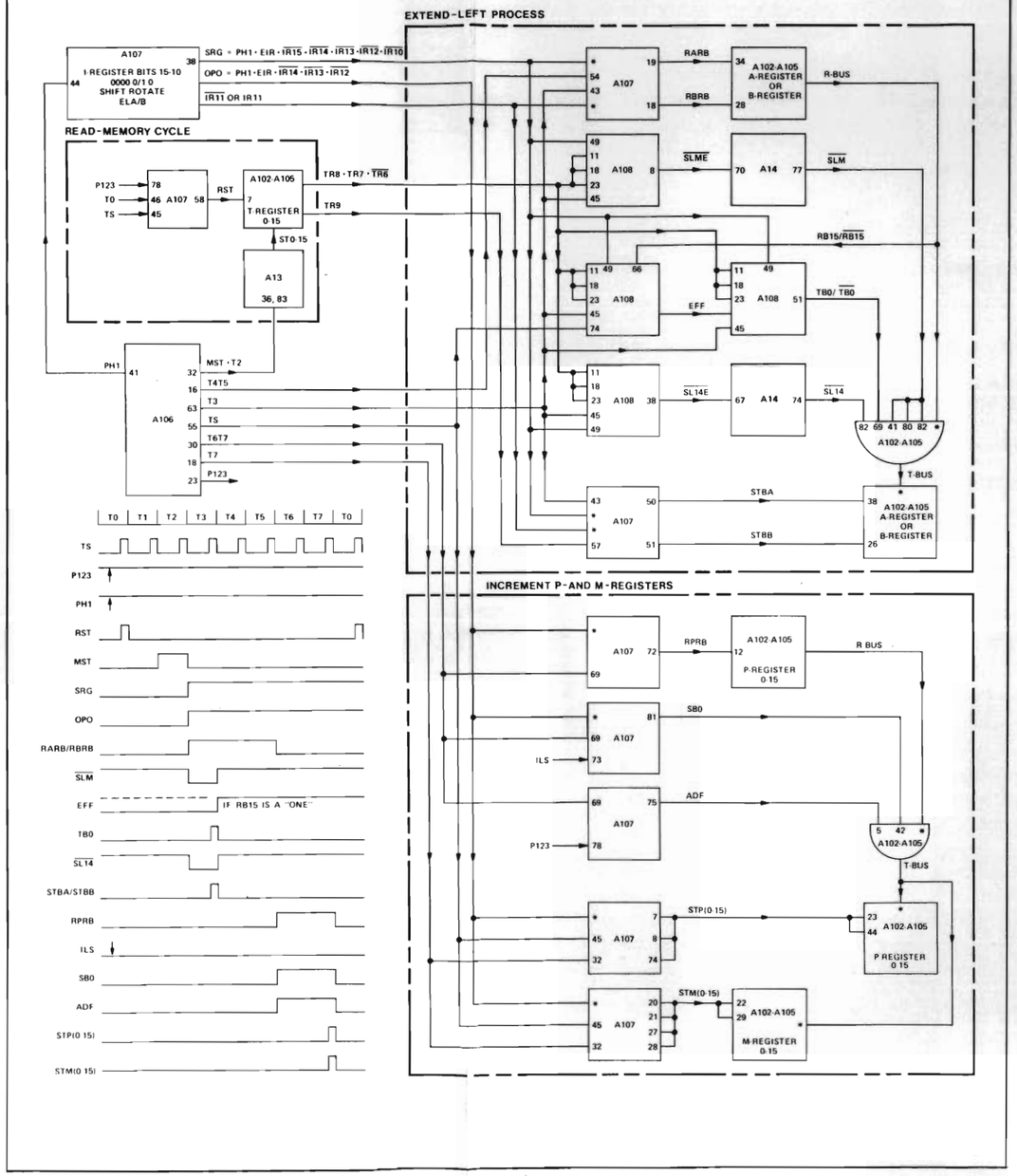
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-30. ELA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus SLM, SL14 Store T Bus in A or B				

Note: Data movement is as follows:





2107-189

Figure 4-66. ELA/B Instruction Processing Circuits, Servicing Diagram

4-317. A/BLF INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the A/BLF instruction. Processing operations are summarized in table 4-31. Point-to-point signal flow during phase 1 is shown in figure 4-67.

4-318. Description. The A/BLF instruction reads a number from the A- or B-register and moves all bits of that number four positions to the left. The high order bits are placed in the low order bit position (see table 4-34). At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-319. The A/BLF instruction is read from memory and executed during phase 1. During time T2 of phase 1 the 000000 or 000010 (bits 15 thru 10 respectively) in the I-register causes signals SRG, OPO, and RARB or RBRB to be generated during time T3. These signals in combination with signals TR6, TR7, TR8, and TR9 from the T-register cause the signals RL4, and STBA or STBB to be generated. These signals cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), the bits of the number moved four positions to the left (signal RL4), and the number stored back into the A- or B-register (signal STBA or STBB).

4-320. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-321. Test Procedure. To test the A/BLF instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 001700 (ALF instruction) or 005700 (BLF instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 152525 and press and release the LOAD A switch if testing the ALF instruction, or LOAD B switch if testing the BLF instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should remain at location 001000, and the A-register should have 052535 in it.

g. Repeat step f above. The P- and M-registers will remain at location 001000, and the A-register should have 052725 in it.

h. At the computer front panel, press and release the RUN switch.

4-322. The computer is now in the run mode executing the ALF instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-67. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

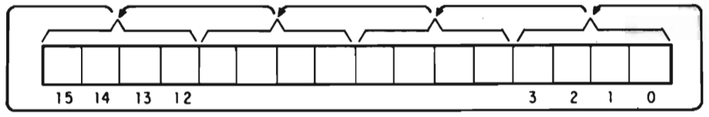
Note

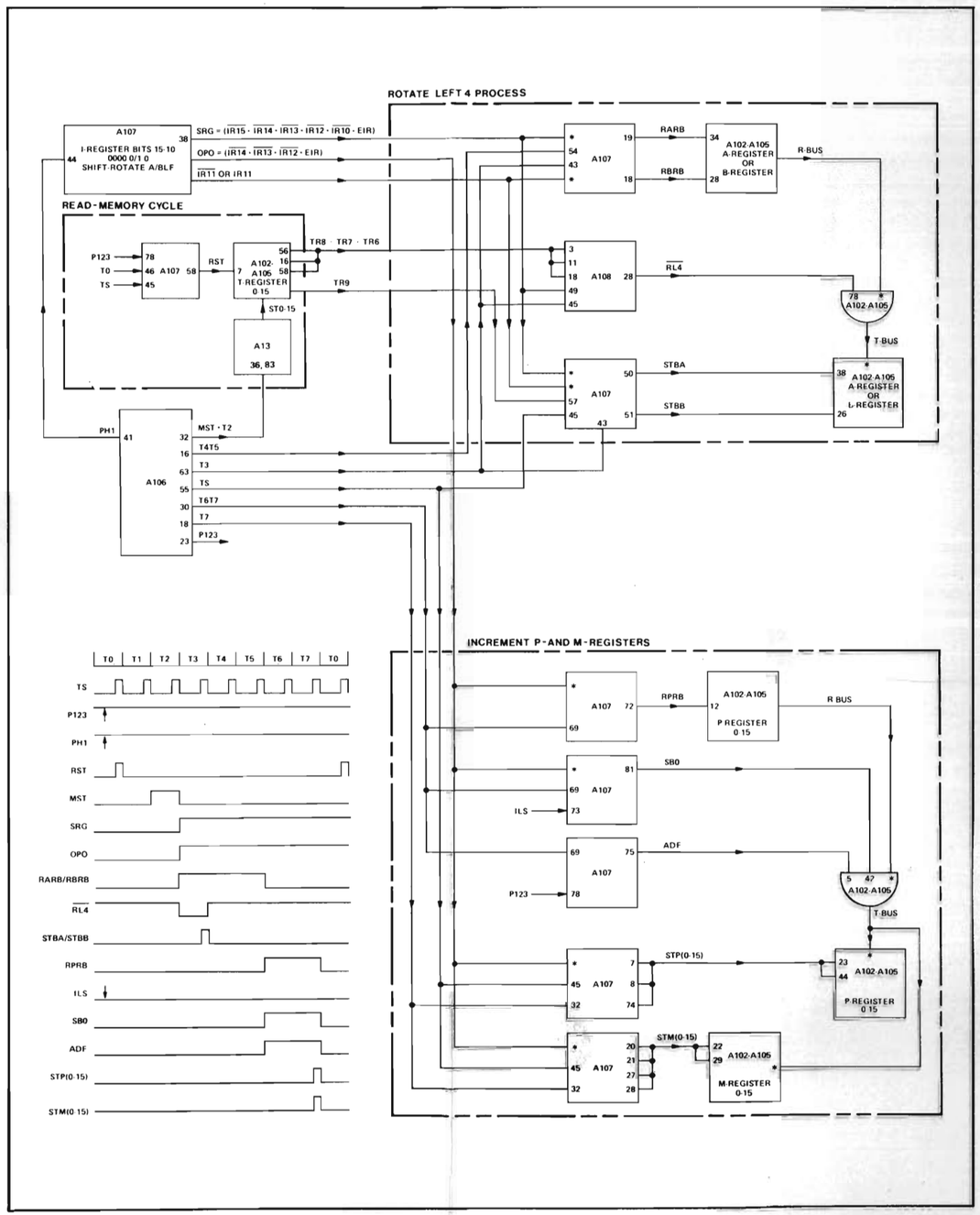
Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-31. A/BLF Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
SHIFT-ROTATE INSTRUCTIONS					T3	T4	T5		
					All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B	Clear E and Skips If TR5 = 1, CLE If TR3 = 1, SLA/B: Read A or B to R Bus If RB0 = 0, Set Carry	All Shifts and Rotates Read A or B to R Bus Shift R Bus to T Bus Store T Bus in A or B		
					Read A or B to R Bus Shift R Bus to T Bus RL4 Store T Bus in A or B				

Note: Data movement is as follows:





2107-190

Figure 4-67. A/BLF Instruction Processing Circuits, Servicing Diagram

4-323. CLA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CLA/B instruction. Processing operations are summarized in table 4-32. Point-to-point signal flow during phase 1 is shown in figure 4-68.

4-324. Description. The CLA/B instruction resets the A- or B-register. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 or 000011 (bits 15 thru 10 respectively) in the I-register causes signals ASG and OPO to be generated during time T3. These signals in combination with signal TR8 from the T-register cause the signals $\overline{EOF}$ and STBA or STBB to be generated also at time T3. These signals cause the R- and S-buses to be combined and transferred to the T-bus (signal $\overline{EOF}$), and the T-bus data (zeros) to be stored in the A- or B-register (signal STBA or STBB).

4-325. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-326. Test Procedure. To test the CLA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002400 (CLA instruction) or 006400 (CLB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 177777 and press and release the LOAD A switch if testing the CLA instruction, or LOAD B switch if testing the CLB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The A-register should be cleared to zero.

g. At the computer front panel, press and release the RUN switch.

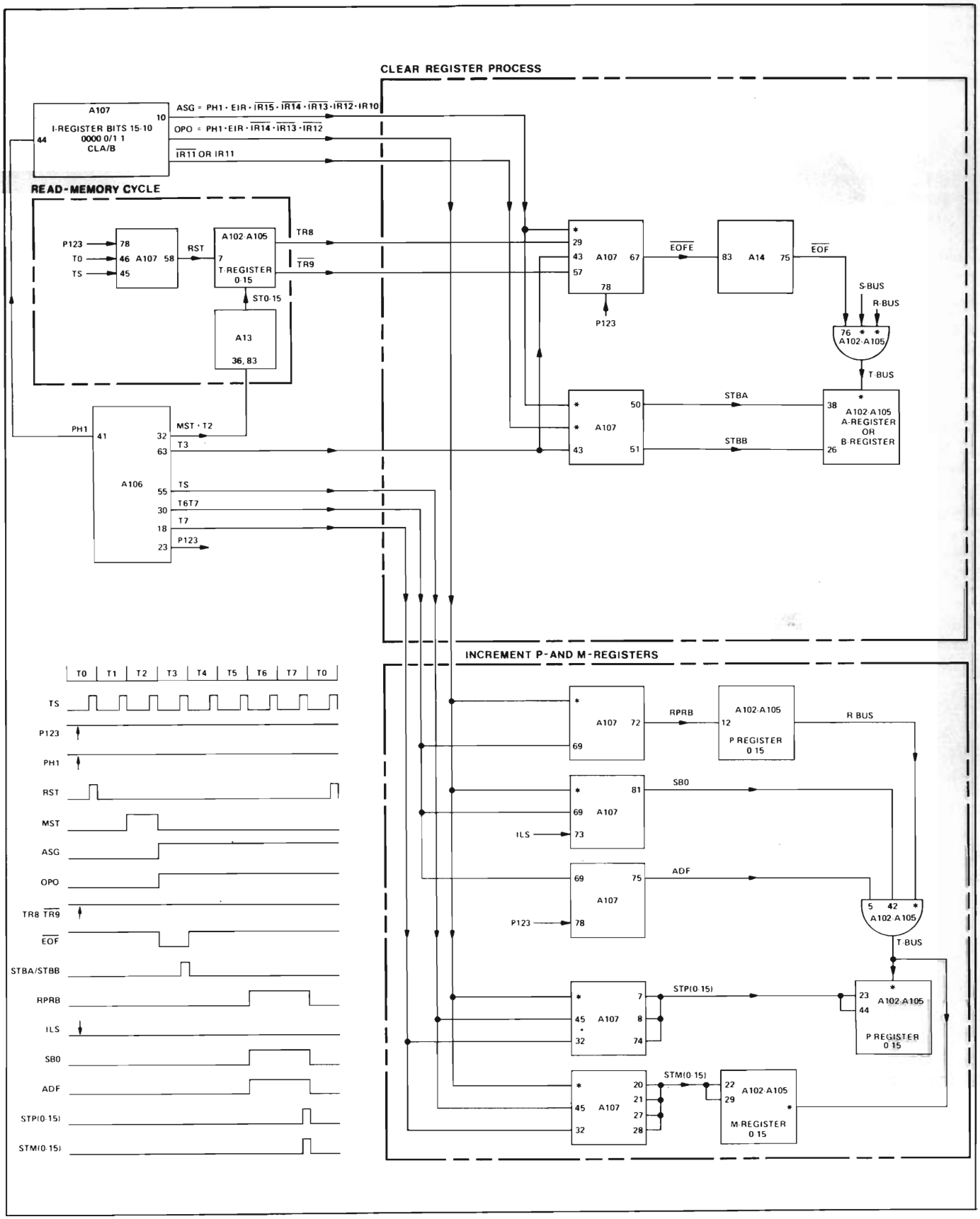
4-327. The computer is now in the run mode executing the CLA instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-68. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-32. CLA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5		
					No Read (R Bus all zeros) EOF Store T Bus in A/B				



2107-191

Figure 4-68. CLA/B Instruction Processing Circuits, Servicing Diagram

4-328. CMA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CMA/B instruction. Processing operations are summarized in table 4-33. Point-to-point signal flow during phase 1 is shown in figure 4-69.

4-329. Description. The CMA/B instruction compliments the data in the A- or B-register. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 or 000011 (bits 15 thru 10 respectively) in the I-register causes signals ASG and OPO to be generated during time T3. These signals in combination with signal $\overline{TR8}$ and $\overline{TR9}$ from the T-register cause the signals RARB or RBRB, $\overline{CMF}$, and STBA or STBB to be generated also at time T3. These signals cause the A- or B-register data to be read onto the R-bus (signal RARB or RBRB), the R-bus to be complimented and transferred to the T-bus (signal $\overline{CMF}$), and the T-bus data to be stored in the A- or B-register (signal STBA or STBB).

4-330. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-331. Test Procedure. To test the CMA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 003000 (CMA instruction) or 007000 (CMB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 177777 and press and release the LOAD A switch if testing the CMA instruction, or the LOAD B switch if testing the CMB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch twice. The A-register data should be complemented to "zeros" and then back to "ones".

g. At the computer front panel, press and release the RUN switch.

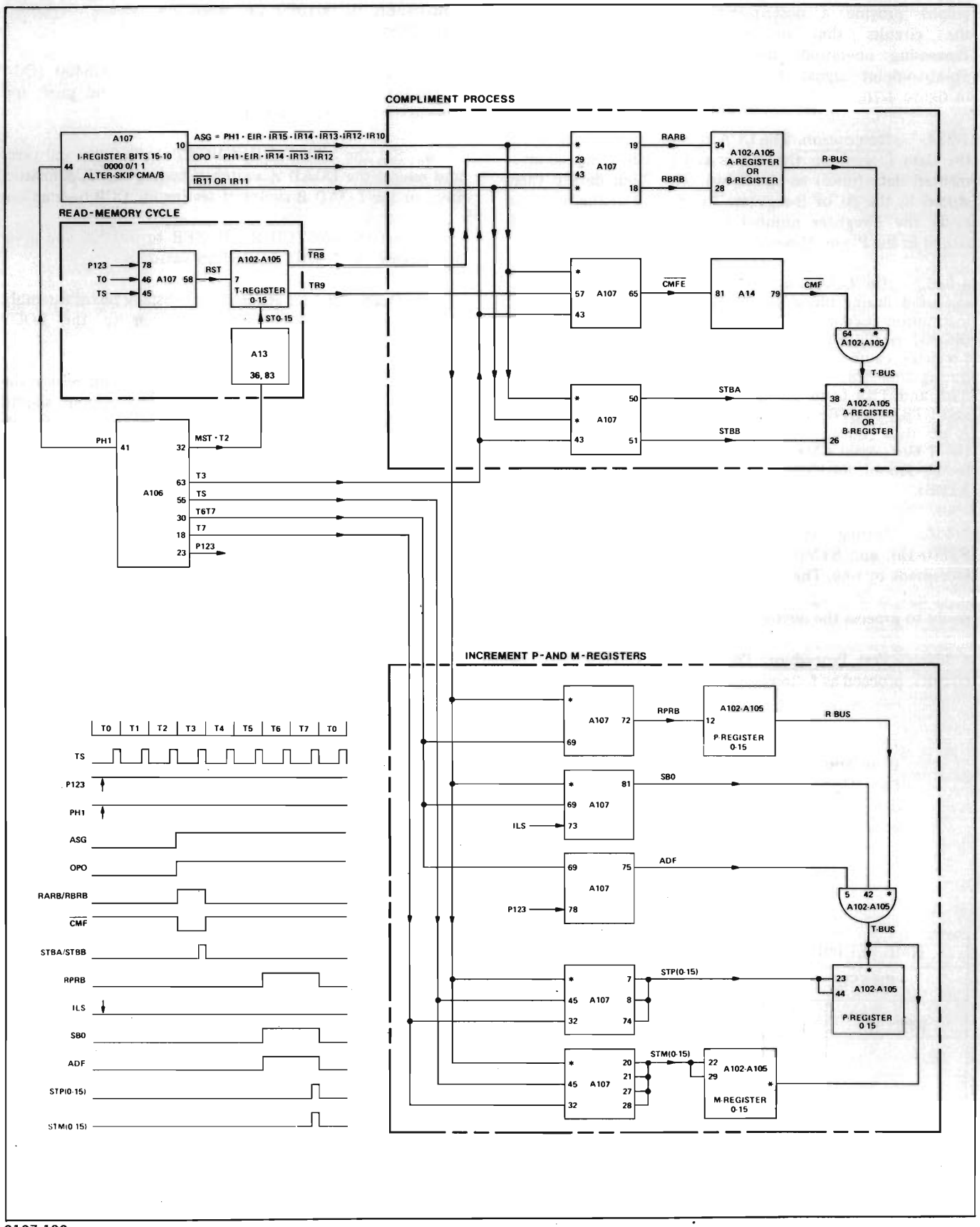
4-332. The computer is now in the run mode executing the CMA instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-69. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-33. CMA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5		
					Read A/B to R Bus CMF Store T Bus in A/B				



2107-192

Figure 4-69. CMA/B Instruction Processing Circuits, Servicing Diagram

4-333. CCA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CCA/B instruction. Processing operations are summarized in table 4-34. Point-to-point signal flow during phase 1 is shown in figure 4-70.

4-334. Description. The CCA/B instruction compliments the data (zeros) on the R-bus and transfers this complimented data (ones) to the T-bus. The T-bus data is then stored in the A- or B-register. At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

4-335. The CCA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 or 000011 (bits 15 thru 10 respectively) in the I-register causes signals ASG and OPO to be generated during time T3. These signals in combination with signals TR8 and TR9 from the T-register cause the signals $\overline{CMF}$, and STBA or STBB to be generated. These signals cause the R-bus data (zeros) to be complimented and transferred to the T-bus (signal $\overline{CMF}$), and the complimented data (ones) to be stored into the A- or B-register (signal STBA or STBB).

4-336. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-337. Test Procedure. To test the CCA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 003400 (CCA instruction) or 007400 (CCB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the CCA instruction, or the LOAD B switch if testing the CCB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should retain 001000 in them and the A-register should have 177777 in it.

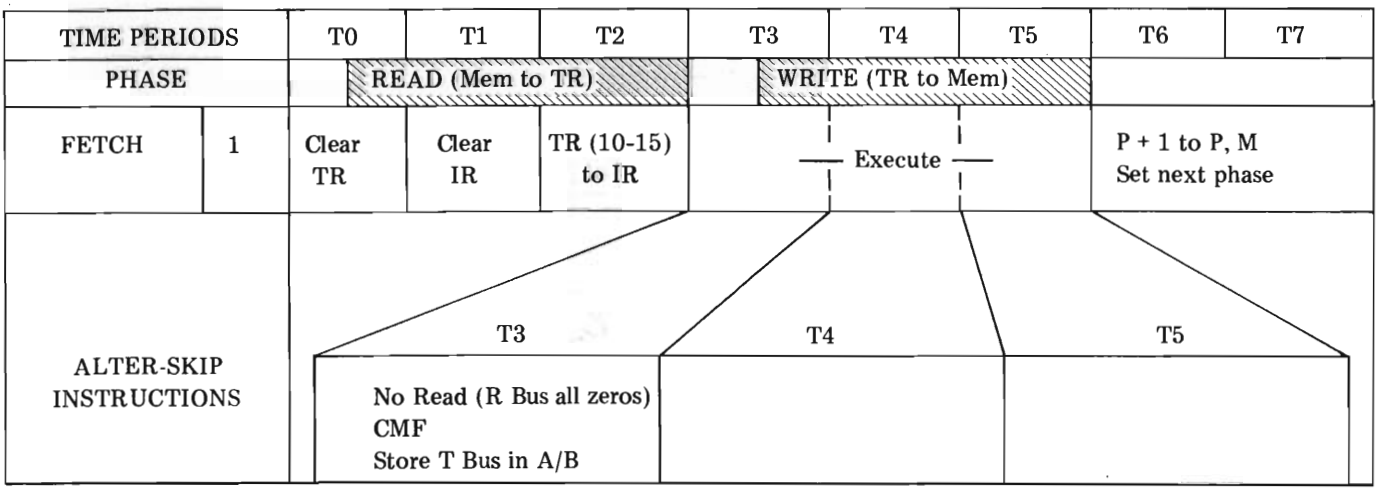
g. At the computer front panel, press and release the RUN switch.

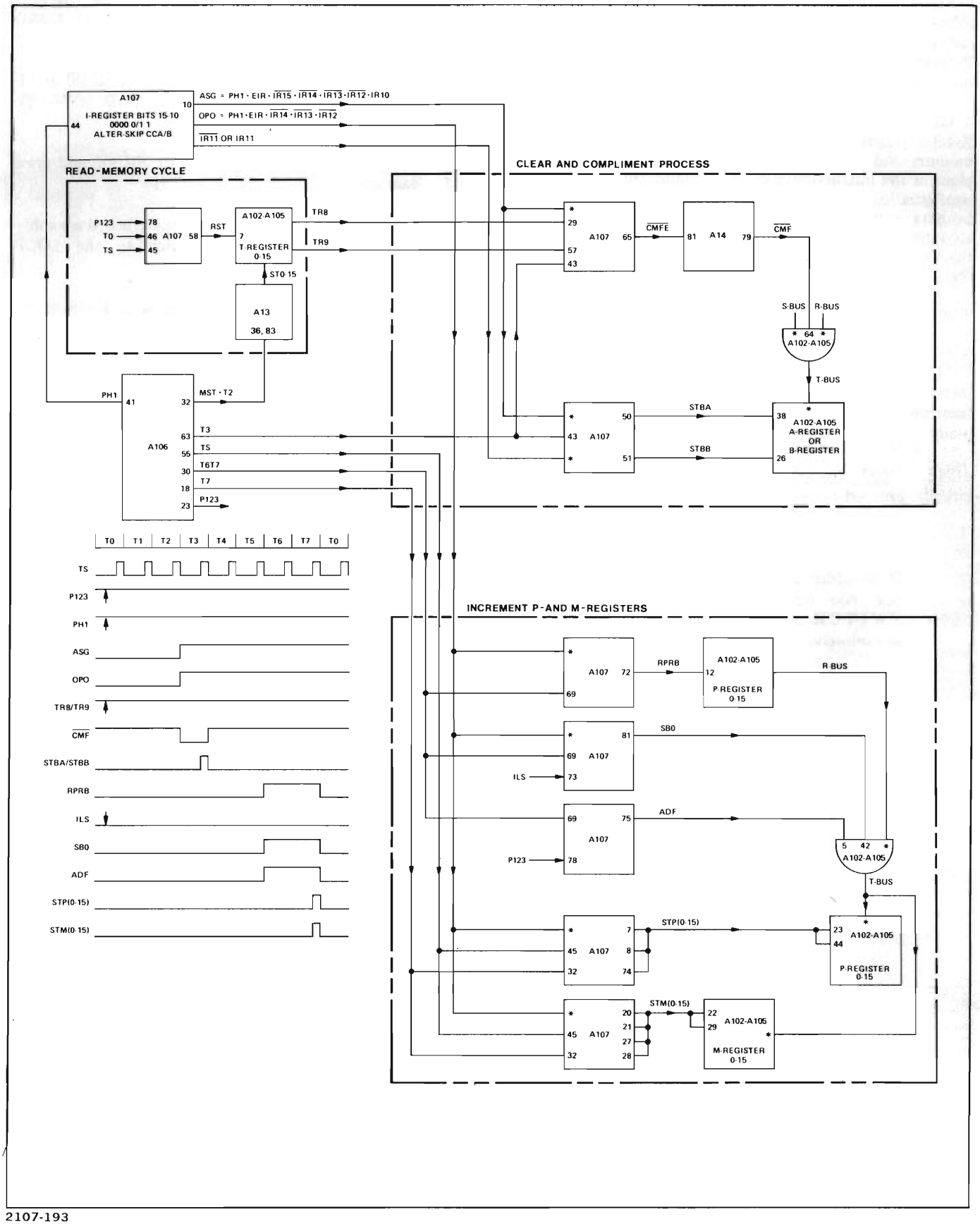
4-338. The computer is now in the run mode executing the CCA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-70. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-34. CCA/B Instruction Processing Operations





2107-193

Figure 4-70. CCA/B Instruction Processing Circuits, Servicing Diagram

4-339. CLE INSTRUCTION (Alter-Skip Group). The following paragraphs provide a description and test procedure for the circuits that process the CLE instruction. Processing operations are summarized in table 4-35. Point-to-point signal flow during phase 1 is shown in figure 4-71.

4-340. Description. The CLE instruction resets the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 (bits 15 thru 10 respectively) in the I-register causes signals ASG, OPO, and RARB to be generated during time T3. These signals in combination with signals TR6 and $\overline{TR7}$ from the T-register cause the E-register to reset at time T3TS. The A-register data is read onto the R-bus (signal RARB) during time T4T5 but is not used.

4-341. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-342. Test Procedure. To test the CLE instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002100 (CLE instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

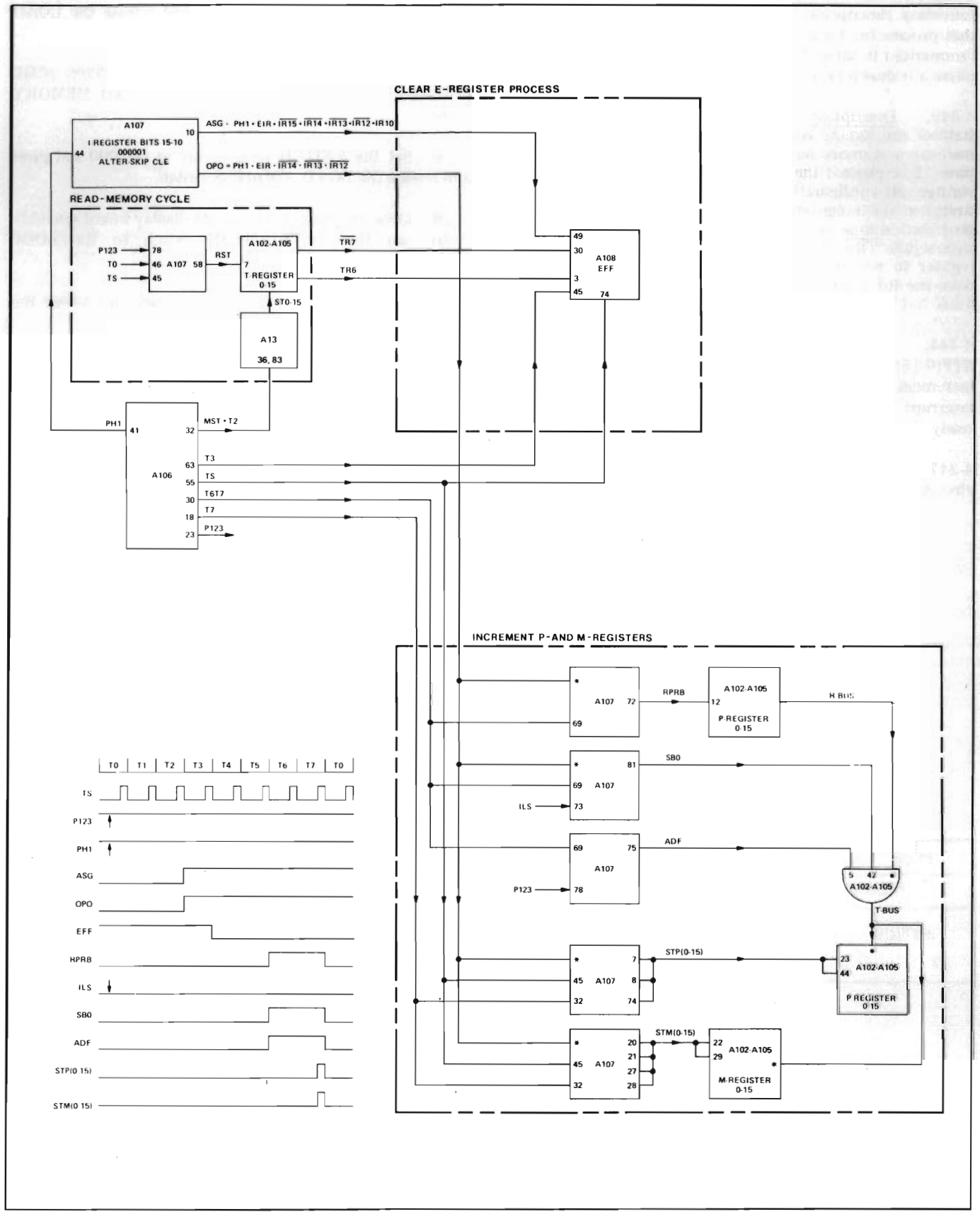
4-343. The computer is now in the run mode executing the CLE instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-71. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-35. CLE Instruction (Alter-Skip Group) Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS			T3: Reset E Flip-flop			T4		T5	



2107-194

Figure 4-71. CLE Instruction (Alter-Skip Group) Processing Circuits, Servicing Diagram

4-344. CME INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CME instruction. Processing operations are summarized in table 4-36. Point-to-point signal flow during phase 1 is shown in figure 4-72.

4-345. Description. The CME instruction reverses the state of the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 (bits 15 thru 10 respectively) in the I-register causes signals ASG and OPO to be generated during time T3. These signals in combination with signals $\overline{TR6}$ and TR7 from the T-register cause the E-register to reverse its state at time T3TS. The A-register data is read onto the R-bus (signal RARB) during time T4T5 but is not used.

4-346. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-347. Test Procedure. To test the CME instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002200 (CME instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

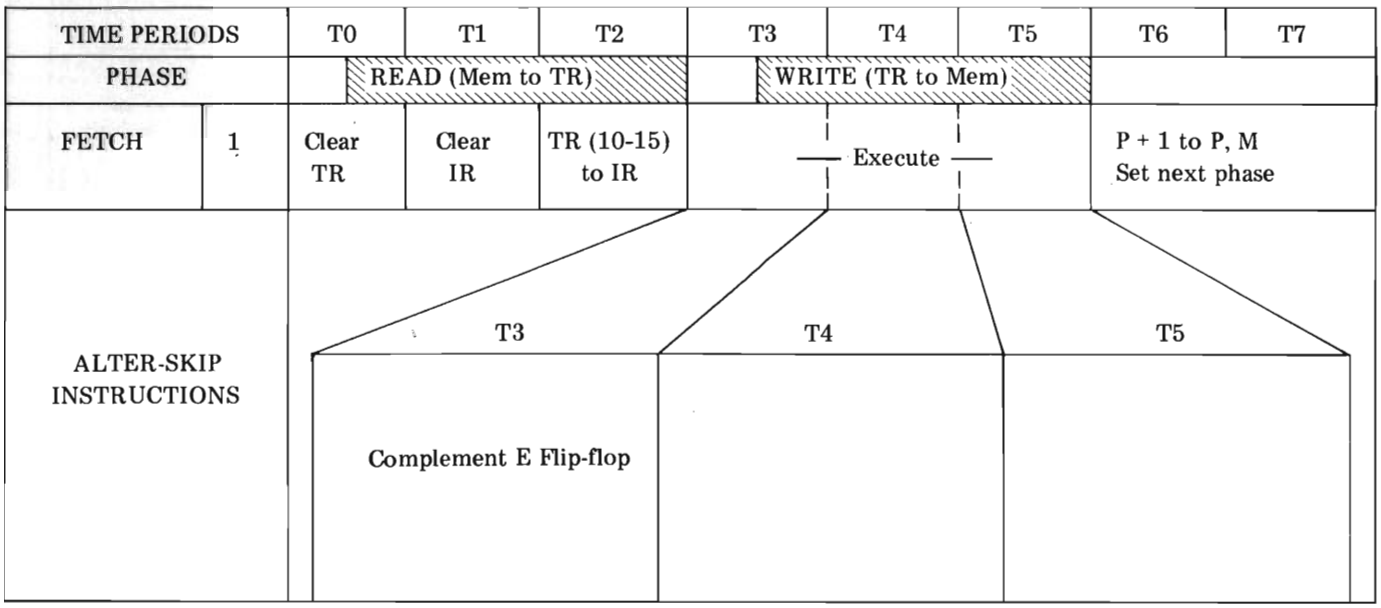
f. At the computer front panel, press and release the RUN switch.

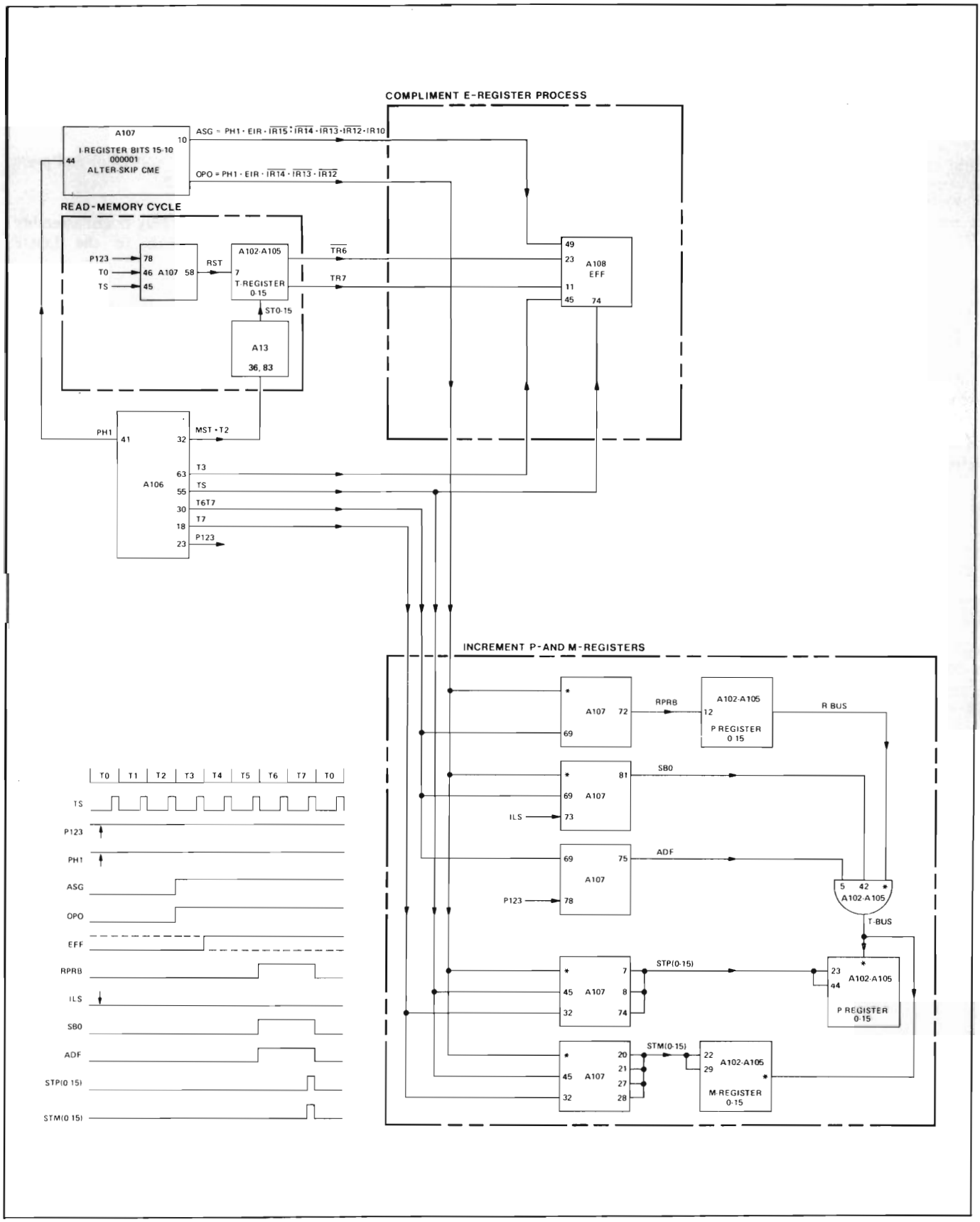
4-348. The computer is now in the run mode executing the CME instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-72. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-36. CME Instruction Processing Operations





2107-195

Figure 4-72. CME Instruction Processing Circuits, Servicing Diagram

4-349. CCE INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CCE instruction. Processing operations are summarized in table 4-37. Point-to-point signal flow during phase 1 is shown in figure 4-73.

4-350. Description. The CCE instruction sets the Extend register (E-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 (bits 15 thru 10 respectively) in the I-register causes signals ASG and OPO to be generated during time T3. These signals in combination with signals TR6 and TR7 from the T-register cause the E-register to set at time T3TS.

4-351. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-352. Test Procedure. To test the CCE instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002300 (CCE instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

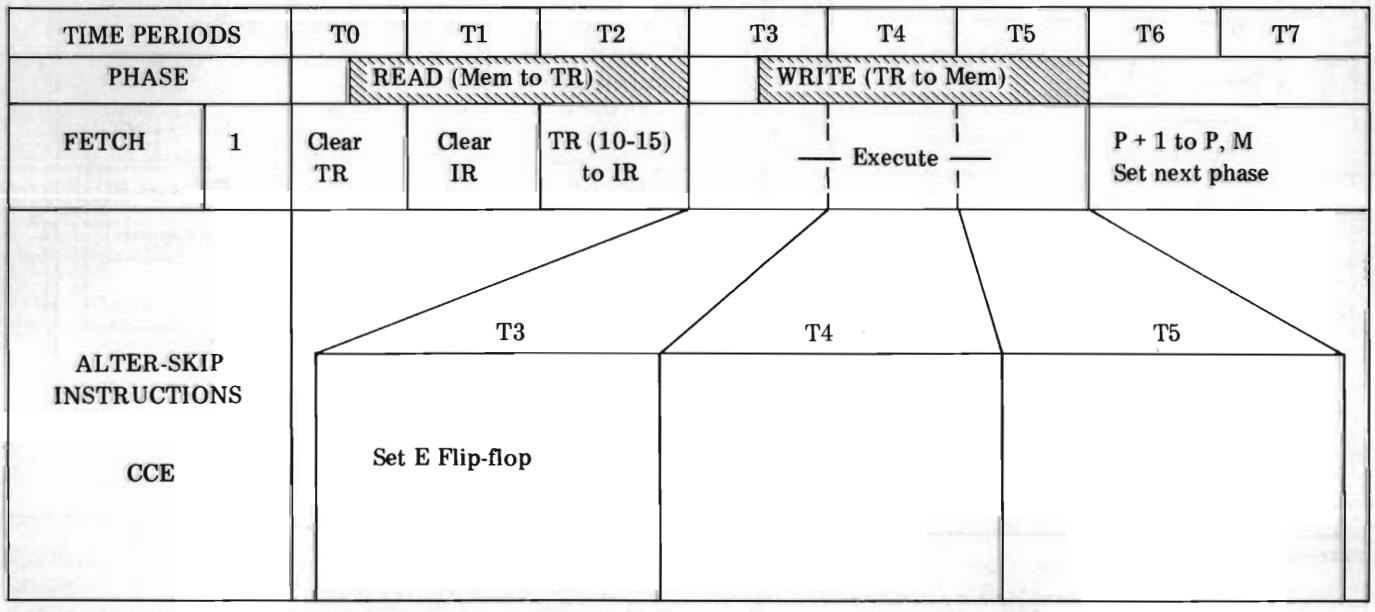
e. At the computer front panel, press and release the RUN switch.

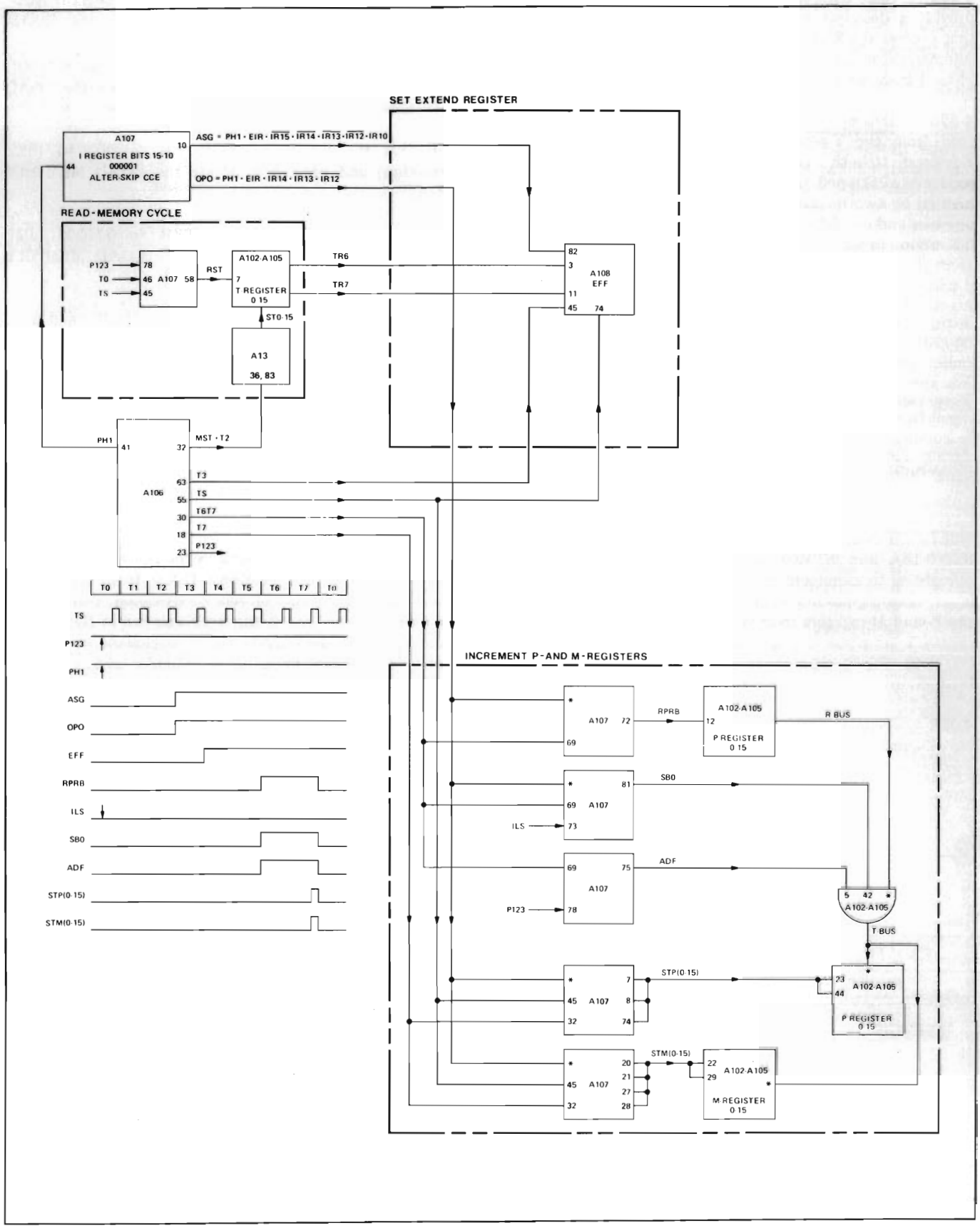
4-353. The computer is now in the run mode executing the CCE instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-73. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-37. CCE Instruction Processing Operations





2107-196

Figure 4-73. CCE Instruction Processing Circuits, Servicing Diagram

4-354. SEZ INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SEZ instruction. Processing operations are summarized in table 4-38. Point-to-point signal flow during phase 1 is shown in figure 4-74.

4-355. Description. The SEZ instruction compares bit zero from the T-register with the reset output of the E-register. If both signals are true, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If both signals are false or one true and one false, the program continues with the next instruction in sequence.

4-356. The SEZ instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 (bits 15 thru 10 respectively) in the I-register causes signals ASG and OPO to be generated during time T3. These signals in combination with signal TR5 from the T-register cause T-register bit zero ($\overline{TR0}$) signal and the signal from the reset side of the E-register flip-flop ($\overline{EFF}$) to be compared and the Carry FF (CFF) to set at time T3TS if signals $\overline{TR0}$ and $\overline{EFF}$ are both true. Signal CFF causes signal C0 to be generated at time T6T7.

4-357. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-358. Test Procedure. To test the SEZ instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002040 (SEZ instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the RUN switch.

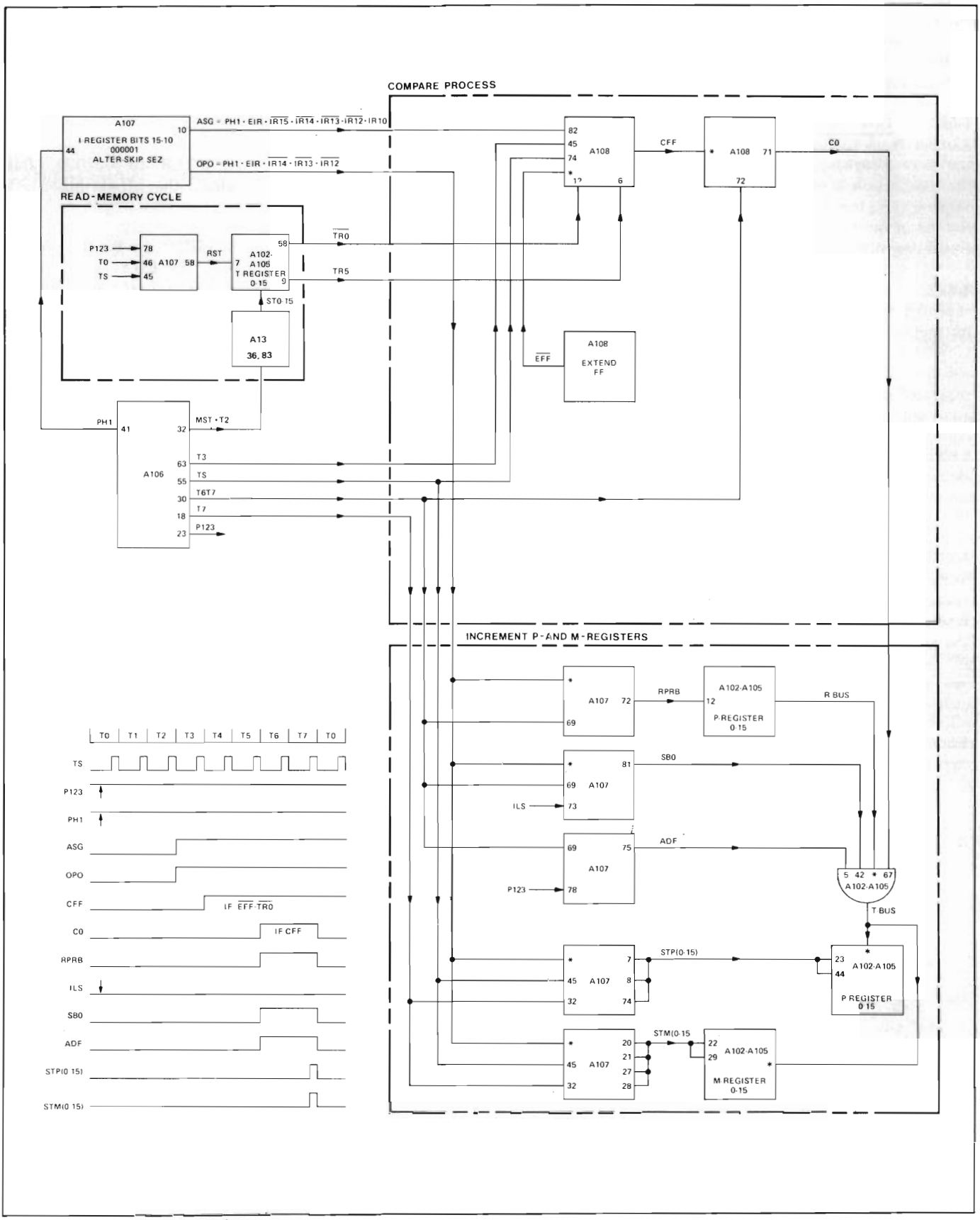
4-359. The computer is now in the run mode executing the SEZ instruction in location 001000. If the E-register is "zero" the JMP instruction will be executed. Using a dual-trace oscilloscope, check the signals shown in figure 4-74. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-38. SEZ Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P +1 +Carry to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5		
					Set Carry if: E = 0 and TR0 = 0, or E = 1 and TR0 = 1				



2107-197

Figure 4-74. SEZ Instruction Processing Circuits, Servicing Diagram

4-360. SSA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SSA/B instruction. Processing operations are summarized in table 4-39. Point-to-point signal flow during phase 1 is shown in figure 4-75.

4-361. Description. The SSA/B instruction reads a number from the A- or B-register and compares bit 15 of the A- or B-register with bit zero of the T-register (TR0). If the comparison is equal, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If the comparison is unequal, the program continues with the next instruction in sequence.

4-362. The SSA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 or 000011 (bits 15 thru 10 respectively) in the I-register causes signals ASG, OPO, and RARB or RBRB to be generated during times T3 and T4. These signals in combination with signal TR4 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), and the Carry FF (CFF) to set at time T4TS if bit zero of the T-register (TR0) and bit 15 of the R-bus (RB15) are equal (both true or both false). Signal CFF causes signal C0 to be generated at time T6T7.

4-363. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-364. Test Procedure. To test the SSA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002020 (SSA instruction) or 006020 (SSB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (equal compare) and press and release the LOAD A switch if testing the SSA instruction, or the LOAD B switch if testing the SSB instruction. (Substitute 100000 for 000000 for an unequal compare.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

4-365. The computer is now in the run mode executing the SSA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-75. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

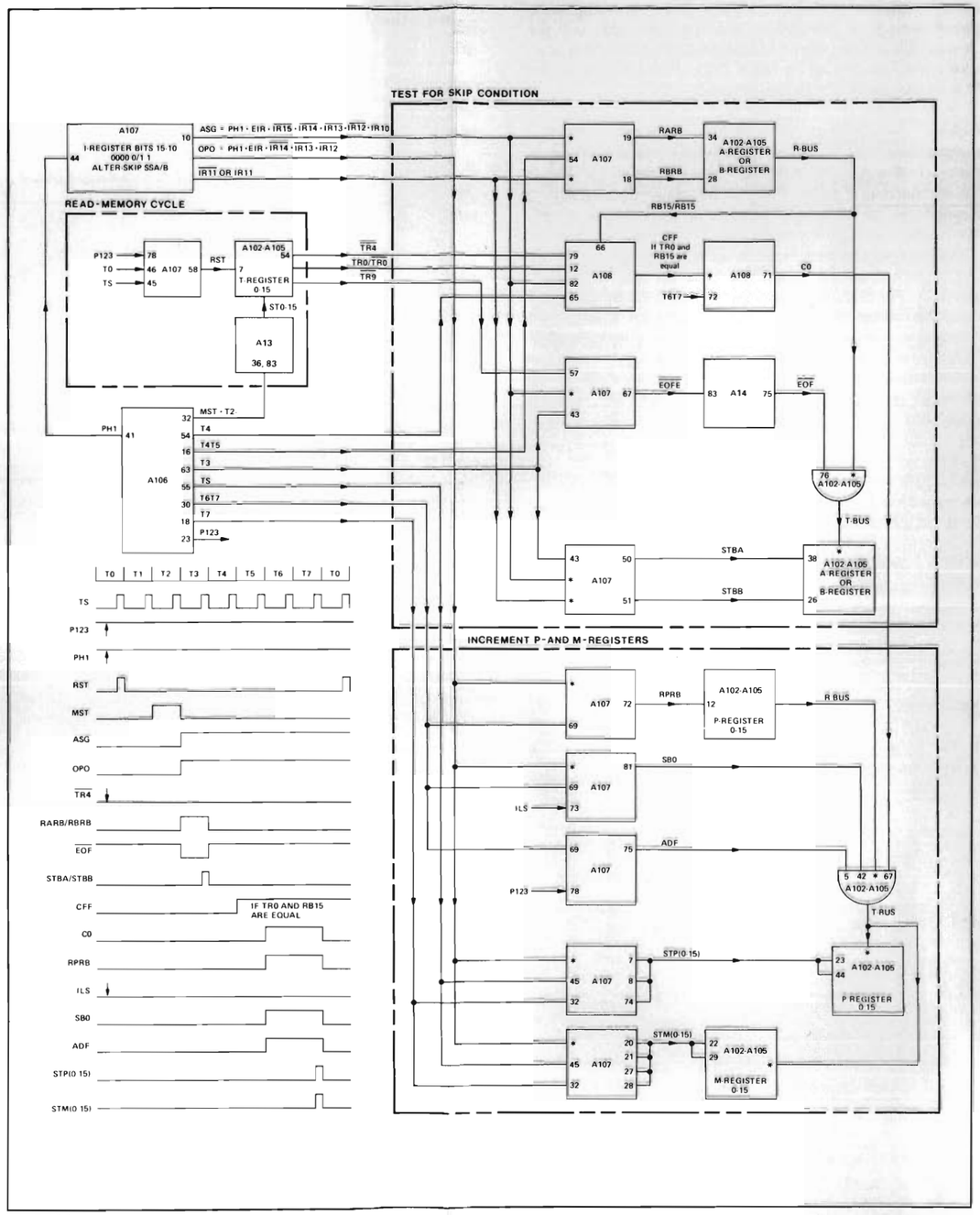
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-39. SSA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	—*Execute—			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5		
						Read A/B to R Bus Set Carry if: RB15 = 0 and TR0 = 0; or RB15 = 1 and TR0 = 1			

*Combination of SSA/B, SLA/B, and RSS is a special case; see paragraph 4-384.



2107-198

Figure 4-75. SSA/B Instruction Processing Circuits, Servicing Diagram

4-366. SLA/B INSTRUCTION (Alter-Skip Group). The following paragraphs provide a description and test procedure for the circuits that process the SLA/B instruction. The processing operations are summarized in table 4-40. Point-to-point signal flow during phase 1 is shown in figure 4-76.

4-367. Description. The SLA/B instruction reads a number from the A- or B-register and compares bit zero of the A- or B-register with bit zero of the T-register. If the comparison is equal, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If the comparison is unequal, the program continues with the next instruction in sequence.

4-368. The SLA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 or 000011 (bits 15 thru 10 respectively) in the I-register causes signals ASG, OPO, and RARB or RBRB to be generated during times T3 and T4. These signals in combination with signal TR3 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), and the Carry FF (CFF) to set at time T4TS if bit zero of the R-bus (signal RB0) and bit zero of the T-register (signal TR0) are equal (both true or both false). Signal CFF causes signal C0 to be generated at time T6T7.

4-369. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-370. Test Procedure. To test the SLA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002010 (SLA instruction) or 006010 (SLB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (equal compare) and press and release the LOAD A switch if testing the SLA instruction, or the LOAD B switch is testing the LSB instruction. (Substitute 000001 to 000000 for an unequal compare.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

4-371. The computer is now in the run mode executing the SLA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-76. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

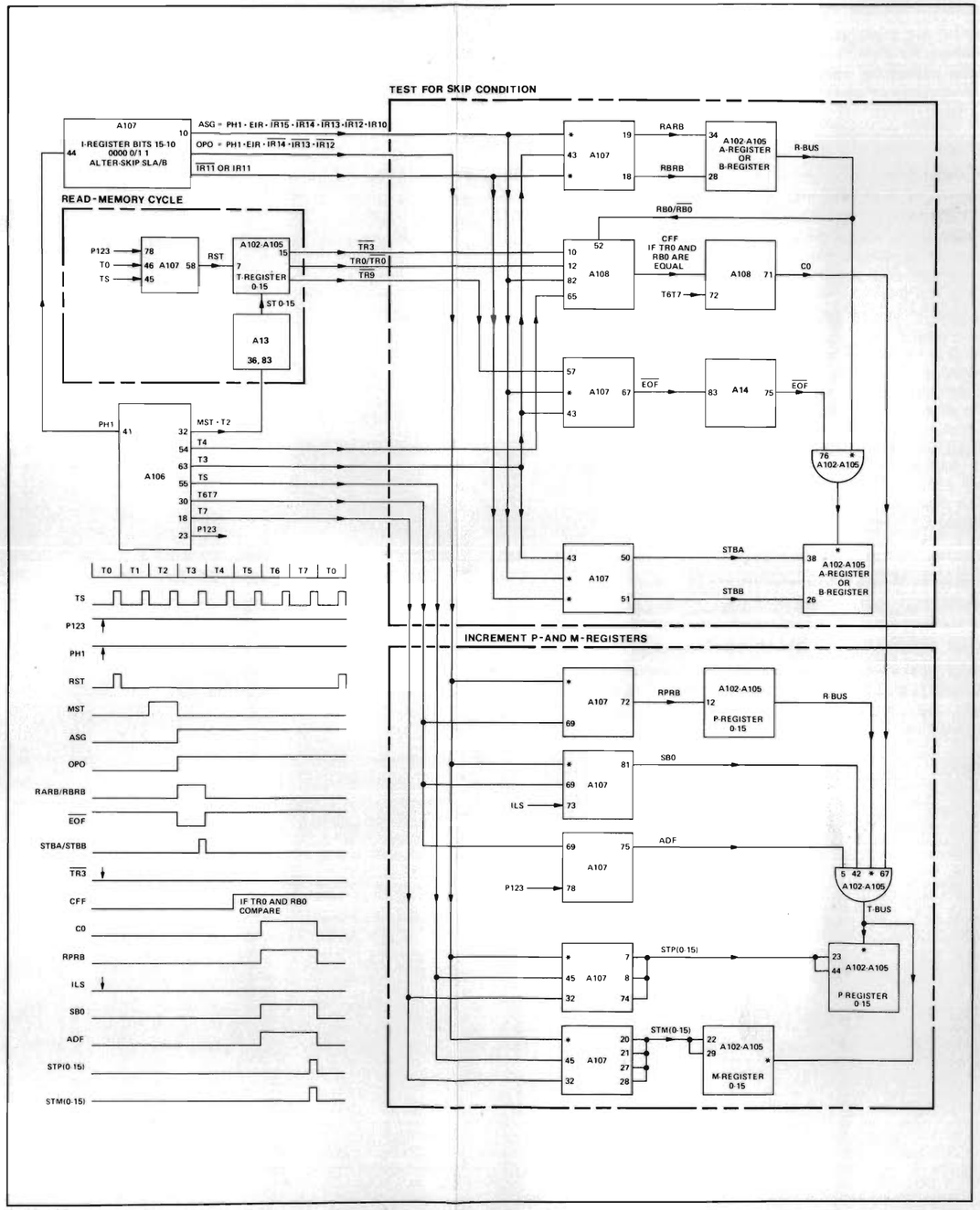
Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-40. SLA/B Instruction (Alter-Skip Group) Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR		*Execute		P +1 +Carry to P, M Set PH1	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5		
						Read A/B to R Bus Set Carry if: RB0 = 0 and TR0 = 0, or RB0 = 1 and TR0 = 1			

*Combination of SSA/B, SLA/B, and RSS is a special case; see paragraph 4-384.



2107-199

Figure 4-76. SLA/B Instruction (Alter-Skip Group) Processing Circuits, Servicing Diagram

4-372. INA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the INA/B instruction. The processing operations are summarized in table 4-41. Point-to-point signal flow during phase 1 is shown in figure 4-77.

4-373. Description. The INA/B instruction reads a number from the A- or B-register and increments that number by one. The incremented number is then stored back in the A- or B-register. At the end of the machine cycle the P-register number is incremented by one and stored in the P- and M-registers and the next phase is set.

3-374. The INA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 0000 0/11 (bits 15 thru 10 respectively) in the I-register causes signals ASG, OPO, RARB or RBRB, SB0, ADF, and STBA or STBB to be generated during time T4T5. These signals in combination with signal TR2 from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB) incremented by one and transferred to the T-bus (signals SB0 and ADF), and stored in the A- or B-register (signal STBA or STBB).

4-375. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-376. Test Procedure. To test the INA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002004 (INA instruction) or 006004 (INA instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 000000 and press and release the LOAD A switch if testing the INA instruction, or the LOAD B switch if testing the INB instruction.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001000 in them and the A-register will have 000001 in it.

h. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the RUN switch.

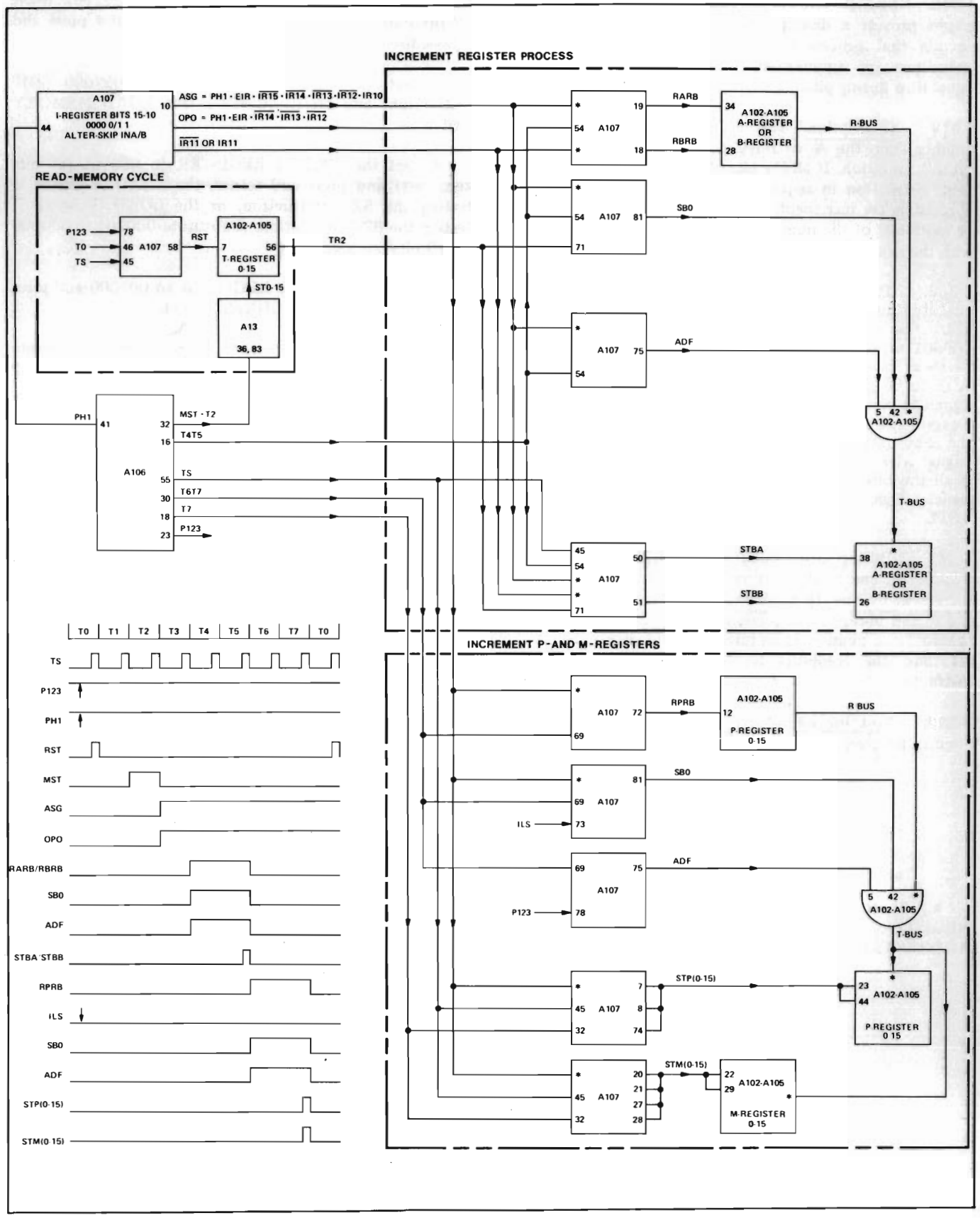
4-377. The computer is now in the run mode executing the INA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-77. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-41. INA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	— Execute —			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS			T3		T4: Read A/B to R Bus; Read "1" to S Bus; ADF; Store T Bus in A/B; If C16: Set E		T5: *Combination of SSA/B, SLA/B, and RSS is a special case; see text.		



2107-200

Figure 4-77. INA/B Instruction Processing Circuits, Servicing Diagram

4-378. SZA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SZA/B instruction. Processing operations are summarized in table 4-42. Point-to-point signal flow during phase 1 is shown in figure 4-78.

4-379. Description. The SZA/B instruction reads a number from the A- or B-register and checks it for an all "zero" condition. If all the bits of the number are zero, the next instruction in sequence is skipped (i.e., the P- and M-registers are incremented by two instead of one). If one or more bits of the number are one, the program continues with the next instruction in sequence.

4-380. The SZA/B instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 or 000011 (bits 15 thru 10 respectively) in the I-register causes signals ASG, OPO, RARB or RBRB, and ADF to be generated during times T3 through T5. These signals in combination with signals $\overline{TR0}$ and $\overline{TR1}$ from the T-register cause the A- or B-register number to be read onto the R-bus (signal RARB or RBRB), transferred to the T-bus (signal ADF), and the Carry FF (CFF) to set at time T5TS if all the bits of the T-bus are equal to zero (TAN gates signals). Signal CFF causes signal C0 to be generated at time T6T7.

4-381. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. In combination with signal C0 will cause the P- and M-register to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-382. Test Procedure. To test the SZA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002002 (SZA instruction) or 006002 (SZB instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 000000 (all bits zero test) and press and release the LOAD A switch if testing the SZA instruction, or the LOAD B switch if testing the SZB instruction. (Substitute 000001 to 000000 for all bits not zero test.)

e. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

f. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

g. At the computer front panel, press and release the SINGLE CYCLE switch. The P- and M-registers should have 001001 in them.

h. Repeat step g above. The P- and M-registers should have 001000 in them.

i. At the computer front panel, press and release the RUN switch.

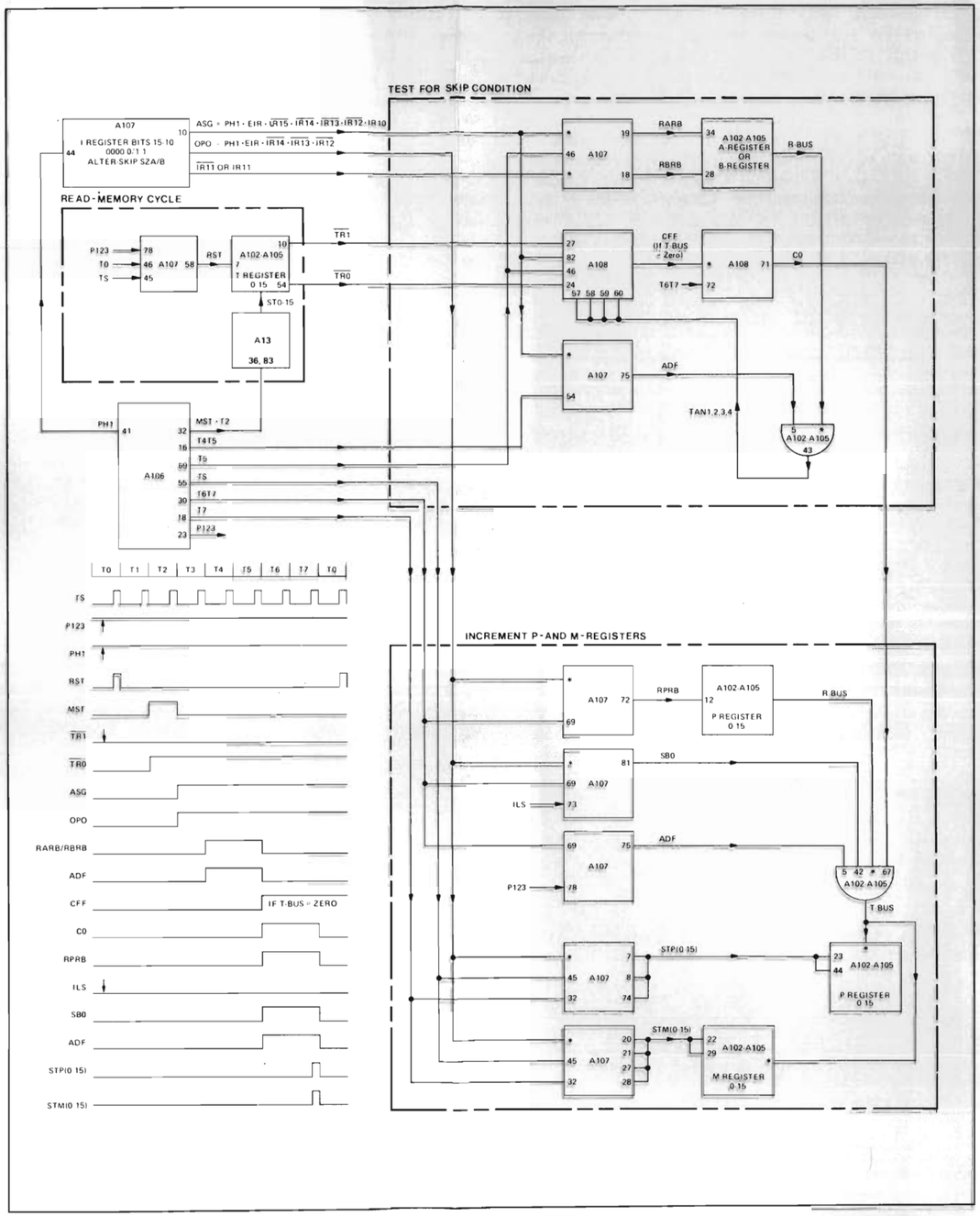
4-383. The computer is now in the run mode executing the SZA instruction in location 001000. Using a dual-trace oscilloscope, check the signals shown in figure 4-78. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-42. SZA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR	Execute			P + 1 to P, M Set next phase	
ALTER-SKIP INSTRUCTIONS					T3	T4	T5 Read A/B to R Bus IOF R Bus to T Bus Set Carry if: T Bus all zeros and TR0 = 0, or T Bus all ones and TR0 = 1		



2107-201

Figure 4-78. SZA/B Instruction Processing Circuits, Servicing Diagram

4-384. RSS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the RSS instruction.

4-385. Description. The RSS instruction, when processed alone (not in combination with any of the other ASG skip instructions), or when processed in combination with any of the ASG non-skip instructions, causes an unconditional skip to occur. Normally the other ASG skip instructions will cause a skip to occur when a zero condition is sensed. When the RSS instruction is used in combination with any of the other ASG skip instructions a skip will occur when a non-zero condition is sensed. Only when used in combination with the SSA/B or SLA/B instructions, must bits 15 and 0 both be true for the skip to occur. At the end of the machine cycle the P-register number is incremented by one if no skip condition has been generated, or is incremented by two if a skip condition has been generated. The incremented number is then stored in the P- and M-registers and the next phase is set.

4-386. The RSS instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 000001 or 000011 (bits 15 thru 10 respectively) in the I-register causes signals ASG and OPO to be generated during time T3. These signals in combination with signal TR0 from the T-register cause the Carry FF (CFF) to be set. Signal CFF causes signal C0 to be generated at time T6T7.

4-387. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) normally cause the P- and M-registers to increment by one. However, if the Carry FF is set, these signals in combination with signal C0 will cause the P- and M-registers to increment by two. The next phase (phase 1, or phase 4 if an interrupt is in progress) is then set, and the computer is ready to process the next instruction.

4-388. Test Procedure. The RSS instruction is tested in combination with the SEZ instruction (paragraph 4-354). To test the RSS instruction circuits proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 002041 (SEZ and RSS instructions) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the RUN switch.

4-389. The computer is now in the run mode executing the SEZ and RSS instructions in location 001000. The signal C0 will be generated if the E-register is set. Using a dual-trace oscilloscope, check the signals shown in figure 4-74. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

4-390. INPUT/OUTPUT INSTRUCTION PROCESSING CIRCUITS.

4-391. The circuits that process the 17 input/output instructions are shown in figures 4-79 through 4-90. Input/output instructions are used in the computer program to address a selected input/output location (select code) and specify a desired data transfer or control operation involving the select code which is addressed. (Four instructions included in the input/output instruction set are used to perform control operations involving the overflow register. For this reason, these four instructions are sometimes considered to be part of the register reference instruction set. However, for troubleshooting purposes they are treated as input/output instructions because they use the input/output instruction format.) Input/output instruction formats are shown in figure 4-1. The paragraphs which follow describe the purpose and use of each instruction, and explain how the processing circuits implement and execute the instructions. Tables summarizing the processing operations, and servicing diagrams showing signal flow and timing within the processing circuits, are included for reference during explanation and troubleshooting. Suggested troubleshooting test procedures are presented for each instruction.

4-392. HLT INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the HLT instruction. Processing operations are summarized in table 4-43. Point-to-point signal flow during phase 1 is shown in figure 4-79.

4-393. Description. The HLT instruction clears RUN FF 1 and RUN FF 2, turns off the RUN indicator, turns on the HALT indicator and the FETCH indicator, and enables the front panel switches. It also causes the A- or B-register data

to be transferred to the T-bus but makes no use of this data. It clears any addressed I/O device FLAG FF if bit 9 of the instruction (signal TR9) is true. At the end of the machine cycle, the P-register number is incremented by one and stored in the P- and M-registers and phase 1 is set.

4-394. The HLT instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 (bits 15 thru 10 respectively) in the I-register causes signals IOG, OPO, and RARB or RBRB to be generated during time T3 through T5. These signals in combination with signals $\overline{TR6}$, $\overline{TR7}$, and $\overline{TR8}$ from the T-register cause the signal HIN to be generated at time T3 which clears the RUN FF 1 (RF1) at time T5. Clearing RUN FF 1 causes PH1 FF to set and the FETCH indicator to go on allowing RUN FF 2 (RF2) to clear at time T7S. Clearing RUN FF 2 causes the HALT indicator to go on, the RUN indicator to go off, and the front panel switches to be enabled. During times T3 through T5 the A- or B-register data is read onto the R-bus (signal RARB or RBRB), and transferred to the T-bus (signal $\overline{IOF}$) but is not used. During time T4 the INTERRUPT SYSTEM ENABLE FF and the I/O device FLAG FF whose address appears in the last six bits of the HLT instruction are cleared. (signals TR9 and CLF).

4-395. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer stops ready to process the next instruction.

4-396. Test Procedure. To test the HLT instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 103001 (HLT instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction) and press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At display board assembly A501, set the INSTRUCTION switch to the LOOP position.

f. At the computer front panel, press and release the RUN switch. The computer will appear to remain in the halt mode.

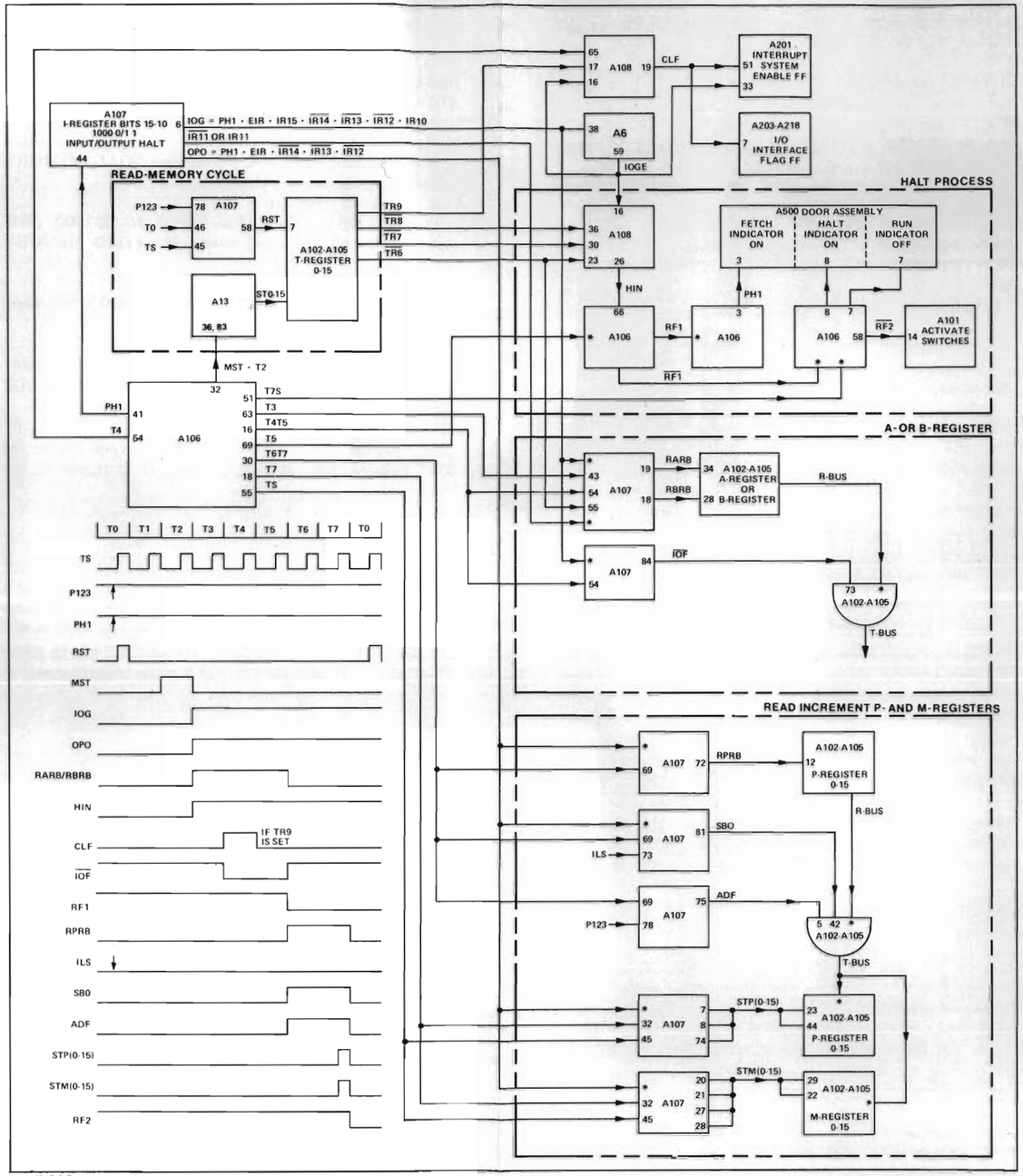
4-397. Using a dual-trace oscilloscope check the signals shown in figure 4-79 at the backplane connectors or at a specific card by using the extender card and the extender cable. The signals are generated each time the RUN switch is pressed. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-43. HLT Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR (10-15) to IR				P + 1 to P, M Reset Run FF Set PH1	



2107-202

Figure 4-79. HLT Instruction Processing Circuits, Servicing Diagram

4-398. STF INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the STF instruction. Processing operations are summarized in table 4-44. Point-to-point signal flow during phase 1 is shown in figure 4-80.

4-399. Description. The STF instruction sets the flag flip-flop addressed in the select code portion of the instruction. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 (bits 15 thru 10 respectively) in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the $\overline{TR8}$, $\overline{TR7}$, and TR6 signals from the T-register cause the STF signal to be generated at time T3. The IOGE signal in combination with the TR5, TR4, TR3, TR2, TR1, and TR0 signals from the T-register are used to address the desired computer or interface flip-flop. The STF signal then sets the flip-flop.

4-400. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.
ready to process the next instruction.

4-401. Test Procedure. To test the STF instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1021XX (STF instruction) and press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

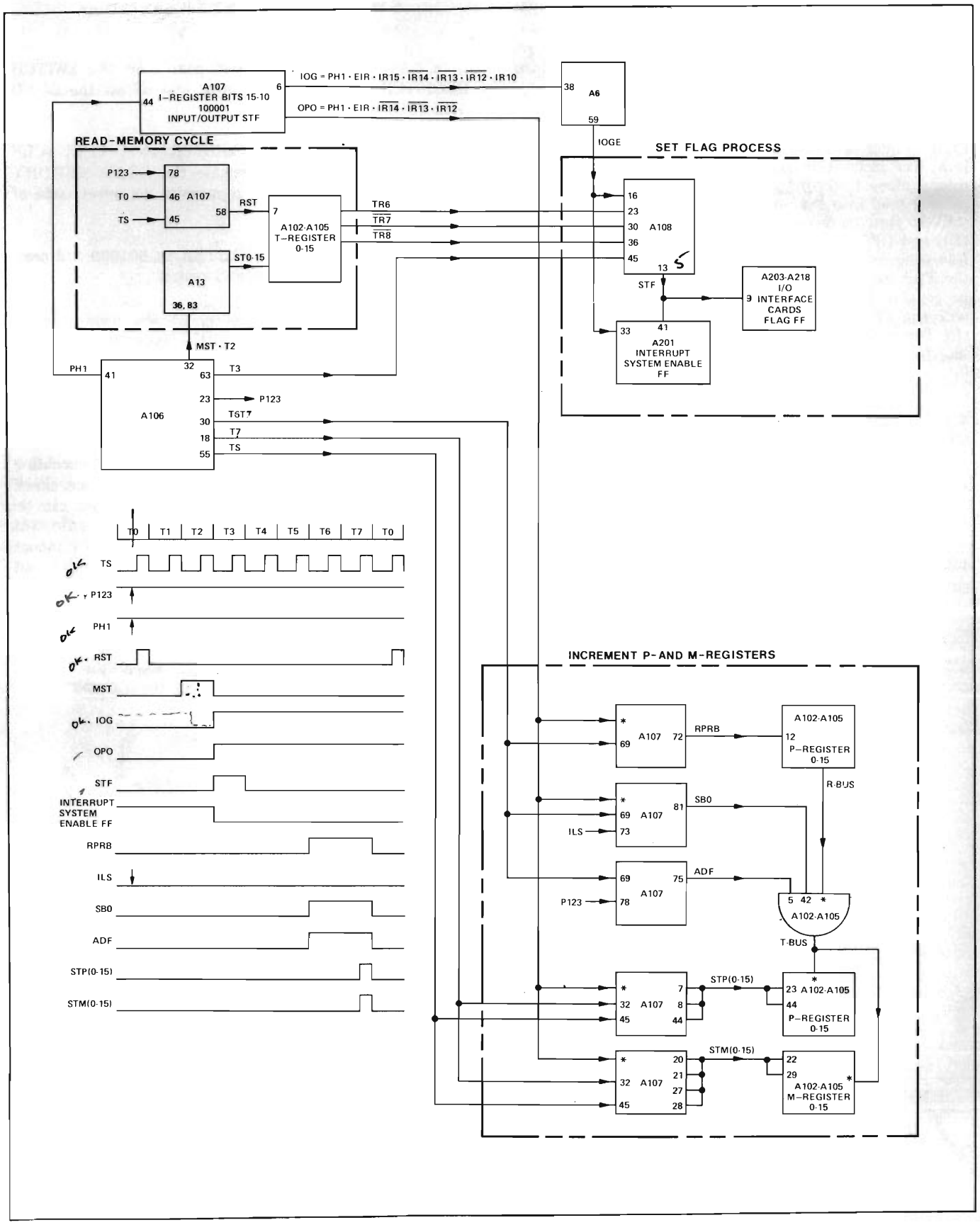
4-402. The computer is now in the run mode executing the STF instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-80. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-44. STF Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR	Set Flag: Select Code			P + 1 to P, M Set next phase	



2107-203

Figure 4-80. STF Instruction Processing Circuits, Servicing Diagram

4-403. CLF INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CLF instruction. Processing operations are summarized in table 4-45. Point-to-point signal flow during phase 1 is shown in figure 4-81.

4-404. Description. The CLF instruction clears the Flag flip-flop addressed in the select code portion of the instruction. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 (bits 15 thru 10 respectively) in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR5, TR4, TR3, TR2, TR1, and TR0 signals from the T-register are used to address the desired computer or interface flip-flop. The CLF signal then clears the flip-flop.

4-405. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-406. Test Procedure. To test the CLF instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1031XX (CLF instruction) and press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

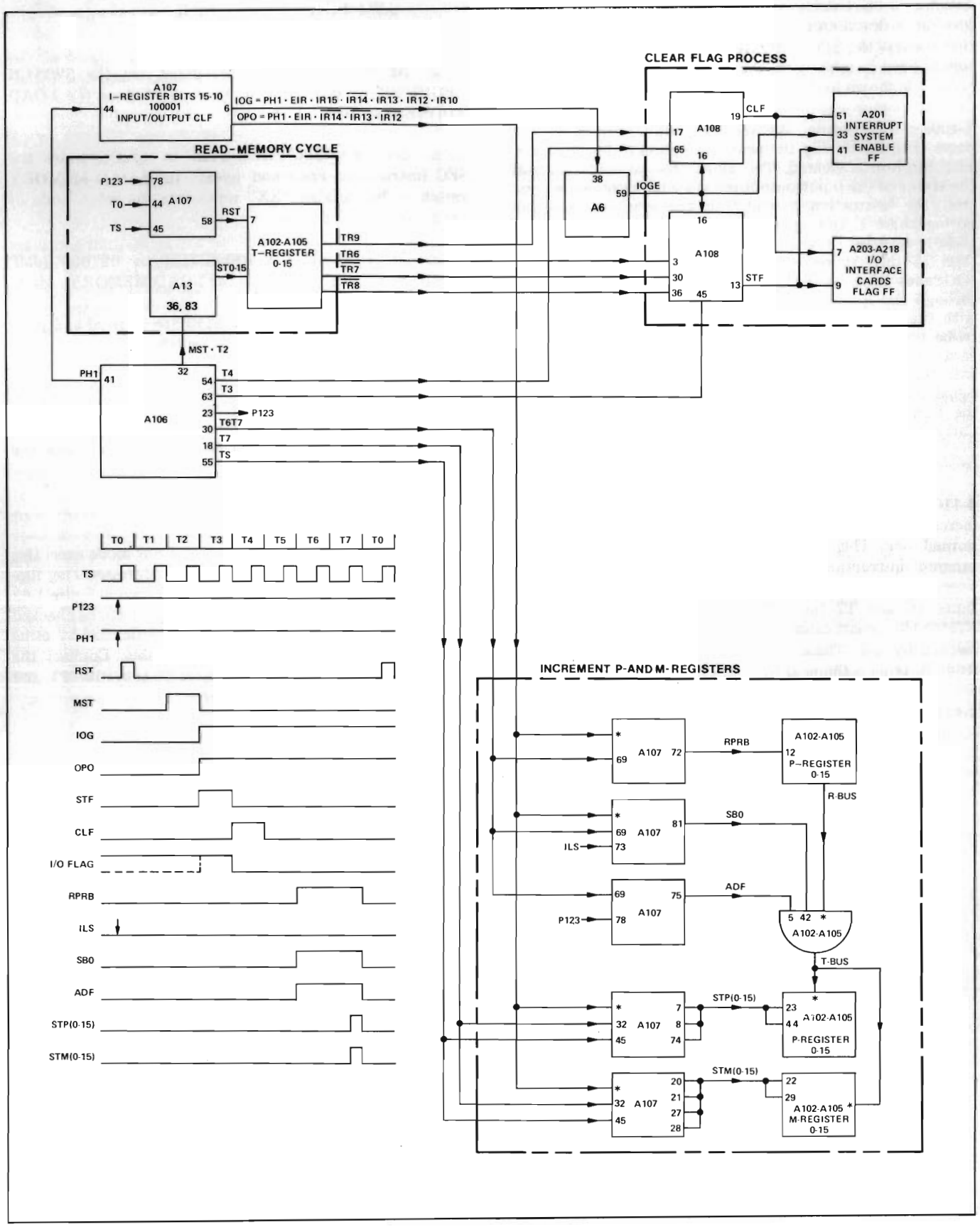
4-407. The computer is now in the run mode executing the CLF instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-81. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-45. CLF Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	TR to IR	Set Flag: Select Code	Clear Flag: Select Code		P + 1 to P, M Set next phase	



2107-204

Figure 4-81. CLF Instruction Processing Circuits, Servicing Diagram

4-408. SFC INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SFC instruction. Processing operations are summarized in table 4-46. Point-to-point signal flow during phase 1 is shown in figure 4-82.

4-409. Description. The SFC instruction causes the computer program to skip the next instruction if the addressed Flag flip-flop is cleared. This allows the computer to test the status of the input/output interface under program control. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 (bits 15 thru 10 respectively) in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. The IOGE signal together with the $\overline{TR8}$, TR7, and $\overline{TR6}$ signals cause the SFC signal to be generated. The SFC signal is routed to the interface cards. The state of the addressed Flag flip-flop is compared with the SFC signal. If the Flag flip-flop is not set, the SKF signal is generated. If the SKF signal is generated it will set the Carry flip-flop at time T4TS. At time T6T7 the set Carry flip-flop will generate the C0 signal.

4-410. The C0 signal is used with the SB0 signal to increment the P- and M-registers by two instead of the normal one. This causes the computer to skip the next program instruction. If the C0 signal is not generated, the normal increment by one operation will occur. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-411. Test Procedure. To test the SFC instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1022XX to test the SFC instruction. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 027000 (JMP instruction). Press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

f. At the computer front panel, press and release the RUN switch.

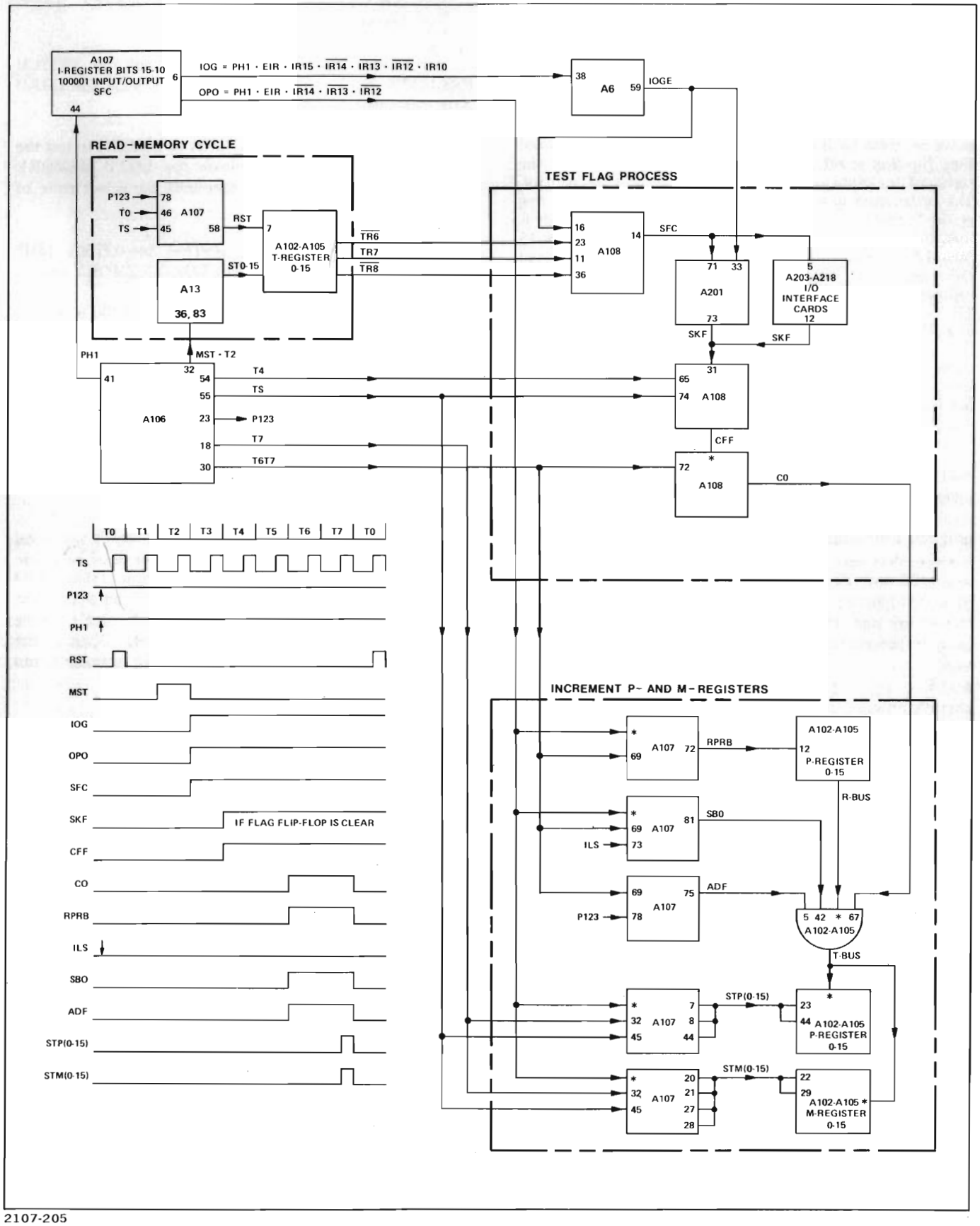
4-412. The computer is now in the run mode executing the SFC instruction. The state of the addressed Flag flip-flop is being tested. Check the signals shown in figure 4-82 using a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-46. SFC Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR	SFC to Interface	SKF sets Carry FF		P + 1 + Carry to P, M Set next phase	



2107-205

Figure 4-82. SFC Instruction Processing Circuits, Servicing Diagram

4-413. SFS INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the SFS instruction. Processing operations are summarized in table 4-47. Point-to-point signal flow during phase 1 is shown in figure 4-83.

4-414. Description. The SFS instruction causes the computer program to skip the next instruction if the addressed Flag flip-flop is set. This allows the computer to test the status of the input/output interface under program control. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 (bits 15 thru 10 respectively) in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. The IOGE signal together with the $\overline{TR8}$, TR7, and TR6 signals cause the SFS signal to be generated. The SFS signal is routed to the interface cards. The state of the addressed Flag flip-flop is compared with the SFS signal. If the Flag flip-flop is set, the SKF signal is generated. If the SKF signal is generated it will set the Carry flip-flop at time T4TS. At time T6T7 the set Carry flip-flop will generate the C0 signal.

4-415. The C0 signal is used with the SB0 signal to increment the P- and M-registers by two instead of the normal one. This causes the computer to skip the next program instruction. If the C0 signal is not generated, the normal increment by one operation will occur. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-416. Test Procedure. To test the SFS instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1023XX to test the SFS instruction. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 027000 (JMP instruction). Press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

f. At the computer front panel, press and release the RUN switch.

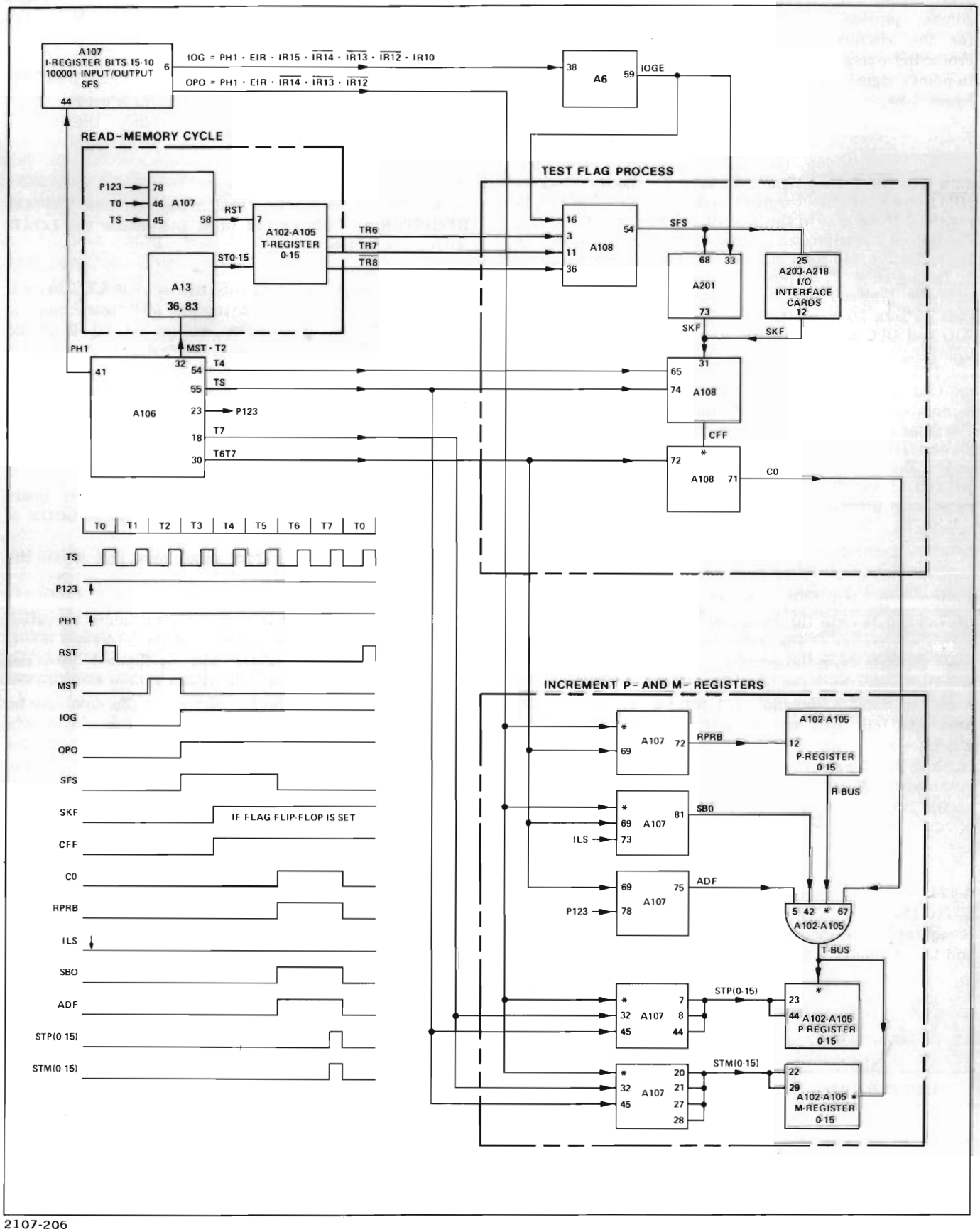
4-417. The computer is now in the run mode executing the SFS instruction. The state of the addressed Flag flip-flop is being tested. Check the signals shown in figure 4-83 using a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-47. SFS Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH	1	Clear TR	Clear IR	IR to IR	SFS to Interface	SKF sets Carry FF		P + 1 + Carry to P, M Set next phase	



2107-206

Figure 4-83. SFS Instruction Processing Circuits, Servicing Diagram

4-418. MIA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the MIA/B instruction. Processing operations are summarized in table 4-48. Point-to-point signal flow during phase 1 is shown in figure 4-84.

4-419. Description. The MIA/B instruction merges input data into the 8 least significant bits of a specified register ($\overline{IR11}$ specifies the A-register and IR11 specifies the B-register). If bit nine of the T-register (TR9) is true, the Flag flip-flop on the addressed interface card will be cleared. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 (bits 15 thru 10 respectively) in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal (if this bit is set) from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR8, and $\overline{TR7}$ signals from the T-register causes the IOI signal to be generated during times T4 and T5. The IOG signal causes the $\overline{IOF}$ signal to be generated during times T4 and T5. The IOG, $\overline{TR6}$, and $\overline{IR11}$/IR11 signals cause the appropriate RARB or RBRB signal to be generated during times T4 and T5.

4-420. The IOI, $\overline{IOF}$, and RARB or RBRB signals route the input data onto the computer bus lines and combine it with the contents of the indicated register. The IOI signal reads the data from the interface card onto the IOBI lines and then onto the S-Bus lines. The RARB or RBRB signal reads the data in the indicated register onto the R-Bus lines. The $\overline{IOF}$ signal combines the data on the R- and S-Bus lines and reads the merged data onto the T-bus lines. At time TS of time T5, the IOG and TR8 and $\overline{TR7}$ signals generate the STBA or STBB signal which stores the data on the T-bus lines into the indicated A- or B-register.

4-421. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-422. Test Procedure. To test the MIA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. Set the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1024XX. This will test the MIA instruction. To test the MIB instruction use 1064XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

4-423. The computer is now in the run mode executing the MIA instruction. The contents of the addressed input/output device data register will be loaded into the A-register. By using select code 01 and keying data into the SWITCH REGISTER, the bit pattern of the data may be easily modified. Check the signals shown in figure 4-84 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-48. MIA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR		Read A/B to R Bus Buffer to S Bus IOF Store T Bus in A/B If TR9 = 1, CLF		P + 1 to P, M Set next phase	

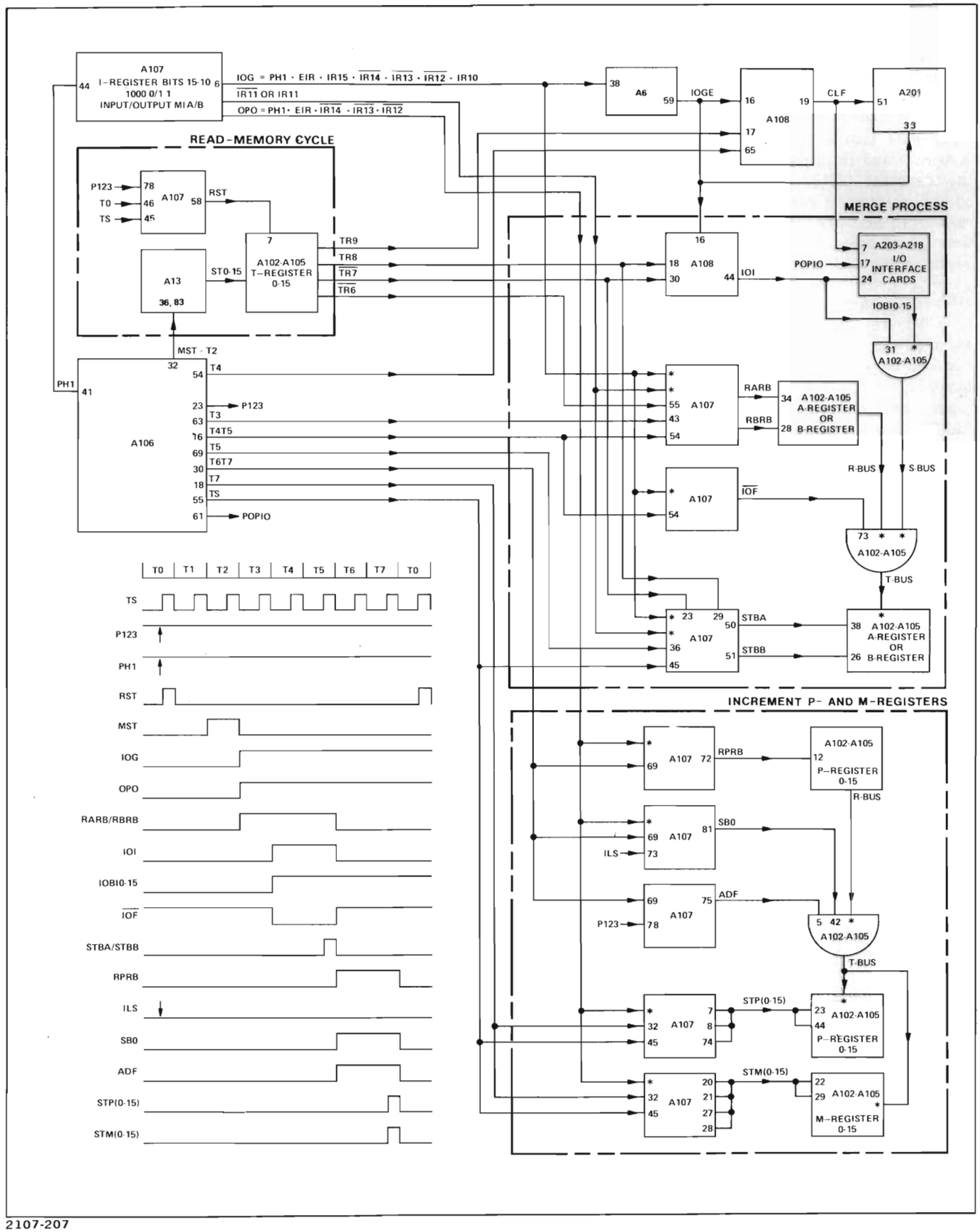


Figure 4-84. MIA/B Instruction Processing Circuits, Servicing Diagram

4-424. LIA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the LIA/B instruction. Processing operations are summarized in table 4-49. Point-to-point signal flow during phase 1 is shown in figure 4-85.

4-425. Description. The LIA/B instruction transfers input data into a specified register ($\overline{IR11}$ specifies the A-register and IR11 specifies the B-register). If bit nine of the T-register (TR9) is true, the Flag flip-flop on the addressed interface card will be cleared. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 (bits 15 thru 10 respectively) in the I-register causes the signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal (if this bit is set) from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR8, and $\overline{TR7}$ signals from the T-register causes the IOI signal to be generated during times T4 and T5. The IOG signal causes the $\overline{IOF}$ signal to be generated during times T4 and T5.

4-426. The IOI, $\overline{IOF}$, and STBA or STBB signals route the input data onto the computer bus lines and store it in the indicated register. The IOI signal reads the data from the interface card onto the IOBI lines and then onto the S-Bus lines. The $\overline{IOF}$ signal transfers the data on the S-Bus lines to the T-Bus lines. At time TS of time T5, the IOG, $\overline{IR11}$ or IR11, TR8 and $\overline{TR7}$ signals generate the STBA or STBB signal which stores the data on the T-Bus lines into the indicated A- or B-register.

4-427. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-428. Test Procedure. To test the LIA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1025XX. This will test the LIA instruction. To test the LIB instruction use 1065XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

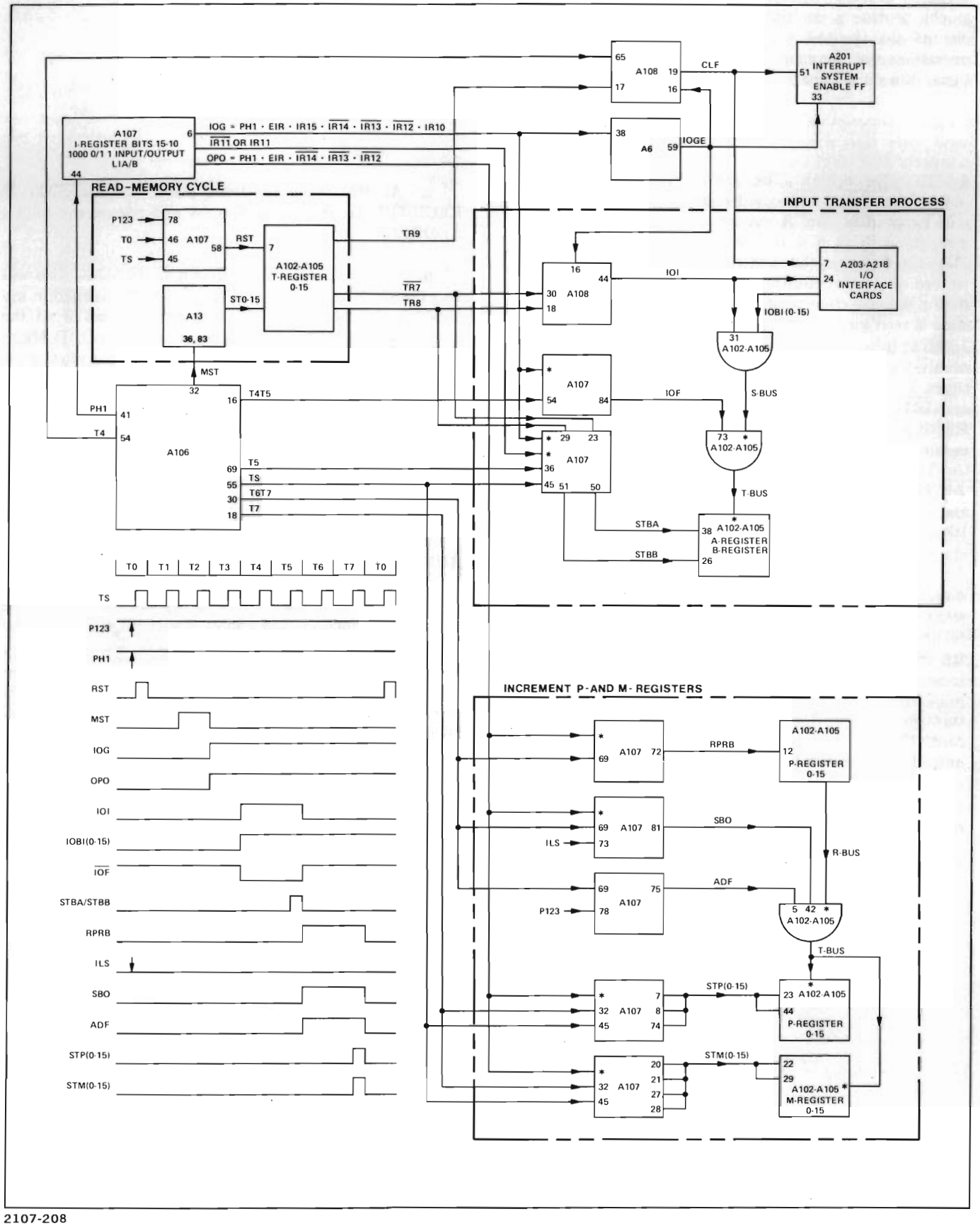
4-429. The computer is now in the run mode executing the LIA instruction. The contents of the addressed input/output device data register will be loaded into the A-register. By using select code 01 and keying data into the SWITCH REGISTER, the bit pattern of the data may be easily modified. Check the signals shown in figure 4-85 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1 and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-49. LIA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR		Buffer to S Bus IOF Store T Bus in A/B If TR9 = 1, CLF		P + 1 to P, M Set next phase	



2107-208

Figure 4-85. LIA/B Instruction Processing Circuits, Servicing Diagram

4-430. OTA/B INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the OTA/B instruction. Processing operations are summarized in table 4-50. Point-to-point signal flow during phase 1 is shown in figure 4-86.

4-431. Description. The OTA/B instruction transfers output data from a specified register to an output device ($\overline{IR11}$ specifies the A-register and IR11 specifies the B-register). If bit nine of the T-register (TR9) is true, the Flag flip-flop on the addressed interface card will be cleared. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 (bits 15 thru 10 respectively) in the I-register causes the signals IOG and OPO to be generated during times T3 through the following time T0. The IOG, $\overline{TR6}$, and $\overline{IR11}$ or IR11 signals cause the appropriate RARB or RBRB signal to be generated at time T3. The IOGE signal in combination with the TR9 signal (if this bit is set) from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the TR8, TR7, and $\overline{TR6}$ signals from the T-register causes the IOO and IOCO signals to be generated during times T4 and T5.

4-432. The RARB or RBRB, IOCO, and IOO signals route the output data onto the computer bus lines and then to the addressed output interface card. The RARB or RBRB signal reads the data from the register onto the R-bus lines. The IOCO signal transfers the data to the IOBO lines. The IOGE signal together with T-register bits TR0 through TR5 provide select code signals to the interface card. The IOO signal transfers the data on the IOBO lines onto the addressed interface card.

4-433. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to be incremented by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-434. Test Procedure. To test the OTA/B instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1026XX. This will test the OTA instruction. To test the OTB instruction use 1066XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

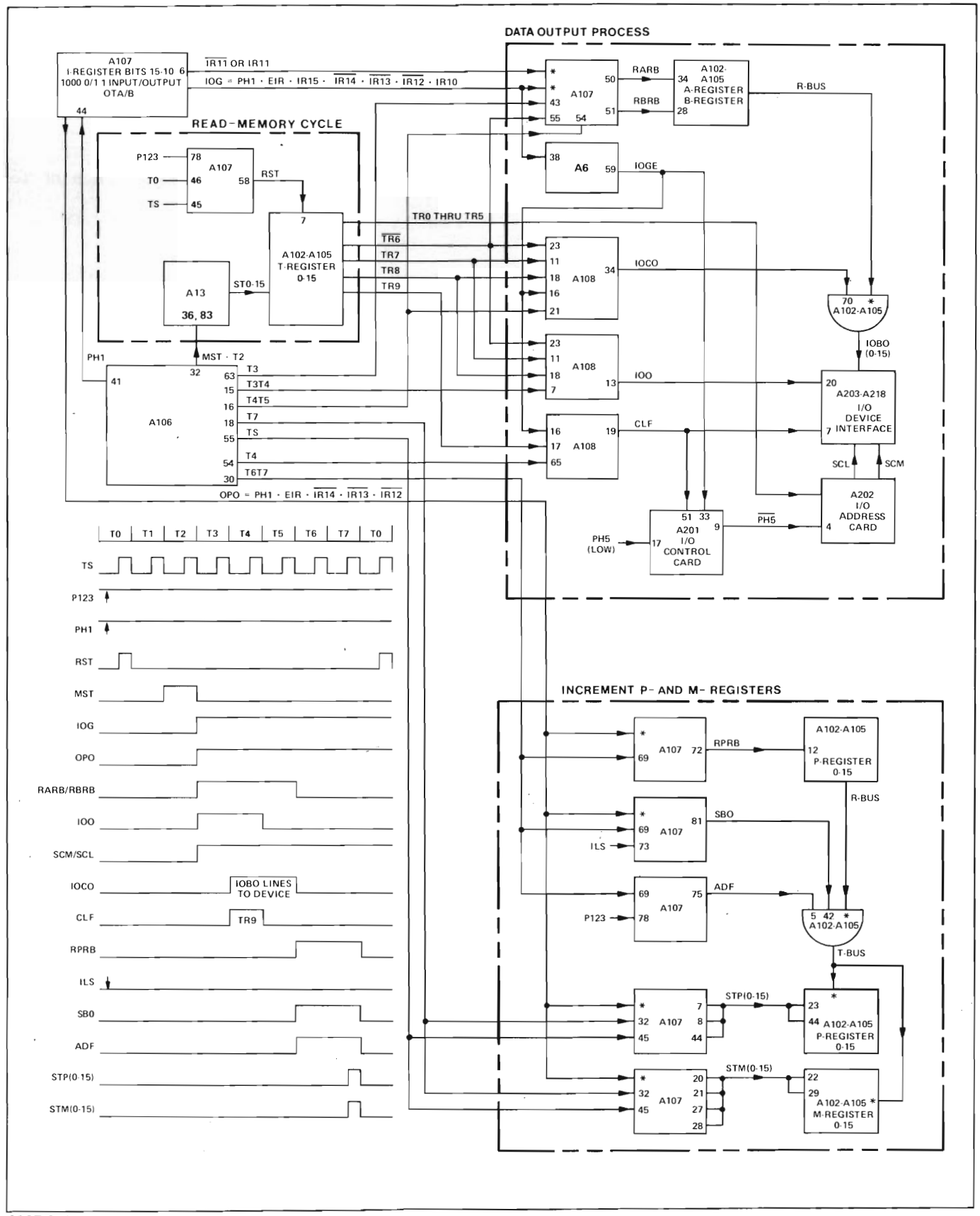
4-435. The computer is now in the run mode executing the OTA instruction. The contents of the A-register will be loaded into the addressed input/output device data register. Check the signals shown in figure 4-86 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-50. OTA/B Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR		Read A/B to R Bus R Bus to Buffer If TR9 = 1, CLF		P + 1 to P, M Set next phase	



2107-209

Figure 4-86. OTA/B Instruction Processing Circuits, Servicing Diagram

4-436. STC/CLC INSTRUCTIONS. The following paragraphs provide a description and test procedure for the circuits that process the STC and CLC instructions. Processing operations are summarized in table 4-51. Point-to-point signal flow during phase 1 is shown in figure 4-87.

4-437. Description. The STC instruction sets the addressed Control flip-flop. The CLC instruction clears the addressed Control flip-flop. The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 or 100011 (bits 15 thru 10 respectively) in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. The IOGE signal together with the $\overline{TR11}$ or TR11, TR8, TR7, and TR6 signals generate the STC or CLC signals. A true TR11 bit will cause the CLC instruction to be generated. A false TR11 bit will cause the STC signal to be generated. If the TR9 bit is true the IOGE signal will cause a CLF signal to be generated at time T4. The STC or CLC signals together with the select code signals cause the Control flip-flop on the addressed interface card to be set or cleared respectively. If the CLF signal has been generated the Flag flip-flop will also be cleared.

4-438. During the T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-439. Test Procedure. To test the STC and CLC instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 1027XX. This will test the STC instruction. To test the CLC instruction, use 1067XX. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch. (The variable "XX" represents the select code of the addressed I/O device.)

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

e. At the computer front panel, press and release the RUN switch.

4-440. The computer is now in the run mode executing the STC (CLC) instruction. The addressed Control flip-flop will be set (cleared). Check the signals shown in figure 4-87 with a dual-trace oscilloscope. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect the oscilloscope channel B input to signal T0 at A106-TP1, and use this as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-51. STC/CLC Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH STC	1	Clear TR	Clear IR	TR to IR	Set Control (Sel. Code			P + 1 to P, M Set next phase	
FETCH CLC	1	Clear TR	Clear IR	TR to IR	Clr. Control (Sel. Code)			P +1 to P, M Set next phase	

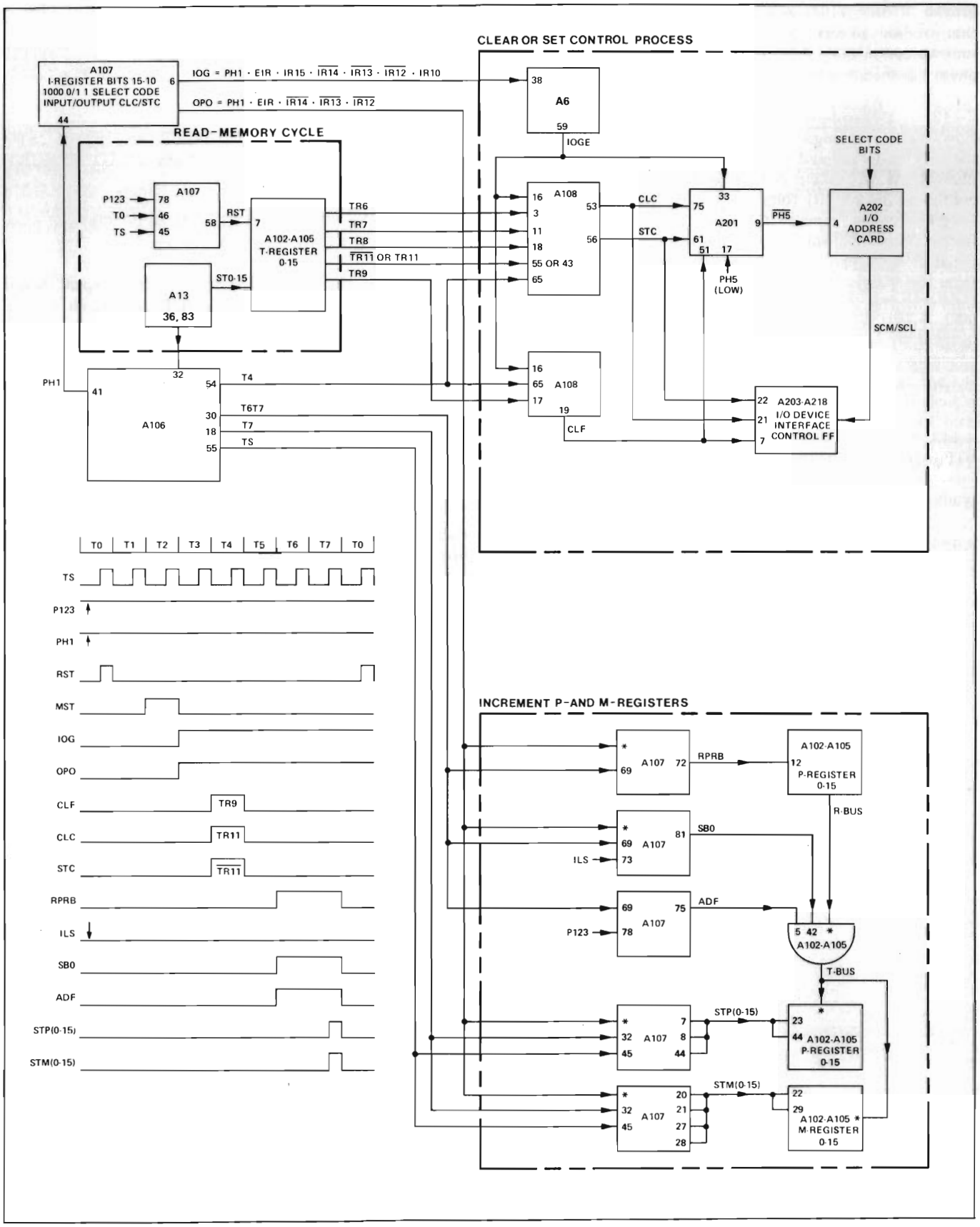


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Figure 4-87. STC/CLC Instruction Processing Circuits, Servicing Diagram

4-441. STO INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the STO instruction. Processing operations are summarized in table 4-52. Point-to-point signal flow during phase 1 is shown in figure 4-88.

4-442. Description. The STO instruction sets the Overflow register (O-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 (bits 15 thru 10 respectively) in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the $\overline{TR8}$, $\overline{TR7}$, and TR6 signals from the T-register cause the STF signal to be generated at time T3. The IOGE signal in combination with the $\overline{TR5}$, $\overline{TR4}$, $\overline{TR3}$, $\overline{TR2}$, $\overline{TR1}$, and TR0 signals from the T-register cause the IOS signal to be generated. At time T3TS the IOS and STF signals set the Overflow register and generate the overflow indication on the front panel.

4-443. During time T6T7 signals RPRB, SBO, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-444. Test Procedure. To test the STO instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 102101 (STO instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

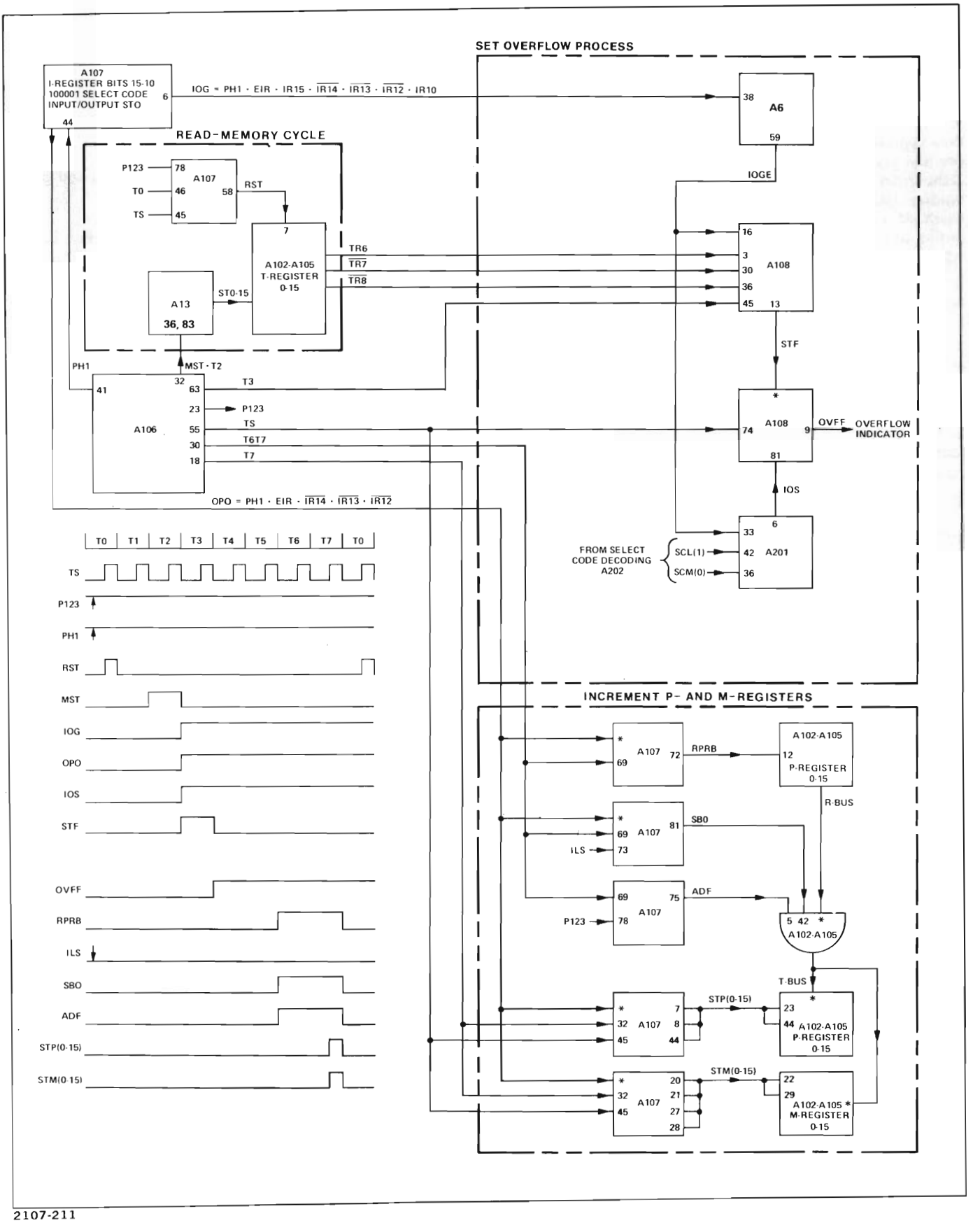
4-445. The computer is now in the run mode executing the STO instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-88. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-52. STO Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR	STF to Overflow FF			P + 1 to P, M Set next phase	



2107-211

Figure 4-88. STO Instruction Processing Circuits, Servicing Diagram

4-446. CLO INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process the CLO instruction. Processing operations are summarized in table 4-53. Point-to-point signal flow during phase 1 is shown in figure 4-89.

4-447. Description. The CLO instruction clears the Overflow register (O-register). The instruction is read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 (bits 15 through 10 respectively) in the I-register causes signals IOG and OPO to be generated during times T3 through the following time T0. The IOGE signal in combination with the TR9 signal from the T-register causes the CLF signal to be generated at time T4. The IOGE signal in combination with the $\overline{TR5}$, $\overline{TR4}$, $\overline{TR3}$, $\overline{TR2}$, $\overline{TR1}$, and TR0 signals from the T-register cause the IOS signal to be generated. At time T4TS the IOS and CLF signals clear the Overflow register and remove the overflow indication on the front panel.

4-448. During time T6T7 signals RPRB, SB0, ADF, STP(0-15), and STM(0-15) cause the P- and M-registers to increment by one. Phase 1 is then set, and the computer is ready to process the next instruction.

4-449. Test Procedure. To test the CLO instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 103101 (CLO instruction) and press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

d. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to the LOOP position.

e. At the computer front panel, press and release the RUN switch.

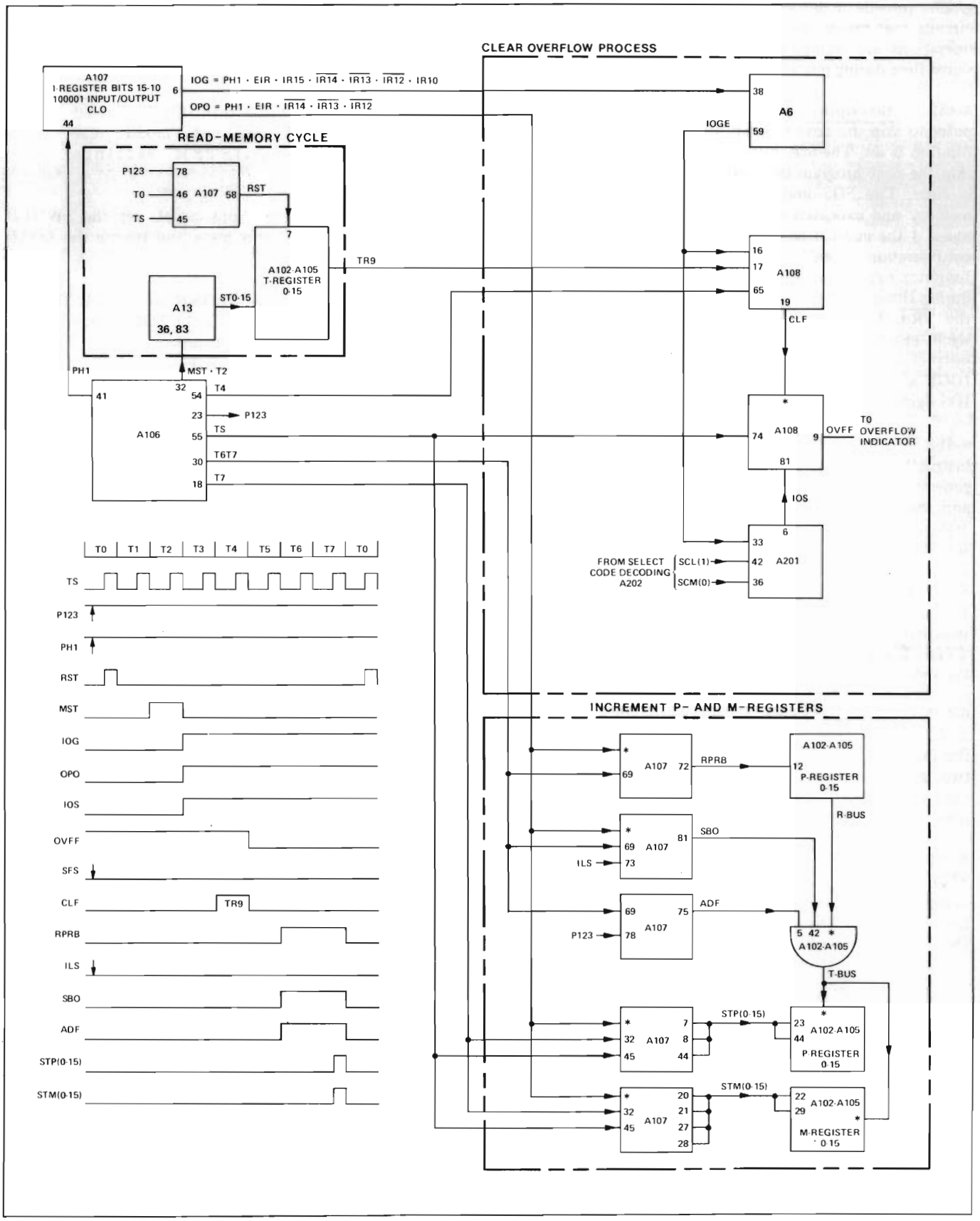
4-450. The computer is now in the run mode executing the CLO instruction. Using a dual-trace oscilloscope, check the signals shown in figure 4-89. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-53. CLO Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH	1	Clear TR	Clear IR	TR to IR		CLF to Overflow FF		P + 1 to P, M Set next phase	



2107-212

Figure 4-89. CLO Instruction Processing Circuits, Servicing Diagram

4-451. SOS/SOC INSTRUCTION. The following paragraphs provide a description and test procedure for the circuits that process SOS and SOC instructions. Processing operations are summarized in table 4-54. Point-to-point signal flow during phase 1 is shown in figure 4-90.

4-452. Description. The SOS instruction causes the computer to skip the next program instruction if the Overflow flip-flop is set. The SOC instruction causes the computer to skip the next program instruction if the Overflow flip-flop is clear. The SOS and SOC instructions are read from memory and executed during phase 1. During time T2 of phase 1 the instruction code is read into the I-register. Bit configuration 100001 (bits 15 thru 10 respectively) in the I-register causes the IOG and OPO signals to be generated during times T3 through the following time T0. At time T3 the $\overline{TR8}$, TR7, and TR6 signals together with the IOGE signal generate the SFS signal. If TR6 is false for the SOC instruction, the SFC signal will be generated instead. The IOGE signal together with the select code bits cause the IOS signal to be generated.

4-453. If the Overflow flip-flop is set and the SOS instruction is being executed, the SFS and IOS signals will generate the SKF signal. If the Overflow flip-flop is clear and the SOC instruction is being executed, the SFC and IOS signals will generate the SKF signal. If TR9 has been set, the CLF signal will be generated at time T4. The CLF signal will clear the Interrupt Control flip-flop on the I/O Control card. This prevents I/O interrupts during normal CLF instructions and is coincidental to the SOS and SOC instructions. The Interrupt Control flip-flop is set during T7TS. The CLF signal together with the IOS signal cause the Overflow flip-flop to be cleared at time T4TS.

4-454. The SKF signal sets the Carry flip-flop at time T4TS. During times T6 and T7 the output of the Carry flip-flop, C0, is used to increment the P- and M-registers by two instead of one. This causes the computer to skip the next program instruction. The Carry flip-flop is cleared at time T0 of the following machine cycle.

4-455. During times T6 and T7 the RPRB, SB0, ADF, STP(0-15), and STM(0-15) signals cause the P- and M-registers to increment by one if an SKF signal has not been generated. The next phase (phase 1) is then set, and the computer is ready to process the next instruction.

4-456. Test Procedure. To test the SOS and SOC instruction circuits, proceed as follows:

Note

If an address other than 001000 is used for the following test, modify the SWITCH REGISTER settings accordingly.

a. At the computer front panel, set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

b. Set the SWITCH REGISTER to 102301. This will test the SOS instruction. To test the SOC instruction, use 102201. To test the CLF operation set bit 9 of the SWITCH REGISTER. Press and release the LOAD MEMORY switch.

c. Set the SWITCH REGISTER to 027000 (JMP instruction). Press and release the LOAD MEMORY switch.

d. Set the SWITCH REGISTER to 001000 and press and release the LOAD ADDRESS switch.

e. Open the door assembly. At the display board assembly A501, set the INSTRUCTION switch to LOOP.

f. At the computer front panel, press and release the RUN switch.

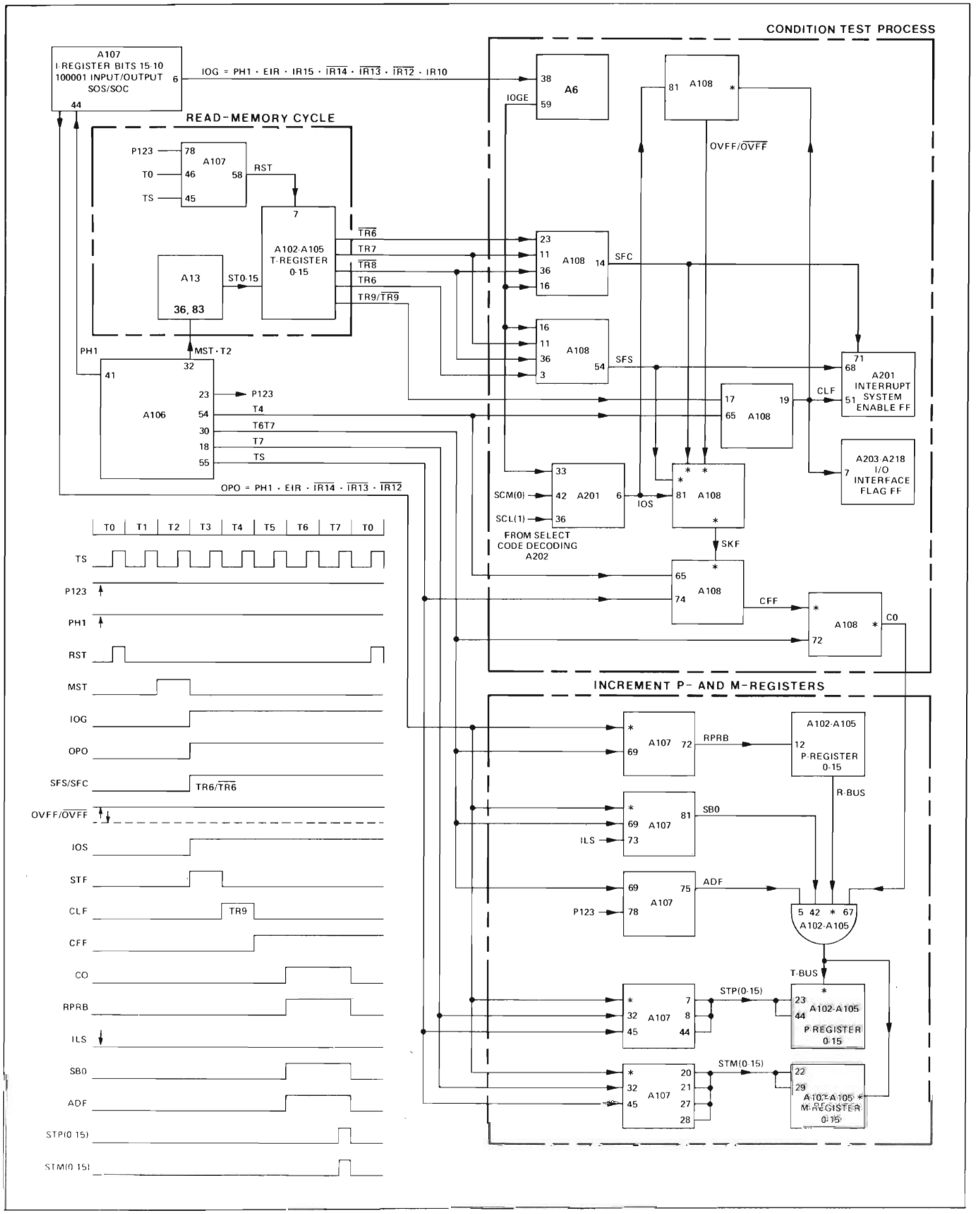
4-457. The computer is now in the run mode executing the SOS (SOC) instruction. Using a dual-trace oscilloscope check the state of the signals shown in figure 4-90. These signals can be checked at the backplane connectors, or at a specific card by using the extender card and the extender cable. Connect oscilloscope channel B input to signal T0 at A106-TP1, and use channel B as the triggering source.

Note

Signal SB0 is inhibited when the INSTRUCTION switch is in the LOOP position.

Table 4-54. SOS/SOC Instruction Processing Operations

TIME PERIODS		T0	T1	T2	T3	T4	T5	T6	T7
PHASE			READ (Mem to TR)			WRITE (TR to Mem)			
FETCH SOS	1	Clear TR	Clear IR	TR to IR OVF	SFS to OVF	SKF to Carry FF		P + 1 + Carry to P, M Set next phase	
FETCH SOC		Clear TR	Clear IR	TR to IR	SFC to OVF	SKF to Carry FF		P +1 +Carry to P, M Set next phase	



2107-213

Figure 4-90. SOS/SOC Instruction Processing Circuits, Servicing Diagram

4-458. MEMORY SECTION TROUBLESHOOTING.

4-459. GENERAL.

4-460. The core memory in the computer is of three-wire design, with an X-drive line, Y-drive line, and inhibit-sense line strung through each core. A current reversing capability for the X-drive line permits two 4K (4,096 word) modules to share common lines and operate in tandem as a single 8K (8,192 word) core stack. The computer mainframe can contain from one to four core stacks, with memory capacity increased in 8K increments for each stack installed, up to a maximum of 32K (32,768 words). The first 8K increment is furnished as part of the basic computer. The second, third, and fourth increments are optional (factory installed as options 005, 006, and 007, respectively; field installed using the 12615A Accessory Kit). For additional information concerning memory options, refer to the 12615A Installation Manual (part no. 12615-90001).

4-461. Figure 3-1 is an overall block diagram of the computer, including the memory section. When a word is to be read from memory, the address is placed in the M-register. The address is decoded by the address decoding gates on the memory address decoder and X-Y driver/switch cards, which select the appropriate driver and switch circuits. Current flows from the driver to the switch, or vice versa, and the cores of the selected word are set to the zero state. For each core that contained logic 1, a sense amplifier detects an output from the core. The sense amplifier sets the corresponding position of the T-register to logic 1 via the memory data buffer. Since the T-register is cleared before the word is read out, the register contents become the same as the word read from memory. The word read out must then be restored in the memory location from which it was acquired. To do this, the memory section attempts to store logic 1 in every bit position of the word. However, the inhibit driver for each bit of the word senses the corresponding bit in the T-register, and if the bit is logic 0 the inhibit driver prevents the writing of logic 1 in the appropriate bit position of the selected word location in memory. By this means the word read from memory is restored in the original location.

4-462. The operation described above is also performed when placing a new word into a memory location, except that the word read out of memory is not stored in the T-register. Instead, the new word is placed in the T-register via the IOBI lines. The new word is then stored in memory rather than the original word. (Refer to paragraph 3-59 for a more detailed account of memory operation). When troubleshooting the memory section, it is necessary to determine which of the following types of faults exist:

a. Addressing fault.
b. Read fault.
c. Write fault.

4-463. The type of fault can be determined from the symptoms observed, from running the diagnostic programs, and by using panel controls to store and read test words. A small test program can be used (refer to paragraph 4-464) as a further means of determining the type of fault. During these test operations, oscilloscope examination of waveforms will serve as an aid in determining the type of fault. It should be noted that when an addressing fault exists, it affects both read and write operations. Therefore, if a word is written in a given location and then read back, operation may appear normal because the word will have been written in and read from the wrong location.

4-464. MEMORY TEST PROGRAM.

4-465. Storing a known bit pattern throughout core memory, or loading a known bit pattern into the A-register from core memory, can aid in determining if a problem is the result of a faulty core memory assembly. A simple method of doing this is described below. Since signal MST is inhibited during a "store" operation, the "load" operation must be performed when testing the signals that occur after signal MST. The procedure described below either stores (STA) or loads (LDA) any desired 16-bit word (bit pattern) throughout core memory (except in the protected area of memory containing the loader program) or the A-register, depending upon the test instruction used. The following procedure establishes an instructional loop to permit oscilloscope examination of signal waveforms.

Note

Do not omit step "a" below, otherwise data in the protected area of memory may be destroyed.

a. Make sure the LOADER switch is in the PROTECTED position.

b. Press and release the PRESET switch.

c. Set all SWITCH REGISTER switches to logic 0 (down) position.

d. Press and release the LOAD ADDRESS switch.

e. Set the SWITCH REGISTER switches to 070000 (STA instruction) or 060000 (LDA instruction).

f. Press and release the LOAD A switch.

g. Press and release the SINGLE CYCLE switch.

h. Set the PHASE switch to the LOOP position.

i. Set into the SWITCH REGISTER switches the desired 16-bit test word which is to be stored (usually all "ones" or all "zeros").

j. Press and release the LOAD A switch.

k. Press and release the RUN switch.

4-466. The test word will continue to be stored (written) throughout memory, or loaded into the A-register from memory, until the HALT switch is pressed. To change the test word, press and release the HALT switch and repeat steps "i" and "j", of the above procedure.

4-467. REFERENCES.

4-468. When troubleshooting the memory section, refer to Section III for an overall block diagram discussion (paragraph 3-59) and detailed theory (paragraph 3-86). Refer to Section VII for detailed diagrams, signal lists, and backplane wiring information.

4-469. Tables 4-55 through 4-59 and figures 4-91 through 4-99 support the descriptions and test procedures presented in this section of the manual. Table 4-55 is a troubleshooting guide for addressing problems. It shows the function of each M-register bit in the addressing scheme, lists the location of the circuit card that controls a specific segment of memory, and lists the circuits and control signals activated for specific addresses and modes (i.e., memory read cycle or memory write cycle). Table 4-56 lists sense amplifier control signals and test points where the signals can be tested. Table 4-57 is similar to table 4-56 in that it lists the control signals and test points for the inhibit driver circuits. Table 4-58 lists the data signals for all 16 data bits (from sense amplifier circuit output to inhibit driver circuit output) including the backplane connector pins where the signal can be tested and the gating (control) signals that allow the data signals to pass from one circuit to another. Figure 4-91 is a block diagram of the memory section showing signal flow within specific functions of memory (i.e., addressing, sensing, inhibiting). This diagram will serve as an aid in understanding the overall operation of the memory section. Figures 4-92 through 4-99 are examples of normal waveforms found at these test points. These figures and tables will be found useful when troubleshooting the memory section. The test procedure in paragraph 4-477 will also aid in the memory troubleshooting process.

4-470. ADDRESSING CIRCUITS.

4-471. DESCRIPTION. The selection of a particular word location in the core stack assembly is a function of the following cards:

a. Timing generator card A106.
b. Arithmetic logic cards A102, A103, A104, and A105.
c. Memory address decoder card A14.
d. X-Y driver/switch cards A8, A11, A18, and A21.

Note

Cards A8, A11, and A18 are not installed when only a single 8K core stack assembly is used.

4-472. Timing Generator Card. The timing generator card produces timing and control signals (MRT1, MRT2, MIT, MWT1, MWT2, MSG, and MST) for the memory section. Refer to paragraph 4-156 for complete memory timing information.

4-473. Arithmetic Logic Cards. The arithmetic logic cards contain the M-register. The M-register holds the address bits for the location in memory in which reading or writing will take place. (Other registers and circuits are also located on these cards, but they do not affect memory addressing.)

4-474. Memory Address Decoder Card. The memory address decoder card decodes the memory address bits (signals MR0 through MR14 from the M-register) to access the core stack and module in which the addressed location is situated. This card generates signals MOD0 through MOD7 and M0 through M11, which along with memory timing signals MRT1, MRT2, XT1, XT2, and MIT, cause the appropriate X-Y driver/switch circuits to be energized.

4-475. The memory address decoder card also has decoding circuits which determine if a location within the upper 77 (octal) locations of memory (loader area) is being addressed. If one of these protected locations is addressed, and signal LPS is true (LOADER switch is in the PROTECTED position), signal MPT is generated which, if the parity error option is installed, causes the computer to halt. A true MPT signal also causes decoder circuit U106 to be cleared and the memory read and write process to be inhibited by blocking the decoding networks on the X-Y driver/switch, sense amplifier, and inhibit driver cards. The memory address decoder card also contains buffer circuits for logic signals which are used at the arithmetic logic cards to process data. Refer to Section III for complete memory address decoder circuit information.

4-476. X-Y Driver/Switch Cards. The X-Y driver/switch cards decode the memory address bits M0 through M11 and signals MOD0/1 through MOD6/7. When decoded, these signals, along with the timing signals MRT1, MIT, XT1, and XT2, select the proper driver/switch circuits. The driver switch circuits provide X and Y drive-line currents in the proper direction at the proper time to read data from the selected memory location. The same process is used to write data back into the selected location. Refer to Section III for detailed driver/switch circuit information.

4-477. TEST PROCEDURE. The following general-purpose procedure may be used to troubleshoot a memory addressing problem.

a. Using the method described in paragraph 4-465, load all locations in memory (except the protected area) with logic 1's.

b. Press and release the HALT switch.

c. Set all SWITCH REGISTER switches to logic 0 (down) position.

d. Press and release the LOAD ADDRESS switch.

e. Press and release the DISPLAY MEMORY switch. The T-register should have logic 1's in all bit positions (177777).

f. Continue to press and release the DISPLAY MEMORY switch, making a note of all locations that do not contain logic 1's in all bit positions. A pattern of failing locations will be seen. If not, repeat the above procedure, loading all locations in memory with logic 0's.

g. When a pattern of failing locations has been established, compare it with the information given in table 4-55 and troubleshoot the faulty circuit card.

h. Repeat the above procedure to be certain no other problems exist.

Note

Memory address decoder card A14 provides the control signals (MOD0/1 thru MOD6/7) that turn the X-Y driver/switch circuits on and off for an entire 8K stack. Card A14 may be the cause of trouble if entire stack appears to be failing.

4-478. READ AND WRITE CIRCUITS.

4-479. DESCRIPTION. The read and write circuits control data bits as they are stored in, and removed from, the addressed core memory location. These functions are performed by the following circuits cards:

a. Timing generator card A106.

b. Memory data buffer card A13.

c. Sense amplifier cards A9, A10, A19, and A20. (Cards A9, A10, and A19 are not installed if only a single 8K core stack assembly is used.)

d. Arithmetic logic cards A102, A103, A104, and A105.

e. Inhibit driver cards A7, A12, A17, and A22. (Cards A7, A12, and A17 are not installed when only a single 8K core stack is used.)

4-480. Timing Generator Card. The timing generator card produces timing and control signals for the memory section. Refer to paragraph 4-156 for complete memory timing information.

4-481. Memory Data Buffer Card and Sense Amplifier Cards. The circuits on these cards transfer data from the addressed memory location to the T-register on the arithmetic logic cards. The sense amplifier cards each contain an 8K core stack assembly and 17 amplifier circuits which sense and amplify the pulses from the 17 ferrite cores of the addressed memory location. A pulse is produced when a core storing a logic 1 is switched to the logic 0 state during memory read time. The seventeenth sense amplifier on each card is used only when the parity error option is installed in the computer. The memory data buffer card provides circuits for amplifying and gating the 17 data bits from the sense amplifier cards. The memory data buffer card also contains a switch controlled signal generator circuit which can be used for test purposes. The switch controls the state of the MITX output line. The four switch positions and their functions are as follows:

a. The NORM position disconnects the test generator from the MITX output line during normal operation.

b. The ONES position causes logic 1 to be written in all cores of the addressed memory location, except parity.

c. The CB position causes patterns of ones and zeros to be written into alternate blocks of 77_8 memory locations. In all blocks having addresses with an "even" third digit (i.e., 023400 through 023477), zeros are written in the first 37_8 locations (023400 through 023437). Ones are written into all other locations of the block (023400 through 023477), and all blocks having addresses with an "odd" third digit (i.e., 023500 through 023577).

d. The $\overline{CB}$ position reverses the pattern described in step "c" above.

4-482. Arithmetic Logic Cards. The arithmetic logic cards contain the T-register, which receives the word read from core memory via the sense amplifiers and the memory data buffer circuits. The T-register also provides the word to be written into memory via the inhibit driver circuits.

4-483. Inhibit Driver Cards. The inhibit driver cards each contain 17 inhibit driver circuits which sense the bit-positions of the T-register. For each bit-position containing logic 0, an inhibit driver circuit is turned on by the MIT (memory inhibit time) pulse to prevent the writing of logic 1 in the corresponding bit position of the addressed memory location during memory write time. One of the 17 inhibit driver circuits is used only when the parity error option is installed in the computer. One inhibit driver card is used for each core stack assembly. Refer to Section III for detailed inhibit driver information.

4-484. TEST PROCEDURE. Troubleshooting the memory read and write circuits can be accomplished by exchanging circuit cards. After determining which core stack is associated with the failure, the circuit cards associated with that core stack can be exchanged, one card at a time, with the circuit cards associated with another core stack (if the computer has a memory configuration greater than 8K, or spare circuit cards if available). Each time a circuit card is exchanged, a test of the failing core stack locations must be made to see if the trouble indication still exists, or has moved to the core stack locations with which the card was exchanged. If the trouble indication moves or disappears, it can be presumed that the circuit card originally in the card position was faulty. Troubleshooting the memory read and write circuits can also be accomplished

Table 4-55. X-Y Driver Switch Circuit Functions

					M-REGISTER BITS											
					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					NOT USED	CORE STACK		UPPER OR LOWER MODULE	Y-DRIVE LINE SELECTION						X-DRIVE LINE SELECTION					
									MSD				LSD		MSD			LSD		
CARD	MODULE	ADDRESSES	MODES	TIMING SIGNALS	CONTROL SIGNAL				DECODER		DRIVERS		DECODER		DRIVERS		DECODER		DRIVERS	
A21	4K	000000 THRU 007777	READ	XT1, MRT1	MOD0/1				U24		U9, U11, U13, U15		U22		U2, U4, U14, U16		U18		U1, U3, U5, U7	
			WRITE	XT2, MIT	MOD0/1				U23		U9, U11, U13, U15		U21		U2, U4 U14, U16		U17		U1, U3, U5, U7	
	8K	010000 THRU 017777	READ	XT2, MRT1	MOD0/1				U24		U9, U11, U13, U15		U22		U2, U4 U14, U16		U17		U1, U3, U5, U7	
			WRITE	XT1, MIT	MOD0/1				U23		U9, U11, U13, U15		U21		U2, U4, U14, U16		U18		U1, U3, U5, U7	
A18	12K	020000 THRU 027777	SAME AS ABOVE	SAME AS ABOVE	MOD2/3				SAME AS ABOVE											
	16K	030000 THRU 037777																		
A11	20K	040000 THRU 047777	SAME AS ABOVE	SAME AS ABOVE	MOD4/5				SAME AS ABOVE											
	24K	050000 THRU 057777																		
A8	28K	060000 THRU 067777	SAME AS ABOVE	SAME AS ABOVE	MOD6/7				SAME AS ABOVE											
	32K	070000 THRU 077777																		

Table 4-56. Sense Amplifier Control Signals

MEMORY ADDRESS	CARD LOCATION	CONTROL SIGNALS	TEST PINS
000000 thru 017777	A20	MOD 0	3
		MOD 1	4
020000 thru 037777	A19	MOD 2	3
		MOD 3	4
040000 thru 057777	A10	MOD 4	3
		MOD 5	4
060000 thru 077777	A9	MOD 6	3
		MOD 7	4

Table 4-57. Inhibit Driver Control Signals

MEMORY ADDRESS	CARD LOCATION	CONTROL SIGNALS	TEST PINS
000000 thru 017777	A22	MOD 0	6
		MOD 1	12
020000 thru 037777	A17	MOD 2	6
		MOD 3	12
040000 thru 057777	A12	MOD 4	6
		MOD 5	12
060000 thru 077777	A7	MOD 6	6
		MOD 7	12

Table 4-58. Data Signal Test Points

CIRCUIT CARDS	GATING SIGNALS AND TEST POINTS (NOTE 1)	DATA SIGNALS AND TEST POINTS (NOTE 1)																
SENSE AMPLIFIER CARD A9, A10, A19 OR A20	MSG PIN 6	SA OUTPUT SIGNAL:	SA16	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
		SA OUTPUT PIN:	72	71	70	69	68	67	66	65	64	63	21	22	19	20	17	18	15
MEMORY DATA BUFFER CARD A13	MST PINS 38 AND 63	SA INPUT PIN:	71	67	63	59	55	51	45	41	35	31	27	23	19	15	11	7	3
		ST OUTPUT SIGNAL:	ST16	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
		ST OUTPUT PIN:	73	69	65	61	57	53	49	43	37	33	29	25	21	17	13	9	5
ARITHMETIC LOGIC CARDS A102 THRU A105 AND PARITY ERROR CARD A15 (NOTE 2)	NONE		A15	A102				A103				A104				A105			
		ST INPUT PIN:	60	11	52	4	49	11	52	4	49	11	52	4	49	11	52	4	49
		$\overline{\text{TR}}$ OUTPUT SIGNAL:	$\overline{\text{TR16}}$	$\overline{\text{TR15}}$	$\overline{\text{TR14}}$	$\overline{\text{TR13}}$	$\overline{\text{TR12}}$	$\overline{\text{TR11}}$	$\overline{\text{TR10}}$	$\overline{\text{TR9}}$	$\overline{\text{TR8}}$	$\overline{\text{TR7}}$	$\overline{\text{TR6}}$	$\overline{\text{TR5}}$	$\overline{\text{TR4}}$	$\overline{\text{TR3}}$	$\overline{\text{TR2}}$	$\overline{\text{TR1}}$	$\overline{\text{TR0}}$
		$\overline{\text{TR}}$ OUTPUT PIN:	53	15	53	10	54	15	53	10	54	15	53	10	54	15	53	10	54
INHIBIT DRIVER CARD A7, A12, A17, OR A22	MITX PIN 4 (NOTE 3)	$\overline{\text{TR}}$ INPUT PIN:	7	9	82	84	78	80	74	76	75	73	79	77	81	83	13	11	5
		ID OUTPUT SIGNAL:	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		IDXXM1,3,5, OR 7 OUTPUT PIN:	62	60	58	56	54	52	50	46	44	42	38	36	34	32	30	28	26
		IDXXM0,2,4, OR 6:	61	59	57	55	53	51	49	45	43	41	37	35	33	31	29	27	25

NOTES:

1. ALL TEST POINTS (PINS) ARE ON THE CIRCUIT CARD 86-PIN CONNECTOR OR ASSOCIATED BACKPLANE CONNECTOR.
2. SIGNALS AND TEST POINTS FOR DATA BIT 16 DO NOT APPLY UNLESS THE OPTIONAL PARITY ERROR CIRCUIT CARD IS INSTALLED.
3. THE TEST SWITCH ON MEMORY DATA BUFFER CARD A13 MUST BE IN THE NORM POSITION.

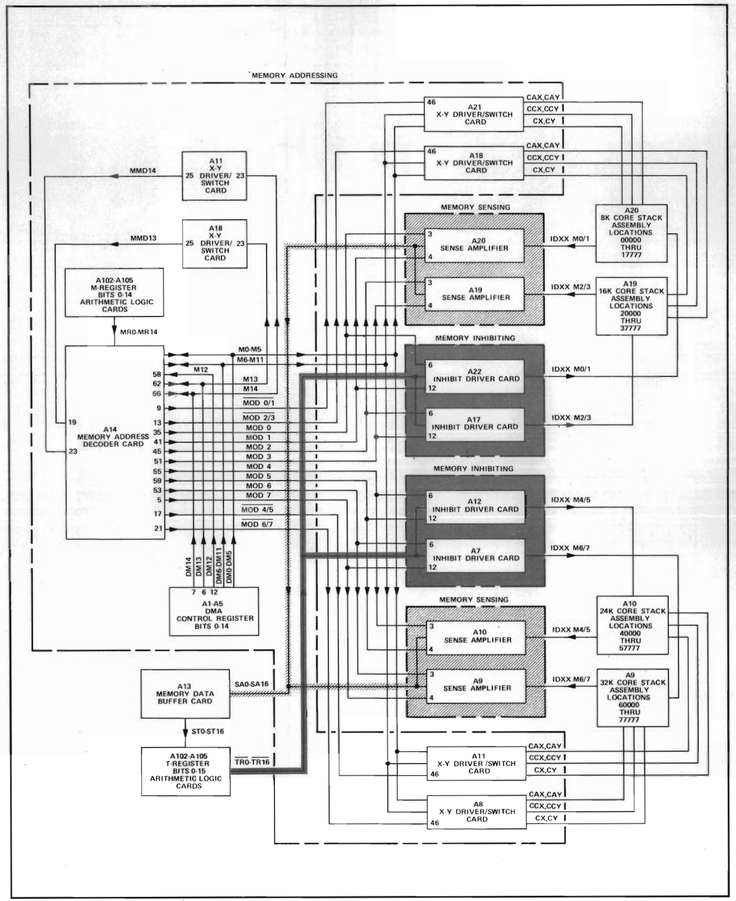
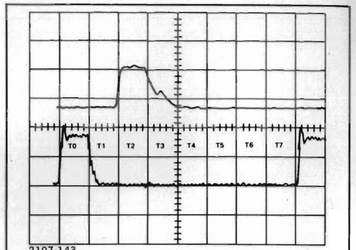


Figure 4-91. Memory Section, Servicing Diagram



2107-143

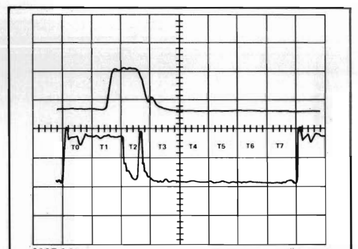
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (SA0):
Input . . . . . A20-15 or A13-3
Volts/cm . . . . . .0.5 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-92. Signal SA0 and Time T0 Waveforms



2107-144

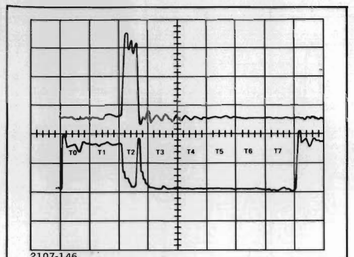
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (SA0):
Input A20-15
Volts/cm . . . . . .0.5 (if using 10:1 probe)

Channel B (MSG):
Input A20-6
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-93. Signals SA0 and MSG Waveforms



2107-146

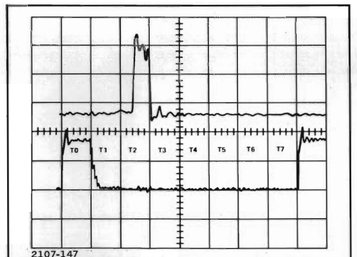
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (ST0):
Input A13-5
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (MSG):
Input A20-6
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-94. Signals ST0 and MSG Waveforms



2107-147

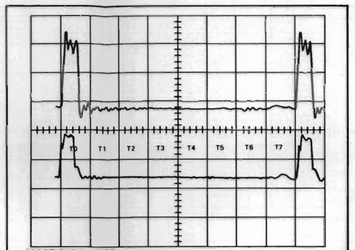
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (ST0):
Input . . . . . A13-5 or A105-49
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-95. Signal ST0 and Time T0 Waveforms



2107-148

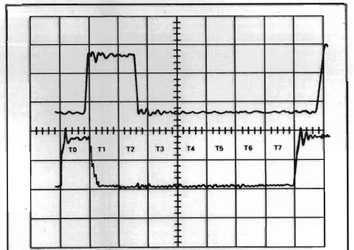
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (ST0):
Input A13-5
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (MST):
Input A13-83
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-96. Signals ST0 and MST Waveforms



2107-150

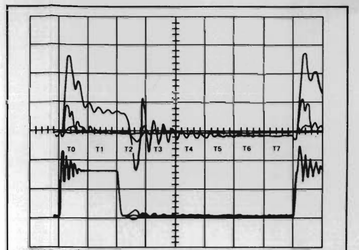
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A ($\overline{TR0}$):
Input A105-54
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-97. Signal TR0 and Time T0 Waveforms



2107-152

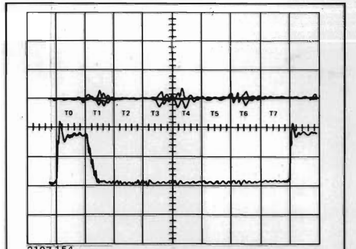
OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (ID0):
Input A22-25
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Channel B (MITX):
Input A22-4
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-98. Signals ID0 and MITX Waveforms (With Zeros in Memory)



2107-154

OSCILLOSCOPE CONNECTIONS & SETTINGS

Channel A (ID0):
Input . . . . . A22-26 or A22-25
Volts/cm . . . . . 0.2 (if using 10:1 probe)

Channel B (T0):
Input A106TP1
Volts/cm . . . . . .0.2 (if using 10:1 probe)

Time/cm . . . . . 0.2 us

Figure 4-99. Signal ID0 and Time T0 Waveforms (With Ones in Memory)

UNFOLD FOR FIGURES 4-92 THRU 4-99

by observing signal waveforms produced by the memory circuits. The following procedure may be used:

a. Using the method described in paragraph 4-465, load all locations into memory (except the protected area) with logic 1's.

b. With an oscilloscope, examine the input and outputs of the circuits affecting the failing bit position or positions (see table 4-58) and compare these signals with the waveforms shown in figures 4-92 through 4-99. If these signals do not come within reasonable tolerances of comparison (see figure 7-1 and table 7-1 for integrated circuit tolerances), the most probable cause of trouble is in the output circuit of the signal currently being examined.

4-485. INPUT/OUTPUT SECTION TROUBLESHOOTING.

4-486. When troubleshooting the I/O section, it is first necessary to determine whether the fault is in the I/O device, the I/O interface card, the I/O address card, or the I/O control card. Other sections of the computer must also be eliminated as the source of trouble. The following procedure is used:

a. Run diagnostic programs for all sections of the computer other than the I/O section. Usually it will not be necessary to run diagnostic programs for non-I/O options.

b. Run the diagnostic program for the I/O device that is operating improperly.

c. Run a diagnostic program for another I/O device, or for the DMA system if the I/O device uses DMA. If DMA and the second I/O device functions properly, the fault probably is in the first I/O device or its interface card. Make oscilloscope, voltmeter, and ohmmeter checks to find the defective component or faulty connection.

d. If the diagnostic program for the second I/O device also shows failures, the I/O control card or I/O address card is probably at fault. Make oscilloscope, voltmeter, and ohmmeter checks to find the defective component or faulty connection. Paragraph 4-184 presents a simple test program which can be run during troubleshooting. Figure 4-100 is a timing diagram of the signals found on the I/O Control and I/O Address cards while running the test program. Note that only the CLF, STF, STC, and NOP instructions are shown. When running the test program it is necessary to change the HLT instruction to a NOP, thereby extending the time the NOP conditions will exist. If the DMA diagnostic program was run and showed failures, troubleshoot the DMA system. For further details regarding the I/O system, refer to the detailed theory in Section III of this manual.

4-487. POWER SUPPLY SECTION TROUBLESHOOTING.

4-488. GENERAL.

4-489. The troubleshooting instructions which follow are based on the assumption that the basic checkout procedure has been performed up to a point at which an abnormal condition, indicating a power supply fault, has been encountered.

4-490. As with other troubleshooting procedures described in this section, only the most usual faults and the most probable causes are dealt with. From the information given, the great majority of faults can be corrected without undue loss of time if the circuit theory of the power supply section is thoroughly understood.

4-491. The 2116C power supply section provides six principal regulated voltages. These voltages, +4.5, -2, +12, -12, +20, and -20 volts, are referred to as controlled voltages because they are turned on and off in a controlled manner. The first two voltages, +4.5 and -2 volts, furnish the operating potentials for most of the logic circuits in the computer. The +12 and -12 volt supplies provide voltages for the memory and I/O sections. The +20 and -20 volt supplies are used by the memory section.

4-492. The power supply also provides unregulated +7 and +35 volts, and regulated +32 volts. The +7 volt power is used for lighting all indicator lamps with the exception of the POWER lamp, which operates from regulated +12 volts. (Only early 2116C computers are equipped with the POWER indicator lamp.) The +35 volt power is used by optional circuit cards which install in the input/output section of the card cage (figure 1-3). The +32 volt power circuit is used when the optional power-fail auto-restart card is installed in slot 6.

4-493. In addition to the dc voltages furnished for use outside the power supply section, additional voltages are produced for use within the power supply section itself.

4-494. For information on the distribution of dc voltages in the computer, refer to figure 7-38 and the signal lists and backplane wiring list in Section VII.

4-495. If failure or overloading occurs for one of the six controlled voltages, some or all of the remaining five controlled voltages are shut down. Figure 3-30 illustrates the requirements of each of the controlled power supplies with respect to the outputs from other supplies. When one of the power supplies shuts down, the series regulator transistors for the supply cut off the flow of current to the load. The voltage source remains turned on.

4-496. Failure of controlled voltage does not generate a power-fail interrupt.

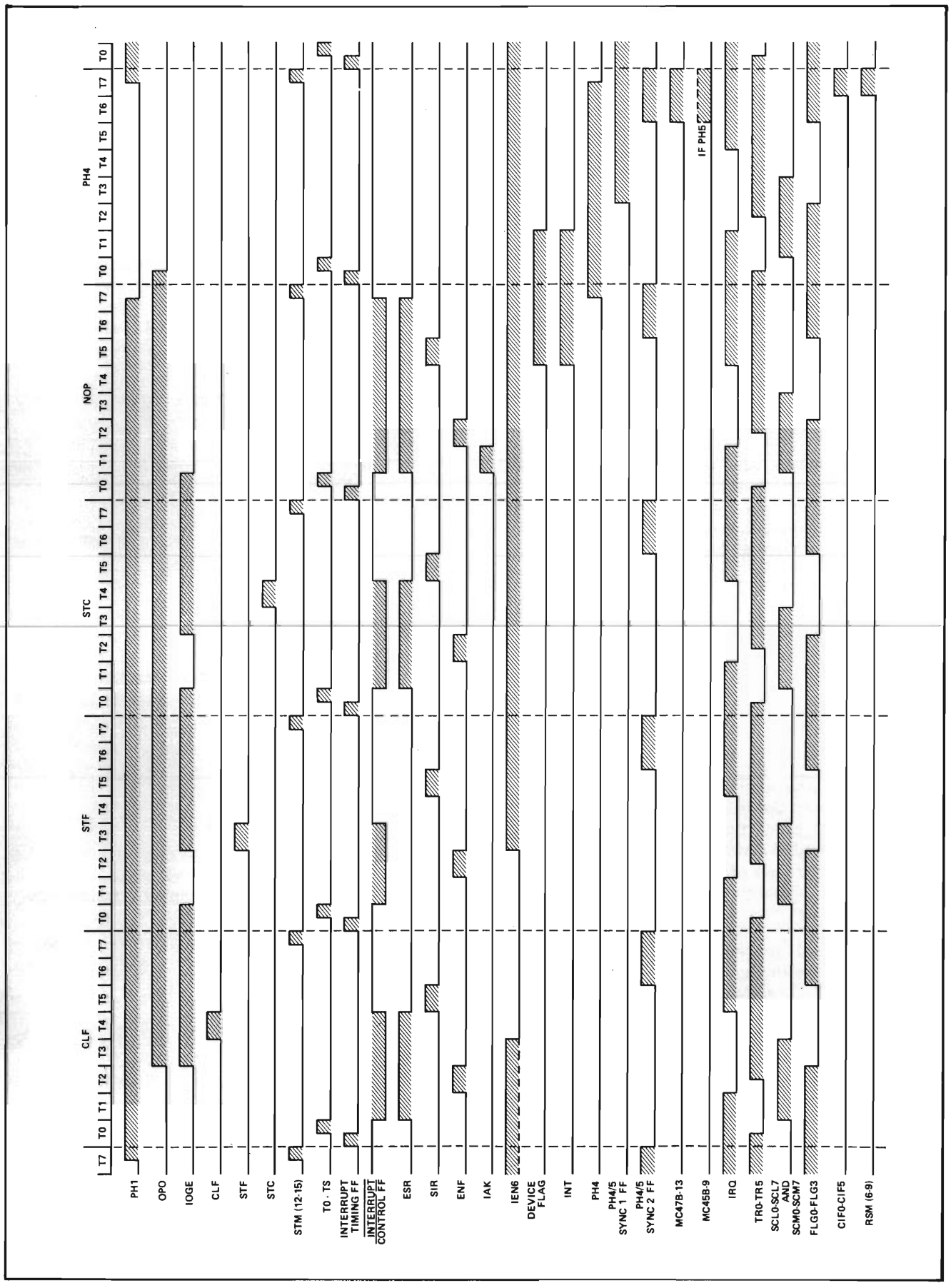


Figure 4-100. I/O Control and I/O Address Signals, Timing Diagram

4-497. When optional circuit cards in the computer card cage increase the load on the +4.5 or -2 volt power supply beyond rated capability, a power supply extended is used. This unit furnishes +4.5 and -2 volt power. These voltages connect in parallel with the same voltages produced in the computer. A power failure in the extender will cause a power-fail interrupt in the computer. Power failure in the extender will also cause shut-down of controlled voltages in the computer because the +4.5 or -2 volt power supply in the computer becomes overloaded.

4-498. Figures 4-101 through 4-104 are waveforms of the six controlled voltages during turn-on and shut-down initiated by the POWER switch. These waveforms were observed using an HP 181A Storage Oscilloscope, and are given here as an aid to understanding power supply operation.

4-499. Fuse locations and ratings are shown in figure 4-105.

4-500. POWER SUPPLY LOADING.

4-501. All controlled voltages, except +4.5 volts, function normally when entirely unloaded. The +4.5 volt supply requires a minimum load, otherwise dc shut-down may take place. This load is provided within the power supply by resistor A310R23.

4-502. To prevent +12, -12, +20, and -20 volts from being applied to the computer load circuits, memory supply regulator card A302 may be removed. This cuts off the series regulator transistors for these voltages.

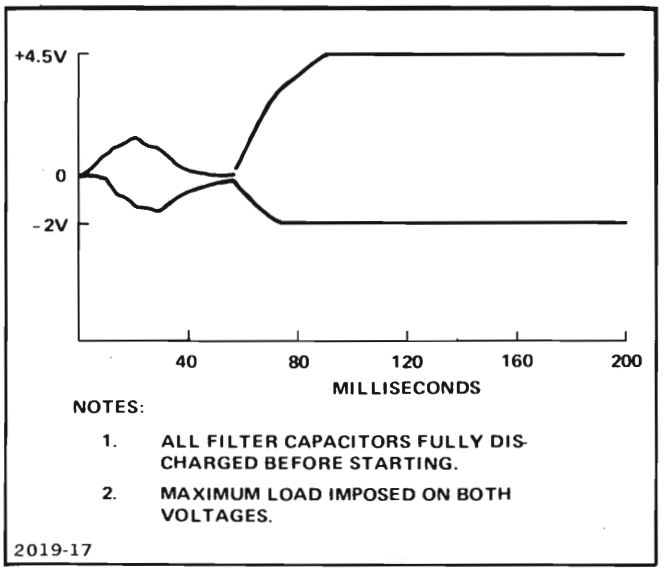


Figure 4-101. Turn-On Waveforms, +4.5 and -2 Volts

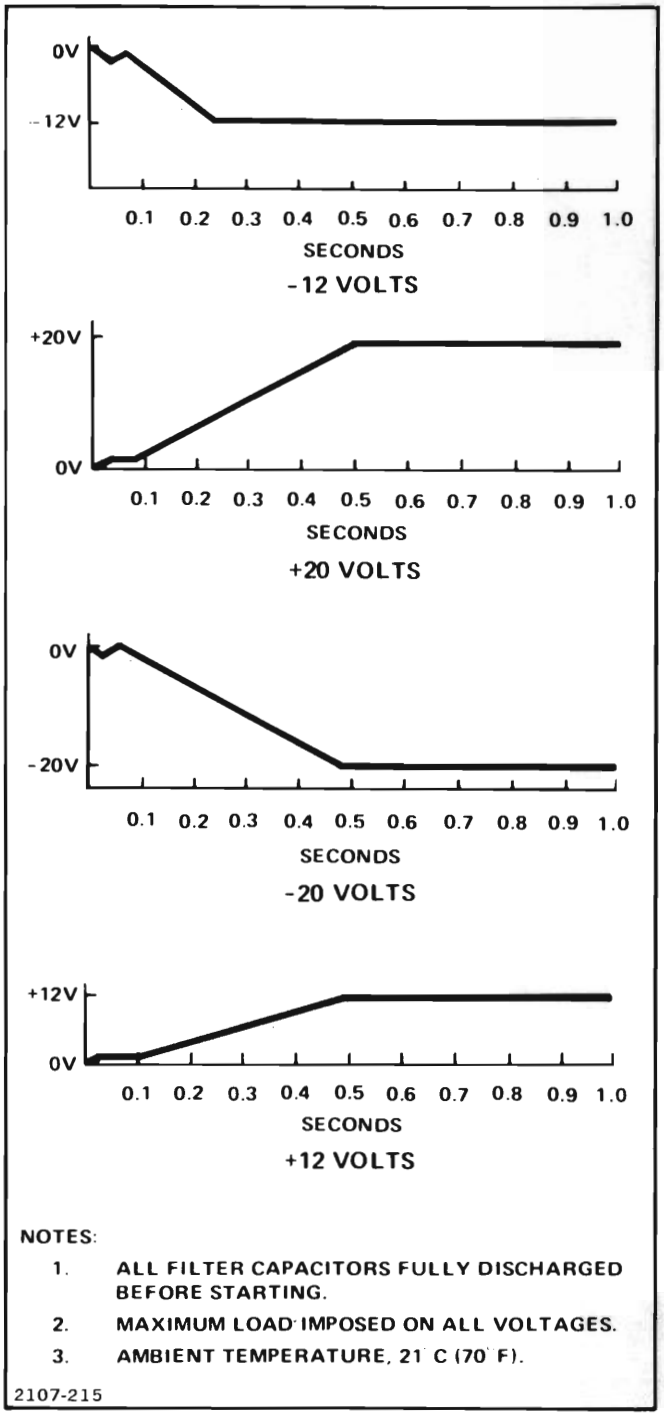


Figure 4-102. Turn-On Waveforms, -12, +20, -20, and +12 Volts

4-503. To prevent any controlled voltage from being applied to the computer load circuits, logic supply regulator card A301 may be removed.

4-504. SUBSIDIARY VOLTAGES.

4-505. If one of the subsidiary voltages used in the power supply section is at fault, one or more of the controlled voltages will also be affected. Troubleshooting the

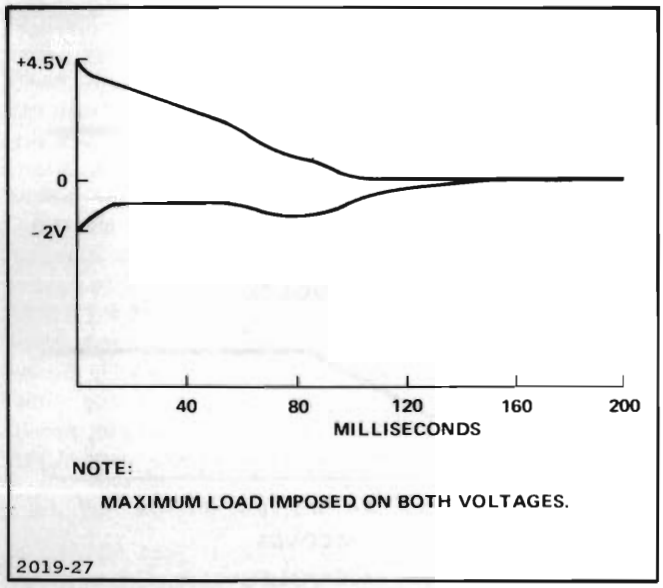


Figure 4-103. Shut-Down Waveforms, +4.5 and -2 Volts

controlled voltage will lead to the defective subsidiary voltage. Fuses F2, F3, and F8 (see figure 4-105) are used for the subsidiary voltages.

4-506. POWER SUPPLY TROUBLESHOOTING PROCEDURES.

4-507. PRECAUTIONS. Carefully observe the following warning and cautions when servicing the power supply.

WARNING

Before removing the transformer cover (figure 1-4) during troubleshooting, turn the POWER switch off, unplug the ac power cable, and wait 3 minutes for filter capacitors to discharge. If this procedure is not followed, ac line-voltage and dc voltages with heavy current capability exist at exposed terminals beneath the transformer cover. If the metal cover touches one of these terminals when being removed, the result may be death, injury, or damage to equipment.

CAUTION

Before removing or installing a circuit card in the power supply section, turn the POWER switch off and wait 3 minutes for filter capacitors to discharge. Failure to observe this precaution may result in damage to components.

CAUTION

Do not apply power to the computer when an overvoltage protection circuit is disconnected. An overvoltage condition can destroy components on cards in the card cage. To check operation of the power supply without the overvoltage protection circuits, first remove all cards from the card cage, with the exception of power fail interrupt card A6 and front panel coupler card A101. These cards must be in place before the power supply can be turned on. However, bear in mind that an overvoltage condition can destroy components on card A6.

CAUTION

If the fans in the computer are disconnected or inoperative, overheating and component damage will occur. To troubleshoot the computer ac circuits when the fans are inoperative, first eliminate all loading on the dc supplies by removing logic supply regulator card A301.

4-508. PRELIMINARY FAULT ANALYSIS. When power supply trouble is suspected, localize the fault by the following procedure. Then proceed to the indicated paragraph for further troubleshooting instructions.

a. If register lamps on display board A501 are lighted, proceed to step "c" below. If no register lamps are lighted, check the operation of the fans in the computer. If the fans are functioning, proceed to step "b" below. If the fans are inoperative, examine fuse A312F1 (see figure 4-105). If fuse is intact, proceed to paragraph 4-509. If the fuse is open and a replacement fuse blows, proceed to paragraph 4-510.

b. If a power supply extender is used, check +4.5 and -2 volts at overvoltage protection assembly A121 in the computer. If either or both voltages are not present, eliminate the extender as the source of trouble by the process described in paragraph 4-511.

c. Check the six controlled voltages with a four-digit dc digital voltmeter. These voltages are available at test jacks on overvoltage protection assembly A121. Acceptable voltage levels are listed in tables 5-1 and 5-2. Figure 3-30 shows the manner in which the controlled voltages affect each other. Continue the troubleshooting procedure as described in the following paragraphs:

(1) If no controlled voltage is available, proceed to paragraph 4-512.

(2) If only -2 volts is available, proceed to paragraph 4-513.

(3) If only -2 and +4.5 volts are available, proceed to paragraph 4-514.

(4) If all controlled voltages are available but no register indicator lamps are lighted, proceed to paragraph 4-515.

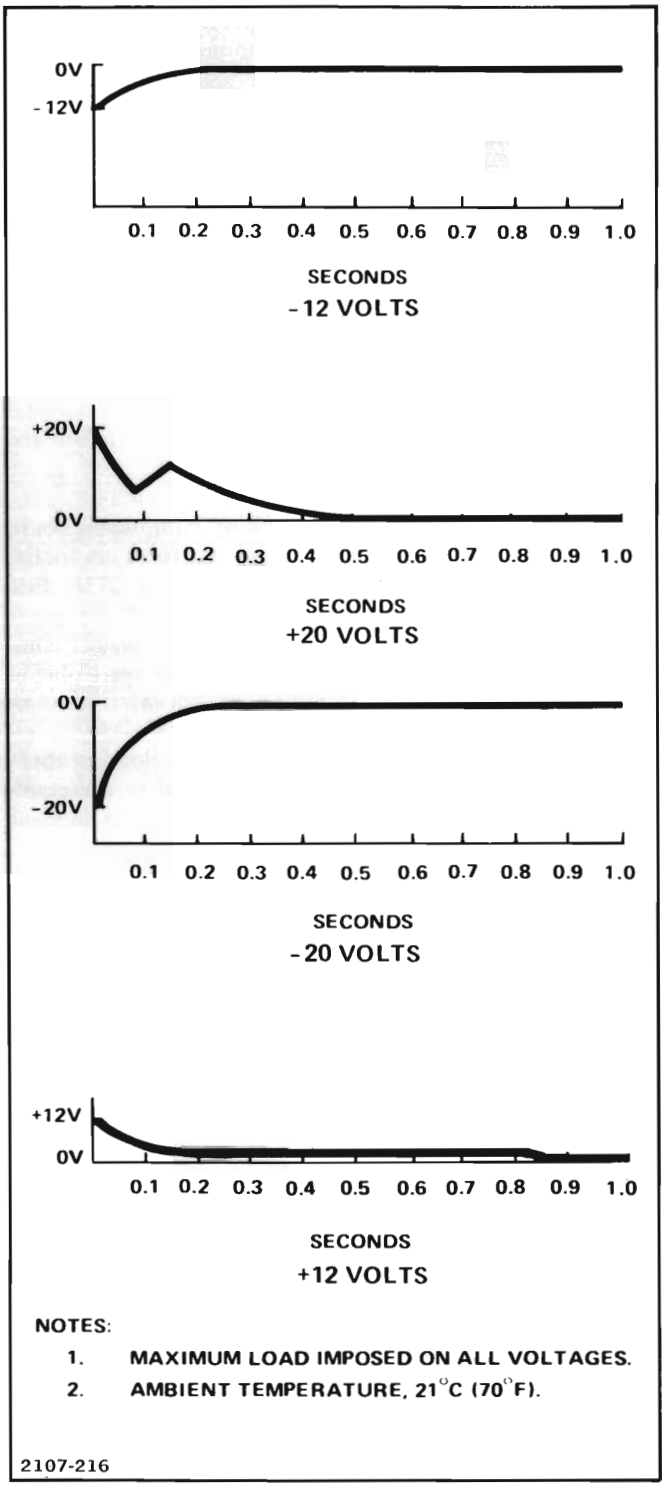


Figure 4-104. Shut-Down Waveforms, -12, +20, -20, and +12 Volts

4-509. OPEN IN AC CIRCUITS. If symptoms indicate an open in the computer ac distribution circuits, first ascertain that power is available at the ac outlet used. Also make sure fuse A312F1 is intact (see figure 4-105). Then turn the POWER switch off, unplug the ac power cable, open the card cage, and search for scorched electrical insulation. Remove the transformer cover and examine the power transformer and its connecting wires for burn discoloration. Replace any damaged components or wires. Then ascertain the cause of damage and correct the fault. Refer to figures 3-6, 7-32 through 7-34, and 7-36 through 7-38 for wiring information. If no evidence of burn damage is found, apply power to the computer and make voltage checks in the ac distribution circuits. (If the fans are not operating, eliminate overheating in the dc load circuits and the power supply by removing logic supply regulator card A301 before application of power.)

4-510. SHORT IN AC CIRCUITS. If fuse A312F1 is open and a replacement fuse blows, a short exists in the ac circuits. Turn the POWER switch off, unplug the ac power cable, open the card cage, and search by sight and smell for scorched electrical insulation in the power supply section. Remove the transformer cover and examine the power transformer and connecting wires for burn discoloration. Replace any damaged components or wires. If no evidence of burn damage is found, disconnect portions of the ac circuits and apply power to see whether fuse A312F1 still blows. (Because of the low resistance of the power transformer primary winding, ohmmeter checks are not practical.) Insulate the ends of disconnected wires with electrical tape. Disconnecting the fans will not result in overheating if power is left on for only a few seconds. Refer to figures 3-6, 7-32 through 7-34, and 7-36 through 7-38 for wiring information.

4-511. POWER SUPPLY EXTENDER. If a power supply extender is used, it must be eliminated as a source of trouble before troubleshooting is performed on the computer +4.5 or -2 volt power supply. Proceed as follows:

a. Turn off computer power.

b. Reduce power supply loading to within the capabilities of the computer power supply by sliding circuit cards A201 through A222 2 to 3 inches out of the card cage. The 48-pin connectors on the cards can remain in place.

c. Disconnect the extender power supply by removing the connector from J2 at the back of the extender unit. However, do not unplug the connector from A300J2 on the back of the computer; a thermal switch in the extender connects through A300J2 to complete the circuit for the computer thermal switch line (figure 3-7).

d. Turn on computer power. If +4.5 and -2 volts are now normal, the fault is in the extender.

e. If the fault persists, short the thermal switch in the extender by connecting a temporary jumper between the top two terminals on component board assembly A307. Then unplug the connector from A300J2. If the fault still remains, the defect is in the computer.

4-512. FAILURE OF ALL CONTROLLED VOLTAGES. If all six controlled voltages have failed, proceed as follows:

a. Make sure power-line voltage is available by checking for operation of the computer fans.

b. Examine the fuses beneath the transformer cover and on component board assembly A309 (see figure 4-105). If fuses are intact, proceed to step "c". If a fuse is open, replace it. If the replacement fuse blows upon application of power, the -2 volt power supply or a subsidiary supply is defective; proceed to step "g". (A short or overload in the -2 volt load circuits will cause complete dc shut-down, but will not blow a fuse unless the shut-down circuits are defective.)

c. If all fuses are intact, dc shut-down has taken place. Check for an overload or short external to the power supply, as described in paragraph 4-516. If there is no overload or short, proceed to step "d".

d. Make sure the thermal switches are closed. Do this by measuring the voltage between terminal A100TB1-5 and terminal XA6-52 (figure 3-7) with computer power on. (Attachment of the negative test lead to A100TB1-5, rather than to ground, is necessary because the series regulator transistors for -2 volts are cut off.) If the potential is approximately 10 volts dc, all thermal switches are closed; proceed to step "f".

e. If a thermal switch is open, make voltage checks along the thermal switch line to locate the open switch. When it is found, turn the POWER switch off, unplug the ac power cable, allow 3 minutes for filter capacitors to discharge, and make ohmmeter checks of the circuits in the overheated unit to locate the fault. Bear in mind that excessively high ambient temperature (over 55 degrees C, 131 degrees F) can cause a thermal switch to open. If this is the case, the environment is not suitable for the computer.

f. If thermal switches are closed, check the PSO signal at terminal A100TB1-1 (figure 3-7). In order to produce PSO, the +4.5 volt supply must be on. To turn on this supply, remove power from the computer, then ground the negative (bottom) side of capacitor A301C54, and re-apply power. If the PSO signal is then true and -2 volts is not available, the -2 volt power supply or a subsidiary supply is at fault; proceed to step "g". However, if the PSO signal remains false, the circuits on power fail interrupt card A6 which produce the signal are defective. Make sure +4.5 volts is available, then locate the defective component or faulty connection by making voltmeter and ohmmeter checks on circuit card A6. When the fault is found, remove the ground from A301C54.

g. If the -2 volt power supply or a subsidiary supply appears to be defective, replace logic supply regulator card A301. If this fails to correct the fault, proceed to the next step.

h. Replace large heat sink assembly A304. If this fails to correct the fault, proceed to the next step.

i. Make voltage and resistance checks to locate the fault. If the negative side of capacitor A301C54 was grounded in step "f" above, leave the grounding jumper in place. Start voltage checks at the applicable secondary winding of transformer A311T1, and measure voltages until abnormal conditions are found. Note that the voltages listed in the tables in figure 7-34 are for the normal operating condition in which current limiting does not take place. If the fault causes excessive power supply loading, current limiting may occur and voltages can differ from those listed but still be correct. When the fault is found, remove the grounding jumper from A301C54.

4-513. FAILURE OF +4.5 VOLTS. If -2 volts is available but the remaining controlled voltages are not, the +4.5 volt power supply is faulty or overloaded. To locate the fault, proceed as follows:

a. Examine fuses F12 and F13 on component board assembly A309 (see figure 4-105). If the fuses are intact, proceed to step "b". If a fuse is open, replace it. If the fuse blows again upon application of power, turn off computer power. Then make ohmmeter checks and disconnect components to identify the faulty part. Substitute spare plug-in units (if available) as an aid to fault localization.

b. If fuses are intact, check for an overload or short external to the power supply, as described in paragraph 4-516. If there is no overload or short, proceed to the next step.

c. Replace logic supply regulator card A301. If this fails to correct the fault, proceed to the next step.

d. Replace large heat sink assembly A304. If this fails to correct the fault, proceed to the next step.

e. Make voltage and resistance checks to locate the defective component or faulty connection. Start at the applicable secondary winding of transformer A311T1, and check voltages until abnormal conditions are found. Note that the voltages listed in the tables in figure 7-34 are for the normal operating condition in which current limiting does not take place. If the fault causes excessive power supply loading, current limiting may occur and voltages can differ from those listed but still be correct.

4-514. FAILURE OF MEMORY VOLTAGES. If +20, -20, +12, and -12 volts are not furnished, but -2 and +4.5 volts are available, proceed as follows:

a. Examine the fuses beneath the transformer cover (see figure 4-105). If all fuses are intact, proceed to step "b". If a fuse is open, replace it. If the replacement fuse

blows upon application of power, turn off the computer. Then make ohmmeter checks and disconnect components to localize the faulty part. In the case of plug-in units, substitute a spare unit as an aid to fault localization.

b. If all fuses are intact, check for an overload or short external to the power supply, as described in paragraph 4-516. If there is no overload or short, proceed to the next step.

c. Replace memory supply regulator card A302. If this fails to correct the fault, or if a spare card is not available, proceed to the next step.

d. Replace logic supply regulator card A301. If this action fails to correct the fault, or if a spare card is not available, proceed to the next step.

e. Replace large heat sink assembly A304 and small heat sink assembly A305. If this fails to correct the fault, proceed to the next step.

f. Turn off power and place a shorting jumper across capacitor C56 on logic supply regulator card A301. This short disables the shut-down circuits. Turn on power and check at A121 to determine the voltage that is faulty. Having found the failing voltage, locate the fault by means of voltage and resistance checks. Start at the applicable secondary winding of transformer A311T1, and check voltages until abnormal conditions are found. Note that the voltages listed in the tables in figure 7-34 are for the normal operating condition in which current limiting does not take place. If the fault causes excessive power supply loading, current limiting may occur and voltages can differ from those listed but still be correct. After finding the faulty component or connection, remove the short from capacitor A301C56.

4-515. FAILURE OF +7 VOLTS. If +4.5 volts is available but no register indicators light, examine fuse F10 (see figure 4-105). If the fuse is open and a replacement fuse blows, make ohmmeter checks of the +7 volt load circuits. If the fuse is intact, make voltmeter checks of the +7 volt circuits.

4-516. SHORT OR OVERLOAD OF CONTROLLED VOLTAGES. If symptoms indicate that one of the controlled voltages is shorted or overloaded, proceed as follows:

a. Turn off computer power, wait 3 minutes, then remove logic supply regulator card A301. This will disconnect the power supply loads in the card cage. If the symptoms disappear when power is re-applied, the short or overload is in the card cage or card A301 is defective; proceed to step "b". If the symptoms remain, the fault is in the power supply section; proceed to the applicable paragraph:

(1) Paragraph 4-512(d) if all controlled voltages have failed.

(2) Paragraph 4-513(c) if only -2 volts has failed.

(3) Paragraph 4-514(c) if only -2 and +4.5 volts have failed.

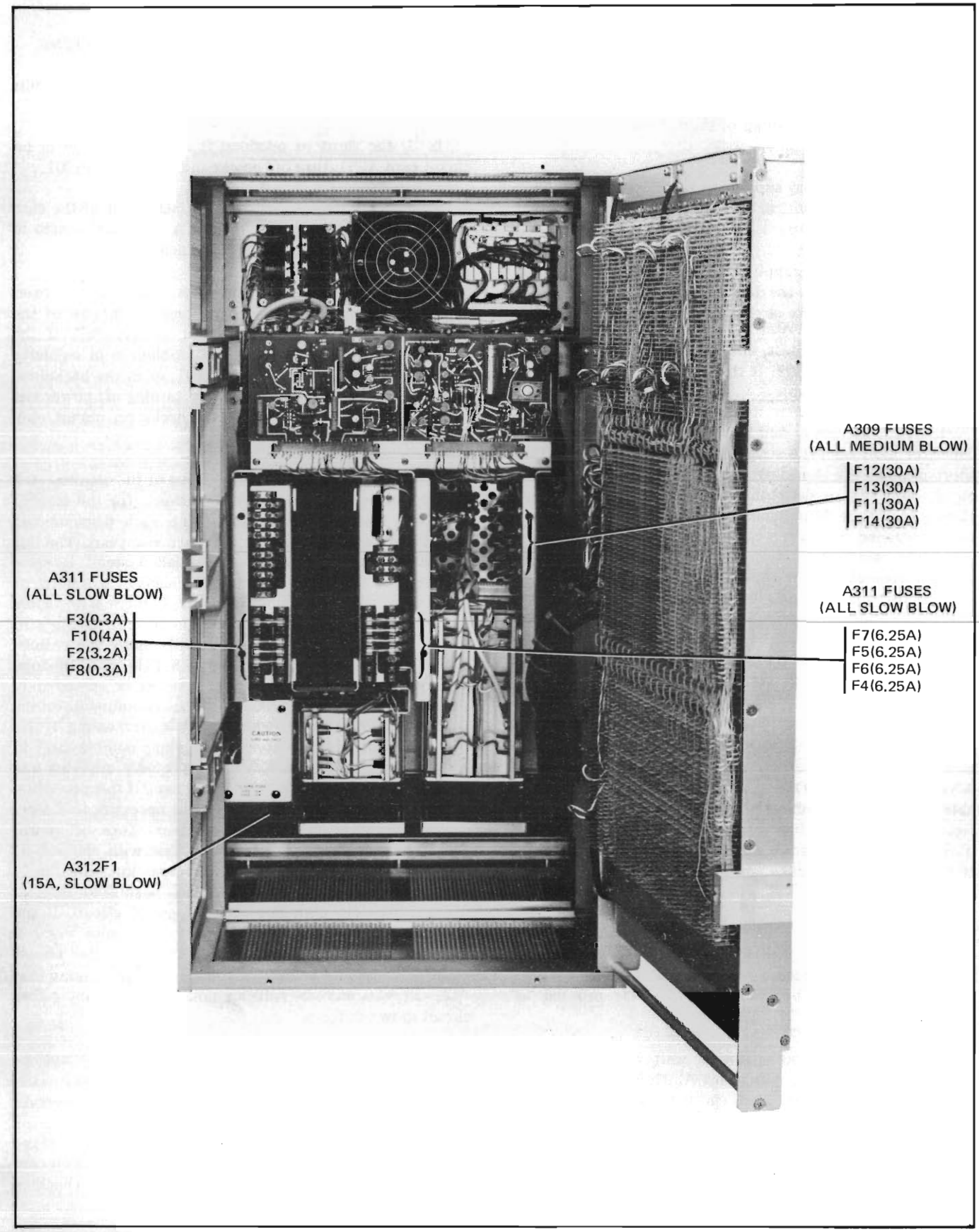
b. If the short or overload is in the card cage or on circuit card A301, turn off power and install card A301.

c. Slide all circuit cards 2 to 3 inches out of the card cage. As exceptions, cards A6 and A101 must remain in place, otherwise power cannot be turned on.

d. Apply power to the computer. If the short or overload symptoms disappear, the problem is in one of the disconnected circuit cards; proceed to step "e". If the symptoms do not disappear, the problem is in regulator card A301, circuit cards A6 or A101, or in the backplane wiring. Troubleshoot these items by turning off power and making resistance and continuity checks on circuit connections, wiring, and components.

e. Turn off power and replace one of the disconnected circuit cards. Turn on power and check for the trouble symptom. Continue this process with each disconnected circuit card until the trouble symptom reappears. The last card installed has the shorted or overloaded circuit. Remove the card and examine it carefully for signs of scorching, or for foreign material causing the short. If there is no visible evidence of the fault, replace the circuit card in the card cage using a card extender. Repeatedly apply and remove power by means of the POWER switch. (This must be done repeatedly because dc shut-down takes place immediately after power is available.) Touch various components on the circuit card to determine whether any is overheating. If this fails to reveal the faulty component, apply cooling spray to various parts of the card, while repeatedly applying and removing power until the fault disappears. If this procedure also fails to isolate the fault, it will be necessary to disconnect components until the short clears. Turn off power before removing each component. Start with electrolytic capacitors, then disconnect ceramic capacitors, and finally remove integrated circuits. If -2 volts is shorted, refer to figure 7-3 before removing each integrated circuit. If the illustration shows that the unit does not receive Vcc (-2 volts), the short cannot be within the integrated circuit package, and it can remain in place. Also bear in mind that +12, -12, +20, and -20 volts are not used by any integrated circuit shown in figure 7-3.

4-517. FAILURE OF POFP PULSE. If symptoms indicate failure of the POFP pulse, check the pulse by connecting an oscilloscope to pin 56 of power fail interrupt card A6. Each time the computer is turned on or off by the POWER switch, a positive pulse should be observed. If the POFP pulse is not present, troubleshoot the circuits on card A6 which generate the pulse (figure 7-5). Start by checking whether the PON signal is true when power is on.



2107-214

Figure 4-105. Fuse Locations

SECTION V

MAINTENANCE

5-1. INTRODUCTION.

5-2. This section describes preventive and corrective maintenance for the 2116C Computer. Not included are maintenance procedures for I/O devices, I/O interface cards, and other optional features. Maintenance information for these items is provided in the documentation for the optional feature concerned.

5-3. Preventive maintenance is performed at scheduled intervals, and its purpose is to prevent or minimize equipment deterioration. Included in the preventive maintenance procedures are performance tests which check computer operation.

5-4. Corrective maintenance is performed when required, and its purpose is to restore normal operation to the computer after a fault has been isolated to a replaceable component. Fault isolation methods are presented in section IV.

5-5. Each maintenance procedure is described in full in this section. When feasible, the detailed description is followed by a summary which repeats the main features of the procedure. This summary may be used as a guide for the performance of maintenance after the reader has become familiar with the detailed description and has put it to practical use at least once.

5-6. To determine the appearance and location of components and assemblies for the performance of maintenance, refer to the parts location diagrams presented in figures 1-3, 1-4, 1-5, and the illustrations in section VII.

5-7. SAFETY PRECAUTIONS.

WARNING

When the computer is on, use caution when working inside the computer cabinet. Many exposed conductors carry low dc voltages which are capable of supplying heavy currents if short-circuited, resulting in high heat and the possibility of painful burns. Use caution when manipulating metal tools or probes. A wrist watch, or a metal necklace, bracelet, or ring must not be worn.
Avoid dropping tools, screws, or other metal objects onto conductors. Remove power and recover dropped objects at once; if forgotten, damage could result later. AC power-line voltage is exposed when certain covers are removed; these covers are listed in the following paragraph. Exercise extreme caution when working in the computer with these covers removed, and never work under this condition unless another person is nearby and within sight. If feasible, unplug the ac power cable before performing any work inside the computer. Dangerous voltage exists even when the POWER switch is off. If working in the power supply section, wait 3 minutes for filter capacitors to discharge after removing power. To prevent explosion resulting from internal heating, always be sure that a replacement filter capacitor is properly connected with respect to polarity. Danger of death or serious injury exists if the precautions above are not observed.

5-8. HIGH VOLTAGE POINTS.

5-9. The highest voltage in the computer is the ac line voltage. This voltage is exposed when any of the following covers is removed:

a. The transformer cover (figure 1-4).

b. The cover or housing of ac section A312 (figure 1-4).

c. The left side cover of the computer cabinet.

d. The bottom panel on the card cage (figure 1-5).

e. The shrink tubing covering the terminals on the back of the POWER switch on control panel assembly A502.

5-10. TRANSFORMER COVER.

5-11. Before removing the transformer cover (figure 1-4), be sure the ac power cable is unplugged, and allow 3 minutes for filter capacitors to discharge. If these precautions are not observed, exposed terminals beneath the cover could be touched by the metal cover as it is removed; these terminals carry ac line voltage and low voltages with heavy current capabilities.

5-12. HEAT SINK ASSEMBLIES.

5-13. The collectors of transistors on the large and small heat sink assemblies (A304 and A305, figure 1-4) are elec-

trically common with exposed portions of the heat sinks. These exposed areas therefore have dc potentials as high as 20 volts.

5-14. DISPLAY BOARD ASSEMBLY A501.

5-15. The center contacts for lamps on display board assembly A501 are metal strips which swing aside to permit lamp removal. When these strips are moved, the edges of the strips can cause cuts. Use a cloth pad for moving the strips.

5-16. TEST EQUIPMENT GROUND.

5-17. If test equipment has a metal case, the negative test lead preferably should not be internally connected to the case. Instead, the case should be connected to a good earth ground through the test equipment power cord. This precaution prevents the danger of shock or possibility of short when the negative lead is connected to a point not at ground potential.

5-18. PREVENTIVE MAINTENANCE.

5-19. GENERAL.

5-20. The following preventive maintenance procedures are performed at monthly or semimonthly intervals, the frequency depending on the physical conditions prevailing at the particular site. Performance once per month is adequate for most sites. The monthly performance is applicable to computers which operate 24 hours per day, 7 days per week, and may be reduced in accordance with the amount of time the computer is turned off.

5-21. EQUIPMENT REQUIRED.

5-22. The following items are required for the performance of preventive maintenance:

a. Diagnostic program tapes for a complete mainframe checkout.

b. Source of compressed air for cleaning air filters, or two cleaned filters.

c. Source of low pressure air, such as vacuum cleaner air outlet, for blowing dust from computer.

d. One digital voltmeter of the type listed in table 1-5.

e. One general purpose Centigrade thermometer, accurate to at least ±1 degree, for measuring ambient temperature.

5-23. PROCEDURE.

5-24. Before starting preventive maintenance, set up the thermometer for measuring ambient temperature. The thermometer must be near the computer, but away from cold drafts and heat radiating objects. Do not place the thermometer on or in the computer. Plug in the digital voltmeter and turn it on. Then proceed as follows.

a. Voltage Checks. Before making voltage checks, the voltmeter must be allowed the warmup time prescribed by the manufacturer of the instrument. Also, the computer must run, with any type of program, for at least 15 minutes before making the voltage measurements. Voltage checks are then made as indicated below. If any voltage is not within the specified limits, make the necessary corrections as described in paragraph 5-28.

(1) Stop the computer program.

(2) Measure the six dc voltages listed in table 5-1. (Refer to table 5-2 for values for the +20 volt and - 20 volt supplies.) These voltages are available at test jacks on the overvoltage protection assembly.

(3) Set the voltmeter for reading rms ac voltage, and check each of the six voltages listed in table 5-1 for ripple. For each voltage, the indicated ripple should be less than 10 millivolts.

b. Air Filters. Clean the air filters at the bottom of the large and small heat sink assemblies in the power supply. Use the following procedure:

(1) Swing the card cage open.

(2) Remove the two air filters from the computer by pulling them downward.

WARNING

In the next step, use the compressed air nozzle with care. Never direct a compressed air stream toward a person. When reinstalling each filter be sure the notch in the filter is at the rear of the computer.

(3) Take the air filters out of the computer room, and using a source of compressed air, blow the dirt from each filter. Blow in the opposite direction from that in which air normally moves through the filter. Then reinstall each filter. If compressed air is not available at the computer site, install two spare filters which have been cleaned elsewhere.

c. Dust. If required, blow dust and other light debris from the computer, using the blower output from a vacuum cleaner or other source of low pressure air. Turn off the computer when performing this task. Loosen encrusted dust with a brush, and pay particular attention to heat dissipating areas.

d. Basic Checkout. Perform the basic checkout described in paragraph 4-9. If malfunctions are encountered, take the corrective action prescribed.

e. Diagnostic Program Test. Run diagnostic programs as described in paragraph 4-17. If an abnormal condition is found, correct the fault, then rerun the diagnostic programs.

5-25. Upon completion of preventive maintenance for the computer, perform preventive maintenance for I/O devices and other optional units.

Table 5-1. Voltage Regulator Outputs

NOMINAL VOLTAGE	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM
-2	-1.900	-2.000	-2.100
+4.5	+4.365	+4.500	+4.635
-12	-11.76	-12.00	-12.24
+20	(See table 5-2)		
-20	(See table 5-2)		
+12	+11.40	+12.00	+12.60

5-26. CORRECTIVE MAINTENANCE.

5-27. ELECTRICAL ADJUSTMENTS.

5-28. VOLTAGE REGULATOR ADJUSTMENT. The computer has six adjustable voltage regulators, furnishing the following nominal voltages: +4.5, -2, +12, -12, +20, and -20 volts. The outputs of some of these voltage regulators affect the outputs of others; therefore, adjustment of one regulator may necessitate adjustment of additional regulators. Furthermore, the regulators must be adjusted in a prescribed sequence.

5-29. The output voltage to which each regulator is adjusted, and the sequence of adjustment, are shown in table 5-3. Also listed in the table is the potentiometer which is adjusted for each of the six voltages. The outputs of the +20 and -20 volt regulators are set in accordance with the ambient temperature at the time of adjustment; table 5-4 shows the voltages required for various temperatures.

5-30. When adjustment procedures have been completed, all voltages are rechecked. The regulators are readjusted, if required, again following the sequence specified in table 5-3.

5-31. Equipment. Adjustment of the voltage regulators requires the following equipment:

a. One digital voltmeter, of the type listed in table 1-5.

b. One Centigrade thermometer (for measuring room temperature), accurate to at least ±1 degree.

5-32. Procedure. Adjustment of each of the six voltage regulators is essentially the same, and the procedure given below applies to all regulators. The adjustment starts with preliminary procedures, including a check of the ac power line voltage. If more than one voltage regulator is adjusted, the preliminary procedures (steps "a" through "f" below) need not be repeated after adjusting the first regulator. The adjustment procedure is as follows:

a. Place the thermometer near the computer. Select a position free of cold drafts and away from heat-radiating objects. Do not place the thermometer on or in the computer. Allow time for the thermometer to reach ambient temperature before reading it.

b. Turn on the voltmeter. Before using the instrument allow the warmup time prescribed by the manufacturer.

c. Turn on computer power. Also turn on all optional devices used by the computer. Allow 15 minutes warmup time for the computer. During this time, a program (of any type) must be running. The program will exercise the core memory and bring it to normal operating temperature.

d. When the computer and voltmeter have warmed up, set the voltmeter to the proper ac range and measure the power line voltage applied to the computer. If the computer is connected for 115-volt operation, the line voltage should be between 103.5 and 126.5 volts rms. For 230-volt operation, the line voltage should be between 207.0 and 253.0 volts rms.

e. If the power line voltage is above or below the permissible limits, do not attempt to adjust the voltage regulators. Turn off the computer and associated optional devices, and leave them off until the line-voltage fault has been corrected. If the line voltage is satisfactory, proceed with the voltage regulator adjustment.

f. Stop the program by pressing the HALT switch.

g. Set the voltmeter for measuring the dc voltage to be adjusted.

h. Connect one lead of the voltmeter to the ground test jack on overvoltage protection assembly A121. (Observe polarity.)

i. Connect the other lead of the voltmeter to the test jack on the overvoltage protection assembly marked with the dc voltage to be adjusted.

j. With a small screwdriver, adjust the voltage regulating potentiometer to bring the regulated voltage to about the center of the required range. (Refer to table 5-3.) Note that the adjustment voltage range is narrower than the range specified in table 5-1 or table 5-2.

k. When the voltage has been brought within the required range, measure the voltages listed below it in table 5-3. (The voltages are all available at test jacks on the

Table 5-2. Output of +20 Volt and -20 Volt Regulators

TEMPERATURE (°C)	DC VOLTAGE RANGE			TEMPERATURE (°C)	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM		MINIMUM	CENTER	MAXIMUM
0	20.50	21.00	21.50	28	19.38	19.88	20.38
1	20.46	20.96	21.46	29	19.34	19.84	20.34
2	20.42	20.92	21.42	30	19.30	19.80	20.30
3	20.38	20.88	21.38	31	19.26	19.76	20.26
4	20.34	20.84	21.34	32	19.22	19.72	20.22
5	20.30	20.80	21.30	33	19.18	19.68	20.18
6	20.26	20.76	21.26	34	19.14	19.64	20.14
7	20.22	20.72	21.22	35	19.10	19.60	20.10
8	20.18	20.68	21.18	36	19.06	19.56	20.06
9	20.14	20.64	21.14	37	19.02	19.52	20.02
10	20.10	20.60	21.10	38	18.98	19.48	19.98
11	20.06	20.56	21.06	39	18.94	19.44	19.94
12	20.02	20.52	21.02	40	18.90	19.40	19.90
13	19.98	20.48	20.98	41	18.86	19.36	19.86
14	19.94	20.44	20.94	42	18.82	19.32	19.82
15	19.90	20.40	20.90	43	18.78	19.28	19.78
16	19.86	20.36	20.86	44	18.74	19.24	19.74
17	19.82	20.32	20.82	45	18.70	19.20	19.70
18	19.78	20.28	20.78	46	18.66	19.16	19.66
19	19.74	20.24	20.74	47	18.62	19.12	19.62
20	19.70	20.20	20.70	48	18.58	19.08	19.58
21	19.66	20.16	20.66	49	18.54	19.04	19.54
22	19.62	20.12	20.62	50	18.50	19.00	19.50
23	19.58	20.08	20.58	51	18.46	18.96	19.46
24	19.54	20.04	20.54	52	18.42	18.92	19.42
25	19.50	20.00	20.50	53	18.38	18.88	19.38
26	19.46	19.96	20.46	54	18.34	18.84	19.34
27	19.42	19.92	20.42	55	18.30	18.80	19.30

NOTE: Voltages listed are negative for the -20 volt regulator.

Table 5-3. Voltage Adjustments

ADJUSTMENT SEQUENCE	NOMINAL VOLTAGE	ADJUSTMENT POTENTIOMETER	VOLTAGE RANGE		
			MINIMUM	CENTER	MAXIMUM
1st	-2	R76*	-1.980	-2.000	-2.020
2nd	+4.5	R66*	+4.455	+4.500	+4.545
3rd	-12	R125**	-11.88	-12.00	-12.12
4th	+20	R140**	(See table 5-4)		
5th	-20	R155**	(See table 5-4)		
6th	+12	R96*	+11.88	+12.00	+12.12

NOTES:
*Situated on Logic Supply Regulator Card A301.
**Situated on Memory Supply Regulator Card A302.

Table 5-4. Adjustment of +20 Volt and -20 Volt Regulators

TEMPERATURE (°C)	NOMINAL VOLTAGE	TEMPERATURE (°C)	NOMINAL VOLTAGE	TEMPERATURE (°C)	NOMINAL VOLTAGE
0	21.00	19	20.24	38	19.48
1	20.96	20	20.20	39	19.44
2	20.92	21	20.16	40	19.40
3	20.88	22	20.12	41	19.36
4	20.84	23	20.08	42	19.32
5	20.80	24	20.04	43	19.28
6	20.76	25	20.00	44	19.24
7	20.72	26	19.96	45	19.20
8	20.68	27	19.92	46	19.16
9	20.64	28	19.88	47	19.12
10	20.60	29	19.84	48	19.08
11	20.56	30	19.80	49	19.04
12	20.52	31	19.76	50	19.00
13	20.48	32	19.72	51	18.96
14	20.44	33	19.68	52	18.92
15	20.40	34	19.64	53	18.88
16	20.36	35	19.60	54	18.84
17	20.32	36	19.56	55	18.80
18	20.28	37	19.52		

NOTES:

1. Voltages listed are negative for the -20 volt regulator.
2. Voltage must be adjusted to within ±0.1 volt of the amount shown.

overvoltage protection assembly.) If any voltage is not within the limits specified in table 5-3, adjust it. Then proceed with measuring the remaining voltages listed in table 5-3, and adjust any that are not within the required limits.

l. When the regulators have been checked and adjusted, make a final measurement of the six adjustable regulated voltages. Readjust as required, again in the sequence specified in table 5-3. At the end of the adjustment procedure, make a final check of the six voltages.

5-33. Summary of Voltage Regulator Adjustment. The principal steps in adjusting a voltage regulator are as follows:

a. Measure the power line voltage. The voltage should be 103.5 to 126.5 volts (207.0 to 253.0 volts for 230-volt operation).

b. Connect the voltmeter to the appropriate test jack on the overvoltage protection assembly.

c. Adjust the appropriate voltage regulating potentiometer in accordance with table 5-3.

d. Check the remaining voltages listed in table 5-3. Adjust as required.

e. Measure all voltages available at the test jacks on the overvoltage protection assembly. Readjust as necessary. After completion of adjustments, make a final check of all voltages.

5-34. CURRENT LIMITER ADJUSTMENT. The computer has two adjustable current limiters; these are used for the +4.5 volt and -2 volt power supplies. Maladjustment of these regulators is indicated by an inability to correctly adjust the voltage regulator for the dc voltage concerned. (Inability to adjust a voltage regulator may also be due to other causes.)

5-35. The potentiometers for adjusting the +4.5 and -2 volt current regulators are R69 and R84 respectively, situated on logic supply regulator card A301. The potentiometers are factory sealed, and must not be adjusted in the field. (Test and loading equipment for making the adjustment normally is not available at field installations.) If adjustment of potentiometer R69 or R84 seems required, consult the nearest Hewlett-Packard Sales and Service Office.

5-36. POWER FAIL ADJUSTMENT. The following procedure describes how to adjust for the threshold voltage (power line voltage) at which the power fail interrupt occurs. This voltage is 102 to 100 volts rms ac for 115-volt operation, 204 to 200 volts rms ac for 230-volt operation. The adjustment procedure applies to a computer which does not use the Power Fail Interrupt With Automatic Restart Option (option 008). To determine whether the computer has this option, turn off computer power with the POWER switch, and partially withdraw the card from card cage slot 6. If this card has part number 12588-6001 marked on it, refer to the operating and service manual for the 008 option for the power fail adjustment procedure. (The manual part number is 12588-9002.) If the card in

slot 6 has part number 02116-6175 marked on it, the procedure which follows is applicable.

5-37. Two methods of making the power fail adjustment are presented. First, a precise adjustment procedure is described, which accurately sets the threshold voltage. Then a coarse adjustment procedure is described, which can be used as a temporary measure until equipment for making the precise adjustment is obtained.

CAUTION

The power fail interrupt causes a program jump to core storage location 4. If there is no power fail interrupt program in the computer, location 4 should contain a halt instruction. Otherwise a jump may occur from location 4 to a program which will destroy wanted data or cause undesired operation of I/O devices or controlled equipment.

5-38. Equipment. The coarse adjustment requires one Hewlett-Packard Extender Card (part no. 02116-63216).

5-39. The precise adjustment requires the following:

a. One Hewlett-Packard Extender Card (part no. 02116-63216).

b. One ac digital voltmeter with at least a 3-digit display, or an expanded scale ac voltmeter. The meter must be capable of reading ac voltage to within ±1 percent of the true value.

c. One general-purpose oscilloscope.

d. One variable autotransformer capable of supplying sufficient power for the computer. The 2116C requires 1000 to 1600 watts, depending on the optional features used. (To reduce the power requirement of the computer to a minimum, all circuit cards for optional features can be disconnected before making the adjustment. Be sure to turn off power before disconnecting or installing cards. To disconnect each card, slide it out two to three inches.) The autotransformer must be capable of reducing the power-line voltage to 100 volts rms if the computer is connected for 115-volt operation, or to 200 volts rms if the computer is connected for 230-volt operation. If only the more commonly available 115-volt type of autotransformer can be obtained, a 230-volt computer can be temporarily connected for 115-volts for the purpose of making the adjustment, and operated from a 115-volt power source. If this is done, be sure to reconnect the computer for 230-volt functioning after completing the adjustment.

5-40. Precise Adjustment. The precise power fail adjustment is made as follows:

a. Turn on the voltmeter and oscilloscope. Allow the prescribed warmup time before using these instruments.

b. Turn off the computer by means of the POWER switch.

c. Disconnect the Parity Error Card (part no. 12591-6001) from slot 15, if the computer has this optional card installed.

d. Using the extender card, extend the power fail interrupt card for test. This card is in slot 6.

e. Connect the autotransformer between the computer and the power line.

f. Connect the voltmeter for measuring the output voltage of the autotransformer.

g. Set the autotransformer to furnish 115 volts rms to the computer (230 volts if the computer is connected for 230-volt operation).

h. Turn on computer power. Allow 15 minutes warm-up time for the computer before making the adjustment. A program can be run during this time, if desired.

i. Adjust the oscilloscope for 1 volt/division vertical deflection, and a sweep rate of 1 millisecond/division.

j. Connect the ground lead of the oscilloscope to the negative lead of capacitor C2 on the power fail interrupt card. (This point is at card ground potential.)

k. After the computer and test instruments have warmed up, stop the computer (if it is running) by pressing the HALT switch.

l. Adjust the autotransformer to 100 volts (200 volts for a 230-volt computer).

m. Adjust the oscilloscope to set the horizontal trace at the center of the screen.

n. Connect the oscilloscope probe to test jack TP1 on the power fail interrupt card.

o. Press the PRESET switch.

p. On the power fail interrupt card, adjust potentiometer R7 to the center of its range of rotation.

q. Adjust the oscilloscope to obtain a display of two positive-going pulses. Do not alter the vertical gain.

r. Adjust potentiometer R7 on the power fail interrupt card until the positive peaks of the pulses are +1.0 to +1.5 volts. (See figure 5-1.) The pulse base line on the oscilloscope is below ground level; be sure to measure the pulse peaks with respect to ground, not with respect to the base line.

Note

After R7 has been set, the peak amplitude may drift above or below the +1.0 to +1.5 volt range. This is a normal condition caused by power line voltage variation.

s. With the autotransformer, adjust the power input to the computer to 102 volts rms (204 volts for a 230-volt computer).

t. Check the power fail adjustment by running the Power Fail Interrupt Test diagnostic program (tape no. 20434B or its latest revision). While the program is running, reduce the ac line-voltage to 100 volts rms (200 volts for a 230-volt computer). A power fail interrupt should occur as the voltage is being reduced.

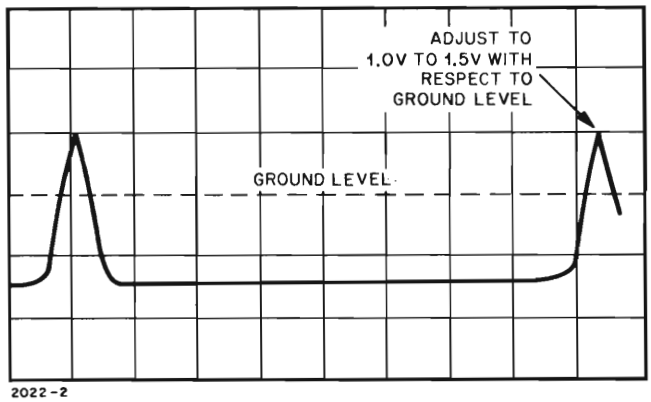
u. Turn off the computer by means of the POWER switch.

v. Remove the extender card and install the power fail interrupt card in slot 6. Components on the card must be to the right.

w. Replace all circuit cards in their normal positions. Components on the cards must be to the right.

x. Unplug the autotransformer.

y. Plug the computer power cord into the electrical outlet.



NOTE: Oscilloscope setting, 1V/cm and 1 millisec/cm.

Figure 5-1. Properly Adjusted Power Fail Pulses

5-41. Coarse Adjustment. A coarse adjustment of the power fail threshold voltage can be made without the use of a variable ac source, oscilloscope, or voltmeter. However, this procedure is recommended for temporary purposes only, and must be followed by proper adjustment as soon as practicable. The only equipment required is the Extender Card (part no. 02116-63216). An oscilloscope will be helpful, but is not essential. The procedure is as follows:

a. Turn on the oscilloscope, if one is available. Allow the prescribed warmup time before use.

b. Turn off the computer by means of the POWER switch.

c. Disconnect the Parity Error card (part no. 12591-6001) from slot 15 if the computer has this optional card installed.

d. Using the extender card, extend the power fail interrupt card for test. This card is in slot 6.

e. Turn on computer power. Allow 15 minutes warmup time for the computer before making the adjustment. A program can be run during this time, if desired.

f. Adjust the oscilloscope for 1 volt/division vertical deflection, and a sweep rate of 1 millisecond/division.

g. Connect the ground lead of the oscilloscope to the negative lead of capacitor C2 on the power fail interrupt card. (This point is at card ground potential.)

h. After the computer and oscilloscope have warmed up, stop the computer (if it is running) by pressing the HALT switch.

i. Adjust the oscilloscope to set the horizontal trace at the center of the screen.

j. Connect the oscilloscope, if used, to test jack TP1 on the power fail interrupt card.

k. On the power fail interrupt card, rotate potentiometer R7 fully counterclockwise.

l. Press the PRESET switch.

m. Rotate R7 slowly clockwise until pulses are observed on the oscilloscope or until the PRESET indicator lights.

n. Rotate R7 one-quarter turn counterclockwise from the point at which pulses were observed or at which the PRESET indicator lighted.

o. Turn off computer power and replace all circuit cards in their normal positions. Components on the cards must face to the right.

p. Restore the computer to normal use, and observe its operation. If the power failure interrupt occurs without noticeable line voltage problems, rotate R7 counterclockwise one-sixteenth of a turn. If power fail interrupts still occur, obtain the proper equipment and make the precise adjustment of R7.

5-42. MECHANICAL ADJUSTMENTS.

5-43. CARD CAGE DETENT ADJUSTMENT. The card cage detent mechanism ensures that the card cage is held in the correct position for sliding the cage in and out of the computer cabinet. Two spring plungers form the principal operating units, as illustrated in figure 5-2. Each plunger consists of a hollow set screw containing a spring loaded detent stud. When the card cage is swung shut, the spring loaded stud snaps into a groove, and the cage is held in the correct position for sliding into the computer cabinet.

5-44. Adjustment of the spring plunger is necessary if the plunger is too high or too low. If the plunger is too low, excessive force is needed to swing the card cage into and out of the detent position. If the plunger is too high, the card cage will not be held in the correct position for sliding the cage in and out of the computer cabinet. Furthermore, if the plunger is too high it may fail to withdraw the card cage slide from the computer cabinet when the card cage is pulled out.

5-45. The spring plungers are adjusted by turning them with a screwdriver. (A nylon locking stud in the side of each plunger holds the plunger in its adjusted position.) The adjustment procedure is as follows:

a. Turn off computer power.

b. Slide the card cage from the computer cabinet.

c. Unscrew both spring plungers until no detent action occurs when the card cage is swung open and shut.

d. Screw down one of the plungers until satisfactory detent action is encountered. This exists when the detent stud snaps into its groove when the card cage is swung shut with moderate force.

e. Screw down the second plunger until excessive force is required to swing the card cage into and out of the detent position. Then unscrew the second plunger until satisfactory detent action occurs.

5-46. CARD CAGE ROLLER ADJUSTMENT. The card cage slides into the computer cabinet on ball bearing rollers. (See figure 5-3.) Three of these rollers are used for each card cage slide; two are situated at the bottom of the slide and one at the top. The top roller can be raised or lowered, and locked into position, to permit the card cage to slide properly in and out of the computer cabinet.

5-47. Adjustment of a card cage roller is necessary if the roller is too high or too low. If the roller is too high, the card cage does not slide freely in and out of the computer cabinet. If the roller is too low, the card cage wobbles when it slides in or out.

5-48. Each of the upper ball bearing rollers is mounted on a screw which has an eccentric shoulder. By turning the screw, the roller is moved up or down. One-half turn of the screw moves the roller from its highest position to its lowest position. A cap nut locks the eccentric screw in the position required.

5-49. The adjustment procedure for the upper or lower roller on the left side of the computer (viewing the computer from the front) is as follows:

a. Turn off the computer by means of the POWER switch.

b. Unplug the computer ac power cable.

c. Remove the left side-cover of the computer cabinet.

d. Slide the card cage from the computer cabinet.

e. Swing the card cage open.

f. Loosen the cap nut which locks the roller to be adjusted. When doing this, use a screwdriver to prevent the eccentric screw from turning.

g. With the screwdriver, turn the eccentric screw to raise the ball bearing against the surface on which it rolls.

h. Holding the eccentric screw in adjustment with the screwdriver, tighten the cap nut.

i. Check the adjustment by moving the card cage slide in and out of the computer cabinet. The slide should move freely, but should have no vertical play. Repeat the adjustment if necessary.

j. Replace the side cover on the computer cabinet.

k. Plug in the computer ac power cable.

5-50. The adjustment procedure for the upper or lower roller on the right side of the computer (viewing the computer from the front) is described below. The procedure requires two persons.

a. Turn off the computer by means of the POWER switch.

b. Remove the right side-cover of the computer cabinet.

c. Slide the card cage from the computer cabinet.

d. Swing the card cage open.

Note

In steps e through i which follow, the weight of the card cage must be supported by one person while a second person makes the adjustments.

e. Remove the support plate from the inner right side of the computer cabinet.

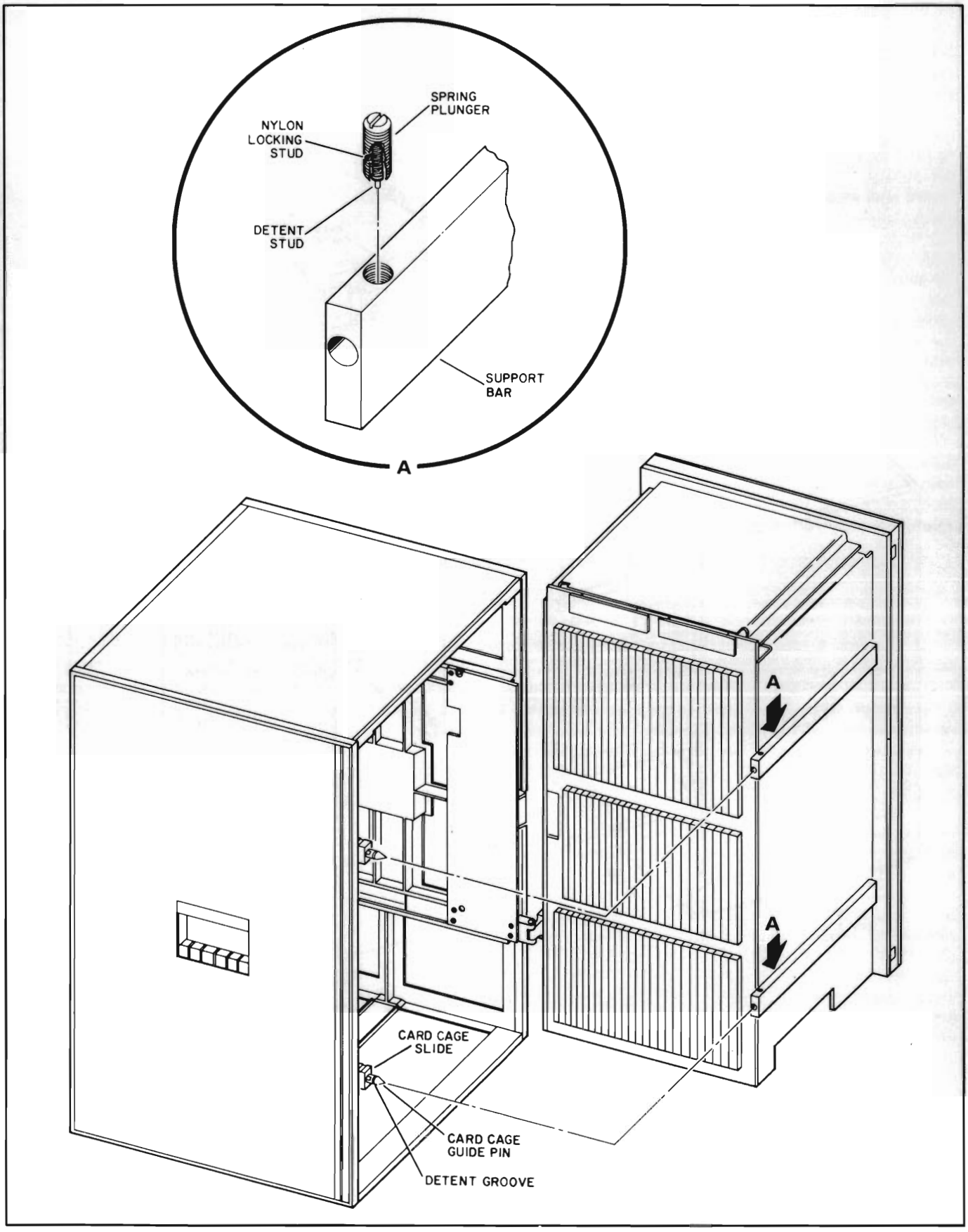


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Figure 5-2. Card Cage Detent Adjustment

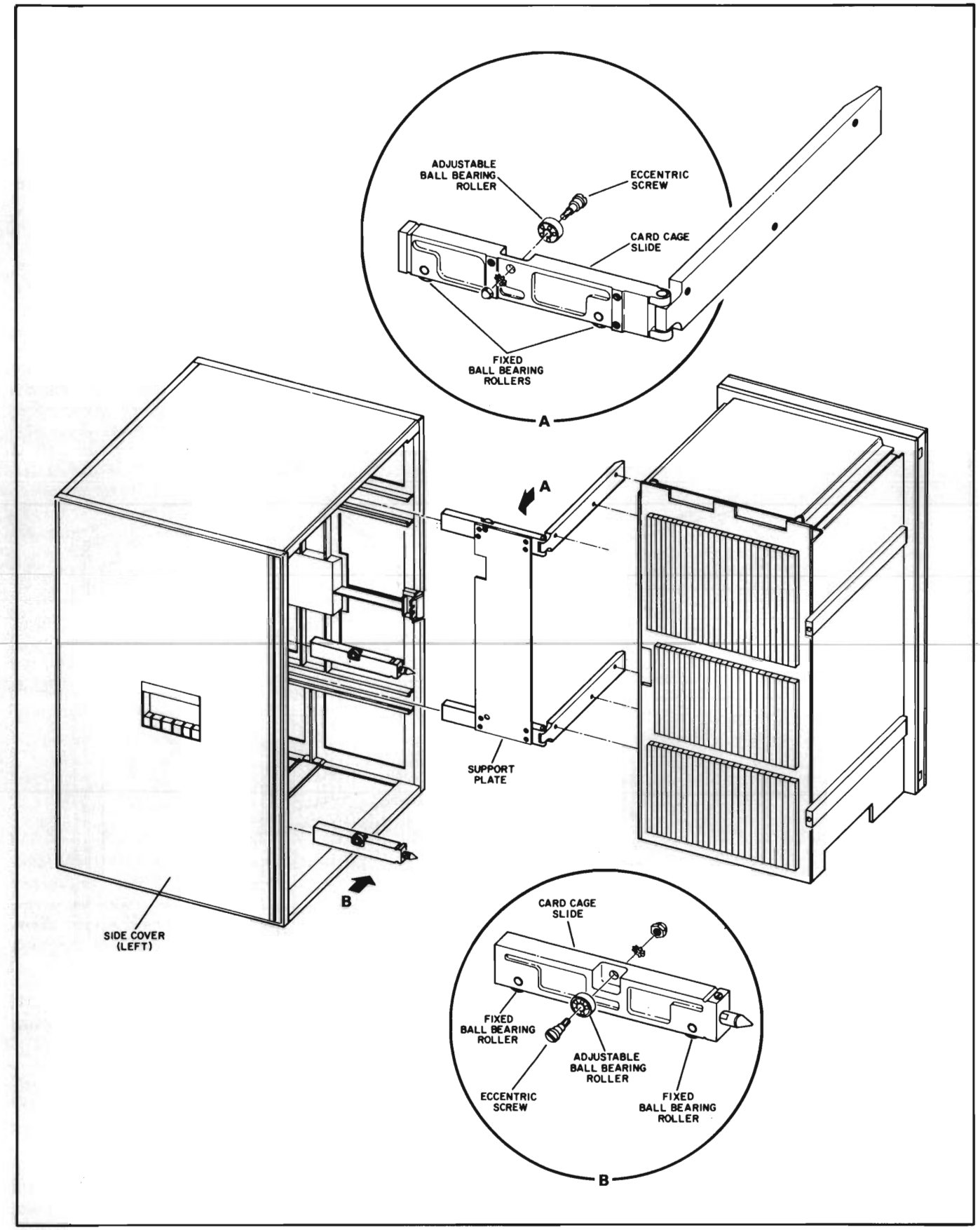

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Figure 5-3. Card Cage Roller Adjustment

f. Loosen the cap nut which locks the roller that is to be adjusted. When doing this, use a screwdriver to prevent the eccentric screw from turning.

g. Turn the eccentric screw to raise the ball bearing roller against the surface on which it rolls.

h. Hold the eccentric screw in adjustment and tighten the cap nut.

i. Install the support plate.

j. Check the adjustment by sliding the card cage in and out of the computer cabinet. The cage should move freely, but the card cage slide should have no vertical play. Repeat the adjustment if necessary.

k. Install the side cover on the computer cabinet.

5-51. DOOR HINGE. There is no adjustment for the door hinge.

5-52. CARD CAGE HINGE. There is no adjustment for the card cage hinge. Sagging of the card cage indicates that the right-hand card cage slides need adjustment.

5-53. DOOR LATCH. There is no adjustment for the door latch. During assembly of the computer, the two vertical catch rods actuated by the door tab catches are ground at the ends to provide the required latching action.

5-54. REMOVAL AND REPLACEMENT PROCEDURES.

5-55. The following paragraphs describe the methods for removing and installing various assemblies and units in the computer. Before performing any of the procedures, read the entire description of the procedure. Heed all warning and caution notices.

CAUTION

Failure to observe the waiting period in the following procedure may result in damage to components on circuit cards.

5-56. CARD REMOVAL AND REPLACEMENT. Before removing or installing cards in the power supply section, turn off power and allow 3 minutes for filter capacitors to discharge.

5-57. Before removing or installing cards in the card cage, turn off power and allow 5 seconds for bypass capacitors to discharge.

5-58. To remove a card from the power supply section, first take out the retaining screw near the center of the card. (See figure 1-4.) Then lift the card from its connector.

5-59. To remove a card from the card cage, first take off the card retainer (figure 1-10, item 1 or 9). Remove the front connector from the card (if any), loosen the card by pulling outward on the extractor levers at the top and bottom of the card (figure 1-8), then withdraw the card.

5-60. When removing or installing cards from the card cage, use extreme care not to damage traces or protruding components on the card or on adjacent cards.

5-61. Cards must be installed in the card cage with components to the right.

5-62. Cards in the card cage are keyed to prevent full insertion if upside down, but they are not keyed to prevent installation in the wrong slot. Therefore, make sure that the reference designation on the card extractor lever corresponds to the number of the slot being used. If there is no reference designation on the extractor lever, refer to figure 7-2 for the card location. Figure 1-4 shows the location of the two circuit cards used in the power supply section. One of these two cards has more connection pins than the other; this can serve as a means of identifying the connector which receives each card.

CAUTION

Failure to turn off power in the following procedure may result in shorting the +7 volt supply.

5-63. LAMP REPLACEMENT. Before removing a lamp from display board assembly A501, turn off power. Otherwise, when the metal strip which makes contact with the base of the lamp is swung aside, it may contact a point at ground potential and cause a short.

CAUTION

Failure to observe the following precautions may result in damage to components.

5-64. REPLACEMENT OF SEMICONDUCTOR DEVICES. When replacing semiconductor devices, be sure not to omit the insulating washer which separates the device from the mounting surface, if such a washer is used. These washers are indicated in the applicable parts location diagrams in section VII.

5-65. When directed to do so by a note on a parts location diagram, be sure to use silicone heat-conducting compound when installing a semiconductor device.

5-66. POWER TRANSFORMER REPLACEMENT. If power transformer A311T1 requires replacement, return the computer to the factory. Refer to paragraph 2-47 for instructions on packing and shipping the computer.

5-67. INTEGRATED CIRCUIT REPLACEMENT. Do not attempt to remove or install an integrated circuit unless a soldering iron specially made for this purpose is available. A rubber bulb with a suction tube for withdrawing molten solder is also an essential tool.

5-68. FILTER CAPACITOR REPLACEMENT. To replace a filter capacitor which is under capacitor board assembly A303, refer to figure 7-24 to determine the location of the capacitor, then proceed as follows:

a. Turn off computer power.

b. Unplug the ac power cable from the back of the computer.

c. Wait 3 minutes for filter capacitors to discharge.

d. Remove the rear cover from the computer.

e. Loosen the five rear retaining screws for capacitor board assembly A303 (figure 5-4).

f. Remove logic supply regulator card A301.

g. Remove memory supply regulator card A302.

h. Remove the screw from the negative terminal of the capacitor to be replaced.

i. Remove the nut from the positive terminal of the capacitor to be replaced.

j. Remove the small screw from the left end of the front (+4.5 volt) bus bar.

k. Remove the four nuts which hold down the front edge of the capacitor board.

l. Remove the three screws along the bottom of the capacitor board bracket in front of the capacitors, and remove the bracket.

m. Lift the front edge of the capacitor board, raising capacitors still fastened to it, and remove the capacitor to be replaced. If necessary, remove capacitors which are in front of it. Mark the reference designation on each good capacitor as it is removed. If the capacitor board cannot be raised high enough to clear the stud in the positive terminal of a capacitor, remove the stud with an Allen wrench. If the board still cannot be raised high enough, remove the right side cover of the computer cabinet, and loosen the +4.5 volt bus bar.

n. Remove the defective capacitor. Remove the stud from the positive terminal of the capacitor, mark the capacitor as faulty, and discard it in a waste receptacle. Do not place the defective capacitor with or near good capacitors.

o. Install the replacement capacitor. Use great care in ensuring that polarity is correct. Before installing the capacitor, determine from figure 7-24 the side of the capacitor which will be in front, and mark that side "front."

p. Reinstall any capacitors which were removed to gain access to the faulty capacitor. Use great care in ensuring that polarity is correct, and that each capacitor is replaced in its original position. Before installation, mark each capacitor with its reference designation (refer to figure 7-24) and mark the front side.

q. Reassemble all parts that were removed or loosened, using the reverse order from disassembly. Be sure that screws are tight, but do not strip threads. Replace all covers, close the card cage, and slide the cage into the computer.

WARNING

Because of the possibility of explosion and resulting injury, be sure all covers are installed and the card cage is slid into the computer before performing the next steps.

r. Plug in the ac power cable.

s. Make preparations for measuring the six regulated voltages, as described in paragraph 5-24, step "e." However, do not allow the prescribed 15-minute warmup period for the computer.

t. Turn on computer power.

u. Quickly measure the voltage and ripple of the six regulated voltages. Because of the lack of warmup, voltage deviations slightly greater than normal can be tolerated.

v. If any voltage is incorrect or has excessive ripple, turn off the computer immediately. Wait at least one hour for any incorrectly connected capacitor to cool, then make sure that filter capacitors have been correctly installed.

w. If the voltages are within the prescribed limits or only slightly beyond them, run any type of program for about 15 minutes, stop the computer, and recheck voltage levels and ripple. All measurements should now be within the prescribed limits.

5-69. REMOVAL AND INSTALLATION OF LARGE OR SMALL HEAT SINK ASSEMBLY. To remove large heat sink assembly A304 or small heat sink assembly A305, proceed as follows. (Two persons are required.)

a. Turn off computer power.

b. Unplug the ac power cable from the back of the computer.

c. Wait 3 minutes for filter capacitors to discharge.

d. Remove the transformer cover (figure 1-4).

e. If large heat sink assembly A304 is being removed, locate the two heavy wires that bolt to the front of the heat sink. In most cases one of these wires is white, and the other is white and blue. With a pencil, mark the color of each wire on the heat sink near the point of attachment. Then detach the two wires from the heat sink.

f. Remove the rear cover from the computer.

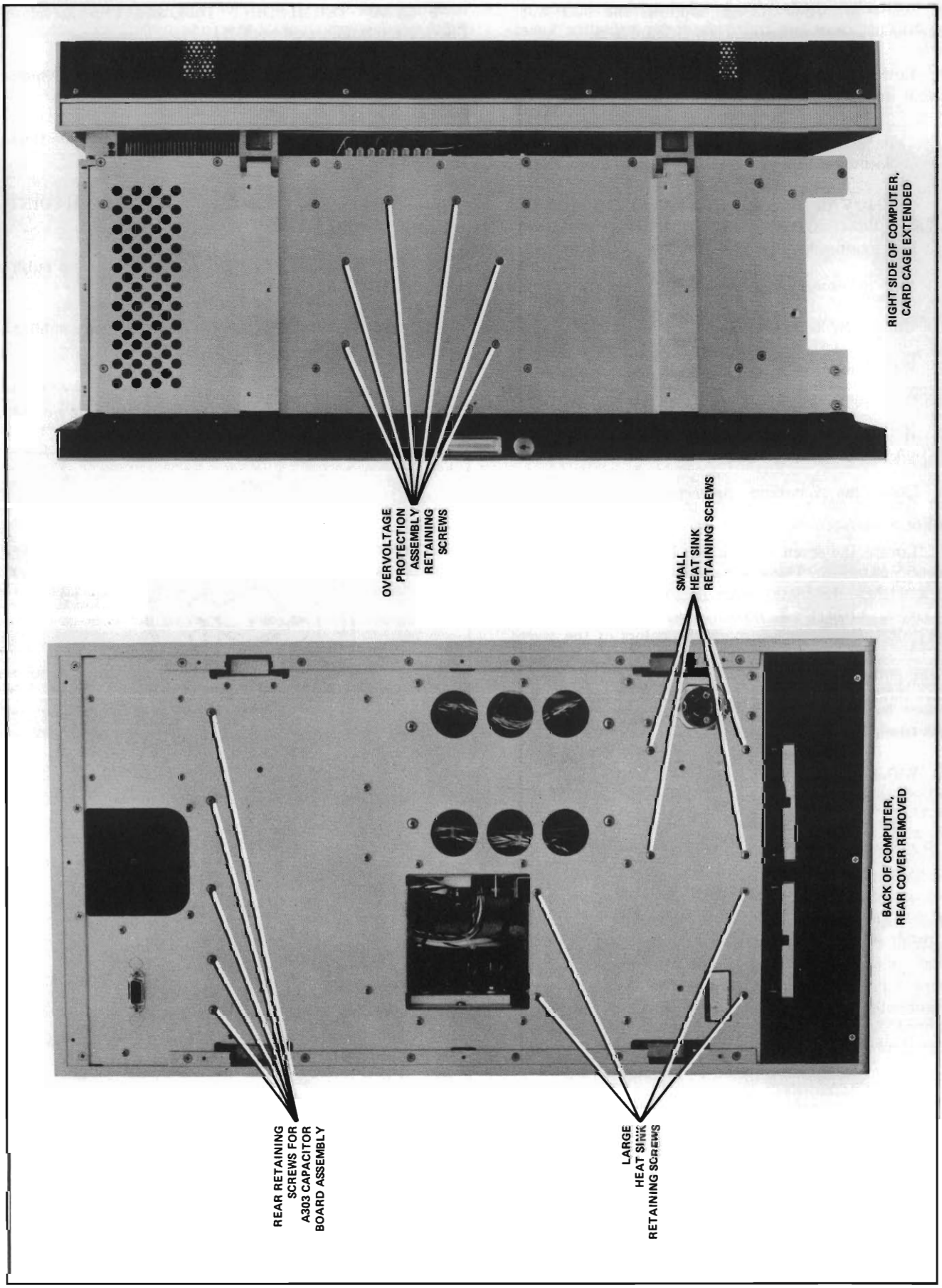

Figure 5-4. Removal of Assemblies

g. While a second person supports the heat sink, remove the heat sink retaining screws (figure 5-4).

h. Lower the heat sink out of its connector, and remove it from the computer.

5-70. The installation procedure for the large or small heat sink assembly is the reverse of the removal procedure.

5-71. REMOVAL AND INSTALLATION OF OVERVOLTAGE PROTECTION ASSEMBLY. To remove overvoltage protection assembly A121, proceed as follows:

a. Turn off computer power.

b. Unplug the ac power cable.

c. Wait 3 minutes for filter and bypass capacitors to discharge.

d. Remove the screws which hold the overvoltage protection assembly in place (figure 5-4).

e. Move the overvoltage protection assembly to the left.

f. Locate the seven wires which leave the overvoltage protection assembly. These are shown in figures 7-16 and 7-17, and their destinations are as follows: A100TB2-1, A100TB2-2, A100TB2-3, A100TB2-4, A100E1, A100E2, and A100E3. On figure 5-5 mark the colors of the seven wires. (Be sure the manual being used is the one assigned to the computer being worked on. The computer serial number should be marked on the title page of the manual.)

g. Disconnect the seven wires.

h. Withdraw the overvoltage protection assembly.

5-72. The installation procedure for the overvoltage protection assembly is the reverse of the removal procedure.

5-73. BACKPLANE CONNECTOR REPLACEMENT. Because of the numerous wires attached to backplane connectors, replacement of a connector should not be attempted in the field. If replacement is necessary, return the computer to the factory for installation of a new backplane. See paragraph 2-47 for information on packing the computer for shipment.

5-74. REPLACEMENT OF BACKPLANE CONNECTOR CONTACTS AND BACKPLANE WIRING. For replacing backplane connector contacts, and for removing and installing wires to these contacts, use the tools listed in paragraph 1-54 and 1-55. Instructions for using these tools are furnished in the following pamphlets, published by AMP Incorporated, Harrisburg, Pennsylvania:

a. A-MP TERMI-POINT Handbook, Amp publication no. 5070.

b. A-MP TERMI-POINT Tool and Clip Selection Chart, Amp publication no. GP 1935.

c. A-MP TERMI-POINT Manual Tool Mandrel Specifications, Amp publication no. GP 2075.

d. A-MP TERMI-POINT Component Color Code Data, Amp publication no. GP 1944.

e. Quality Control Procedure for A-MP TERMI-POINT Clip Applications, Amp publication no. GP 1920.

f. A-MP TERMI-POINT Extraction Tool, Amp publication no. IS 1942.

g. A-MP TERMI-POINT Pull Test Tool, Amp publication no. IS 1933.

h. Operator's Quality Check Procedure for A-MP TERMI-POINT Clip Application, Amp publication no. GP 2019.

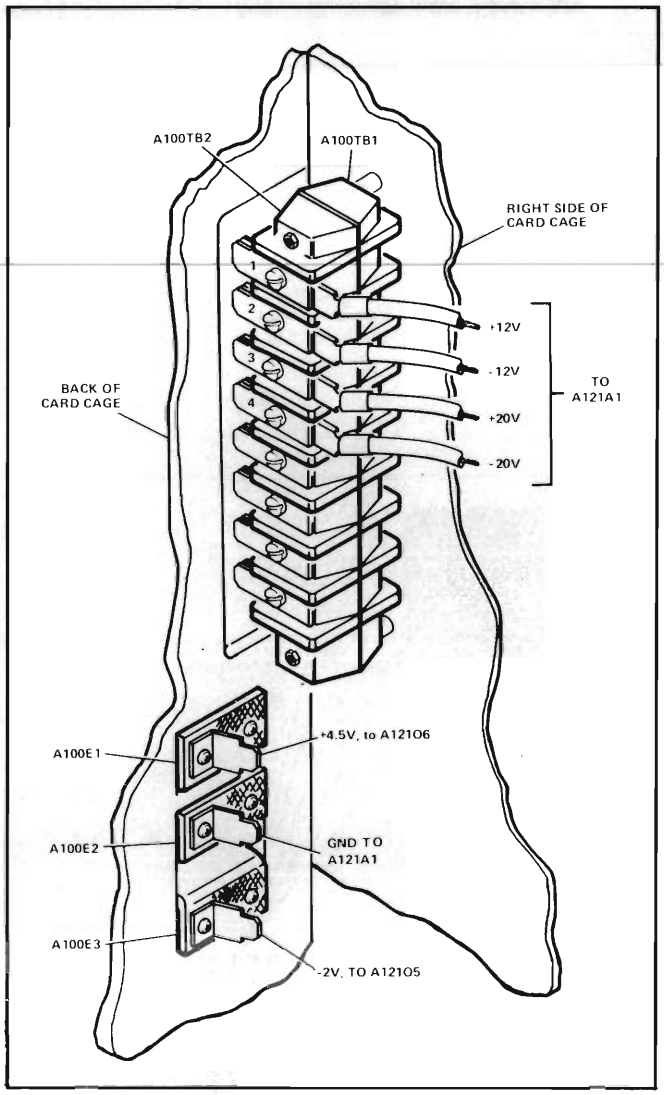

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Figure 5-5. Connections to A121 Overvoltage Protection Assembly, Viewed from Front of Computer

i. A-MP TERMI-TWIST Contact Replacement Tool, Amp publication no. IS 2038.

5-75. The following information is pertinent to use of the wiring tools:

a. Wiring post size is 0.031 x 0.062 inch.

b. Wires between backplane connectors are 26 gauge (American Wire Gauge), 7 strand, and insulation thickness is between 0.022 and 0.045 inch.

5-76. Wires which run from A100TB1, A100TB2, and A200TB1 to backplane connectors have a quick-disconnect lug which solders onto a contact of the backplane connector. A light soldering iron is used for removing and attaching these lugs.

5-77. The -2 volt, +4.5 volt, and ground-return circuits for all cards in the card cage are routed through small bus bars which are visible between the backplane connectors when they are viewed from the card side. The -2 volt backplane bus connects to pins 47 and 48 of all cards in the card cage. The +4.5 volt bus connects to pins 39 and 40 of all cards, and the card cage ground bus connects to pins 1, 2, 85, and 86. The card cage buses cannot be reached without major disassembly of the card cage, and if work is required on these buses, the entire computer must be returned to the factory.

5-78. LUG REPLACEMENT. Crimp-type lugs are used in the power supply section and at the three terminal strips on the card cage. If it becomes necessary to replace one of these, use a solder lug. (In field repair operations, soldering is more reliable than crimping.) If a solder lug of the required size is not available, the crimp-type lug may be reused by soldering to it. With either type of lug do not permit solder to run onto the portion of the lug which will be under a screw. (Hold this portion of the lug uppermost when soldering.) Observe the usual precautions for obtaining a good solder connection.

5-79. WIRE BUNDLING. If it becomes necessary to remove the ties which hold a wire bundle together, do not replace the ties with lacing cord. There are wires as small as 26 gauge (American Wire Gauge) in some bundles; lacing cord can sever the conductors in these wires, leaving no external evidence on the wire insulation. For wire bundling, use the following ties, tightened lightly with a pair of pliers:

a. Cable strap (HP part no. 1400-0493), for wire bundles 1/16 inch to 1-1/8 inches diameter.

b. Cable clamp (HP part no. 1400-0482), for wire bundles from 1/4-inch to 3 inches diameter.

5-80. REMOVAL AND INSTALLATION OF AIR FILTERS. To remove the air filter beneath large heat assembly A304 or small heat sink assembly A305, pull downward on the filter. To install the filter, press it upward into place. When installing, be sure the notch in the filter rim is toward the back of the computer; this notch provides clearance for the 110-volt wires entering the fan.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section provides information on ordering replacement parts for the 2116C Computer. The parts are listed in tables 6-1 through 6-17, and illustrated in figures 6-1 through 6-17. The tables and figures are presented in disassembly sequence. Index numbers on exploded views also are in disassembly sequence.

6-3. Table 6-18 defines abbreviations and reference designations used in the parts tables and in other portions of this manual.

6-4. Table 6-19 provides a listing of all electrical parts, and table 6-20 furnishes a listing of all mechanical parts, used by the computer in its basic configuration. In tables 6-19 and 6-20 parts are listed in part-number sequence. Not included in tables 6-19 and 6-20 are parts for sense amplifier card 02116-63207. (Because this card must not be repaired in the field, parts for it need not be stocked at field installations. The parts therefore are not listed.)

6-5. The last table in this section, table 6-21, identifies the manufacturers indicated by the manufacturer code numbers in the parts tables.

6-6. Not included in tables 6-1 through 6-17 are parts installed on circuit cards in the card cage. For convenience when troubleshooting the computer, information on these parts is included with the logic diagrams in section VII. A list of the circuit cards used in the basic computer configuration is included in table 1-1, and the locations of these cards are shown in figure 7-2.

6-7. DESCRIPTION OF PARTS TABLES.

6-8. The three major assemblies in the computer are the door assembly, the card cage assembly, and the power supply and back panel assembly. These are listed in table 6-1, together with the attaching parts for these assemblies. (Attaching parts are the parts which hold the assemblies in place.) Also included in table 6-1 are the parts which comprise the computer cabinet.

6-9. Tables 6-2, 6-4, and 6-7 list parts for the three major assemblies. The remaining parts tables in this section list parts in the assemblies which make up these three major assemblies.

6-10. The parts tables furnish the following information:

a. The "FIG & INDEX NO." column is headed by an identification of the illustration which shows the parts listed in the table. Below this is the index number (callout number) which identifies each part in the illustration.

b. The "HP PART NO." column lists the Hewlett-Packard part number for each part.

c. The "DESCRIPTION" column names and describes the part. In the case of electronic components, also included is the reference designation of the part, as given on the appropriate schematic diagram. Items in the "DESCRIPTION" column are indented, and preceded by one or more asterisks, to indicate the relationship of the part with preceding parts listed. (See example below.) One asterisk indicates a subassembly of the previous assembly listed, or attaching parts for the subassembly. (Attaching parts are always listed after the item which they attach.) Two asterisks indicate a subassembly of the previous assembled item which has one asterisk, or an attaching part for such a subassembly. Similarly, three asterisks indicate a subassembly of the preceding assembled item that has two asterisks. The symbols "— — — x — — —" follow the last of one or more attaching parts.

EXAMPLE:

Computer
* Card Cage Assembly
(Attaching Parts)
* Screw, Machine, PH, No. 8-32, 3/4 in.
— — — x — — —
** Overvoltage Protection Assembly
(Attaching Parts)
** Screw, Machine PH, No. 6-32, 1/2 in.
** Nut, Plain, Hexagon, No. 6-32
— — — x — — —
*** Overvoltage Protection Subassembly
(Attaching Parts)
*** Screw, Machine, PH, No. 6-32, 1/4 in.
*** Washer, Lock, split, No. 6
— — — x — — —

d. The "MFR CODE" column in the parts tables is a number identifying the manufacturer of each item. Table 6-21 gives the names and addresses of the manufacturers.

e. The "MFR PART NO." column gives the manufacturer's part number for each item listed.

f. The "UNITS PER ASSY" column states the quantity of each part used per assembly or subassembly.

6-11. When a part number is included in the title of a parts table, the assembly covered by the table can be ordered as an assembled unit. If the part number is not included in the table title, only component parts of the assembly can be supplied.

6-12. ORDERING PROCEDURE.

6-13. Parts made by manufacturers other than Hewlett-Packard can be ordered either from the manufacturer or from Hewlett-Packard. To order from manufacturers other than Hewlett-Packard, send the order to the address listed in table 6-21. To order parts from Hewlett-Packard, or to obtain further information about parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. (These offices are listed at the back of this manual.) When ordering from Hewlett-Packard, give the following information for each part:

a. Computer model number.

b. Computer serial number.

c. Hewlett-Packard part number.

d. Description of part.

e. Circuit reference designation, if the part is an electronic component.

f. If the part is installed on an etched circuit card or board, give the revision code stamped in ink on the card or board. If there is no inked number, quote the metal etched number.

g. Include assembly reference designation as a prefix. For instance, order capacitor C1 of shift logic card A108 by the reference designation A108C1.

6-14. To order a part not listed in the replaceable parts tables, give a complete description of the part, and describe its function and location.

Table 6-1. HP 2116C Computer, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	2116C	COMPUTER			
1	02116-0105	* Fan Cover	28480	02116-0105	1
		(Attaching Parts)			
2	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	2
3	2190-0047	* Washer, Recessed, No. 6	00000	OBD	2
4	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
5	02116-63219	* Door Assembly (A500) (see fig. 6-2)	28480	02116-63219	1
		(Attaching Parts)			
	2200-0709	* Screw, Nylon, FH, No. 4-40, 3/8 in.	00000	OBD	4
		- - - x - - -			
6	0570-1049	* Spring Plunger	01226	M-54N	2
7	02116-2013	* Support Bar	28480	02116-2013	1
		(Attaching Parts)			
	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	6
	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	6
		- - - x - - -			
8	02116-0028	* Support Plate	28480	02116-0028	1
		(Attaching Parts)			
9	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	8
10	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	8
		- - - x - - -			
11	02116-2015	* Bearing Shaft	28480	02116-2015	4
12	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	2
13	0590-0010	* Cap Nut, No. 8	00000	OBD	2
14	2190-0010	* Washer, Lock, ext-tooth, No. 8	00000	OBD	2
15	02116-2003	* Eccentric Screw, No. 8	28480	02116-2003	2
16	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	2
17	02116-2016	* Hinge Pin	28480	02116-2016	2
18	02116-2012	* Hinged Slide	28480	02116-2012	2
19	02116-2014	* Hinged Bar	28480	02116-2014	2
		(Attaching Parts)			
20	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	6
21	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	6
		- - - x - - -			
22	02116-63223	* Card Cage Assembly (see fig. 6-4)	28480	02116-63223	1
23	02116-2015	* Bearing Shaft	28480	02116-2015	4
24	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	4
25	0590-0010	* Cap Nut, No. 8	00000	OBD	2
26	2190-0010	* Washer, Lock, ext-tooth, No. 8	00000	OBD	2
27	02116-2003	* Eccentric Screw, No. 8	28480	02116-2003	2
28	1410-0009	* Bearing, Ball, Annular	21335	SIKFS58115	2
29	02116-2023	* Insert, Catch Rod	28480	02116-2023	2
30	02116-2002	* Slide Pin	28480	02116-2002	2
31	02116-2011	* Lower Slide	28480	02116-2011	1
	02116-2010	* Upper Slide (not shown in fig. 6-1)	28480	02116-2010	1
32	2360-0204	* Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	4
33	02116-2034	* Tab Catch, Upper	28480	02116-2034	1
		(Attaching Parts)			
34	2200-0143	* Screw, Machine, PH, 4-40, 3/8 in.	00000	OBD	1
35	2190-0108	* Washer, Lock, split, No. 4	00000	OBD	1
		- - - x - - -			

Table 6-1. HP 2116C Computer, Replaceable Parts (Continued)

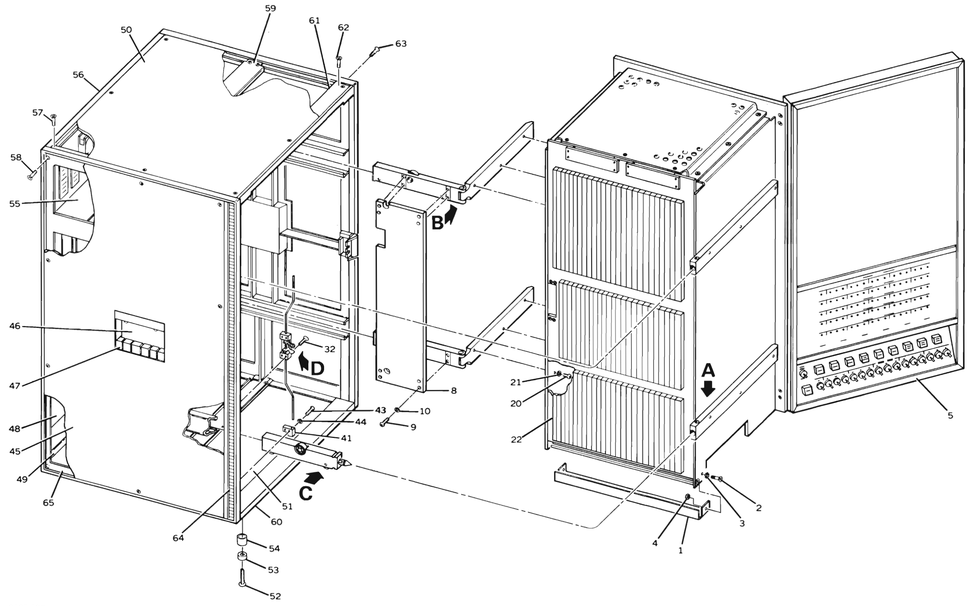
FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-					
36	02116-2063	* Tab Catch, Lower	28480	02116-2063	1
		(Attaching Parts)			
37	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
38	2190-0108	* Washer, Lock, split No. 4	00000	OBD	2
		- - - x - - -			
39	1460-0742	* Spring, Compression, 5/8 in. long, 3/16 in. ID	00000	OBD	1
40	02116-2033	* Catch Rod	28480	02116-2033	2
41	02116-2032	* Latch Retainer	28480	02116-2032	1
42	02116-2023	* Guide, Rod, Lower	28480	02116-2023	1
	02116-2067	* Guide, Rod, Upper (not shown in fig. 6-1)	28480	02116-2067	1
		(Attaching Parts)			
43	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
44	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	2
		- - - x - - -			
45	02116-0013	* Side Cover	28480	02116-0013	2
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	20
		- - - x - - -			
46	5060-0735	* Retaining Plate, Handle	28480	5060-0735	2
		(Attaching Parts)			
	2360-0201	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	4
		- - - x - - -			
47	5060-0763	* Handle	28480	5060-0763	2
48	02116-01118	* Cover, Upper-Rear	28480	02116-01118	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	9
		- - - x - - -			
49	02116-0014	* Cover, Lower-Rear	28480	02116-0014	1
		(Attaching Parts)			
	2360-0192	* Screw, Machine, FH, No. 6-32, 1/4 in.	00000	OBD	3
		- - - x - - -			
50	02116-0016	* Cover, Top	28480	02116-0016	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	8
		- - - x - - -			
51	02116-0016	* Cover, Bottom	28480	02116-0016	1
		(Attaching Parts)			
52	2360-0209	* Screw, Machine, PH, No. 6-32, 1 in.	00000	OBD	4
53	0403-0091	* Insert, Foot	28480	0403-0091	4
54	02116-2057	* Foot, Cabinet	28480	02116-2057	4
		- - - x - - -			
55	02116-63217	* Power Supply and Back Panel Assembly (see fig. 6-7)	28480	02116-63217	1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	14
		- - - x - - -			
56	02116-2009	* Rear Brace	28480	02116-2009	2
		(Attaching Parts)			
57	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
58	2360-0201	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
		- - - x - - -			
59	02116-0012	* Center Brace	28480	02116-0012	2
		(Attaching Parts)			
	2360-0196	* Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	8
		- - - x - - -			
60	02116-2041	* Brace, Front, Lower	28480	02116-2041	1
		(Attaching Parts)			
	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4

Table 6-1. HP 2116C Computer, Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-					
61 ①	02116-2077	* Brace, Top-Front (Attaching Parts)	28480	02116-2077	1
62	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
63	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
		– – – X – – –			
64	5000-0131	* Trim, Aluminum	28480	5000-0131	4
65	02116-2017	* Mainframe	28480	02116-2017	2
		ACCESSORIES (not shown in fig. 6-1)			
	02116-63266	Accessory Kit	28480	02116-63266	1
②	02116-63221	Accessory Kit	28480	02116-63221	1
	5060-8323	Cable, Power	28480	5060-8323	1
	5080-6599	Absolute Block Loader	28480	5080-6599	1
	02115-6047	Cable, Extending	28480	02115-6047	1
	02116-63216	Extender Board, Single Connector	28480	02116-63216	1
	02116-63251	Cable Extending	28480	02116-63251	1
		– – – X – – –			
	1400-0716	Tag, Identification	28480	1400-0716	1
	7120-0134	Tag, Serial No.	28480	7120-0134	1
	7120-2416	Label	28480	7120-2416	1
	5060-6236	Kit, Rack Mounting	28480	5060-6236	1
	5080-6595	Pad, Coding, Fortran	28480	5080-6595	1
	5080-6596	Pad, Coding, Assembler	28480	5080-6596	1
	02116-8177	Decal	28480	02116-8177	1

① On computers with serial number 1108A00276 and above, part number 02116-2041 (index no. 60) is used for both the top and lower front brace and part number 02116-2077 (index no. 61) is not used.

② This Kit is used on computers with serial number prefixes below 1047A, and provides Power Cable (5060-2267) and Label (7120-2433).



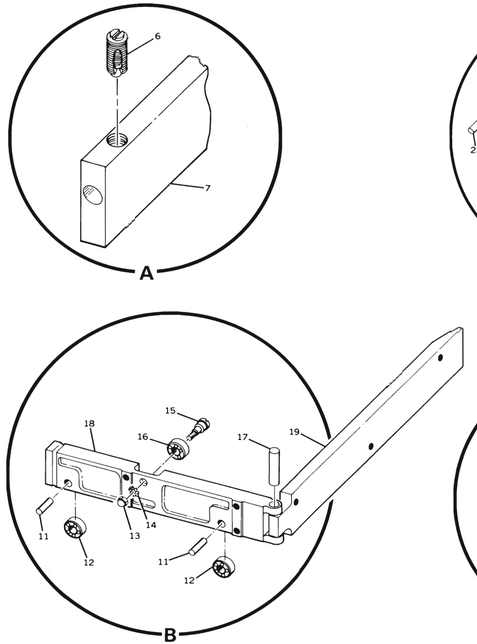


Figure 6-1. 2116C Computer, Major Replaceable Parts

Table 6-2. A500 Door Assembly (02116-63219), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-2-	02116-63219	DOOR ASSEMBLY (A500) (5, fig. 6-1)	28480	02116-63219	1
1	2360-0192	* Screw, Machine, FH, No. 6-32, 1/4 in.	00000	OBD	10
2	1390-0107	* Button Latch	13061	B10-B1	1
		(Attaching Parts)			
3	2360-0202	* Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	1
4	0590-0077	* Nut, Self-Locking, Hexagon, No. 6-32	00000	OBD	1
		– – – x – – –			
5	4040-0431	* Air Deflector	28480	4040-0431	1
		(Attaching Parts)			
6	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
7	3050-0228	* Washer, Flat, No. 6	00000	OBD	6
8	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	6
9	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	6
		– – – x – – –			
10	0400-0082	* Grommet, Nylon	28480	0400-0082	1
11	1400-0741	* Cable Clamp, Base	28480	1400-0741	1
		(Attaching Parts)			
12	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
13	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
		– – – x – – –			
14	0400-0082	* Grommet, Nylon	28480	0400-0082	1
15	02116-0101	* Subpanel	28480	02116-0101	1
15A	02116-63258	* Cable Assembly (A101)	28480	02116-63258	1
16	02116-6290	* Cable Assembly (A102)	28480	02116-6290	1
	02116-6291	* Cable Assembly (A103) (not shown in fig. 6-2)	28480	02116-6291	1
	02116-6292	* Cable Assembly (A104) (not shown in fig. 6-2)	28480	02116-6292	1
	02116-6293	* Cable Assembly (A105) (not shown in fig. 6-2)	28480	02116-6293	1
	02116-6294	* Cable Assembly (A106) (not shown in fig. 6-2)	28480	02116-6294	1
17	2140-0035	* Lamp, Incandescent, 6.3V, 0.75A	71744	1775	86
		(DS1 thru DS 86)			
18	3101-0973	* Switch, Slide, dpdt, 125V, 0.5A, ac/dc	79727	G126-0018	3
		(S111, S112, S113)			
19	02116-6043	* Display Board (A501)	28480	02116-6043	1
		(Attaching Parts)			
20	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	12
21	2190-0108	* Washer, Lock, split, No. 4	00000	OBD	12
22	3050-0222	* Washer, Flat, No. 4	00000	OBD	12
		– – – x – – –			
23	1390-0179	* Lock and Key	74842	D5416J	1
		(Attaching Parts)			
24	No Number	* Screw, Machine, RH (furnished with item 23)			1
25	No Number	* Washer, Lock, int-tooth (furnished with item 23)			1
26	02116-20831	* Latch (furnished with item 23)	28480	02116-20831	1
27	02116-2079	* Spacer	28480	02116-2079	1
		– – – x – – –			
28	0404-0371	* Trim Strip, Right	28480	0404-0371	1
29	0404-0247	* Trim Strip	28480	0404-0247	2
30	0404-0248	* Trim Strip, Left	28480	0404-0248	1
31	1400-0124	* Cable Clamp	00000	OBD	5
		(Attaching Parts)			
32	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	5
33	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	5
34	3050-0228	* Washer, Flat, No. 6	00000	OBD	5
		– – – x – – –			
35	02116-0102	* Cable Clamp Bracket	28480	02116-0102	1
		(Attaching Parts)			
	2360-0200	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		– – – x – – –			

Table 6-2. A500 Door Assembly (02116-63219), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-2-					
36	0460-0020	* Adhesive Cork	28480	0460-0020	1
37	02116-2022	* Vertical Brace	28480	02116-2022	1
38	02116-2078	* Vertical Brace	28480	02116-2078	1
		(Attaching Parts for items 37 and 38)			
	2360-0200	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	6
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	6
		– – – x – – –			
39	02116-2021	* Horizontal Brace	28480	02116-2021	1
		(Attaching Parts)			
	2360-0200	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
40	02116-01104	* Top Door Panel	28480	02116-01104	1
41	02116-0007	* Panel Brace	28480	02116-0007	1
		(Attaching Parts)			
42	2360-0204	* Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	4
43	3050-0228	* Washer, Flat, No. 6	00000	OBD	4
44	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
45	02116-2027	* Vertical Bracket	28480	02116-2027	2
		(Attaching Parts)			
46	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	4
	3050-0228	* Washer, Flat, No. 6	00000	OBD	4
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
		– – – x – – –			
47	02116-2026	* Horizontal Bracket	28480	02116-2026	2
		(Attaching Parts)			
48	2360-0205	* Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	8
49	3050-0228	* Washer, Flat, No. 6	00000	OBD	8
50	3050-0228	* Washer, Flat, No. 6	00000	OBD	8
51	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	8
52	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	8
		– – – x – – –			
53	02116-0007	* Panel Brace	28480	02116-0007	1
54	02116-4002	* Light Mask	28480	02116-4002	1
55	02116-83232	* Sheet, Light Diffusion	28480	02116-83232	1
56	4320-0096	* Extrusion, rubber	28480	4320-0096	1
57	02116-83231	* Window, Display	28480	02116-83231	1
58	No Number	* Control Panel Assembly (A502) (see fig. 6-3)		NSR	1
59	02116-2005	* Bezel, Upper	28480	02116-2005	1
60	02116-2052	* Bezel, Lower	28480	02116-2052	1
		(Attaching Parts for items 59 and 60)			
61	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	8
		– – – x – – –			
62	4320-0043	* Channel, rubber	28480	4320-0043	1
63	02116-6295	* Door Frame	28480	02116-6295	1

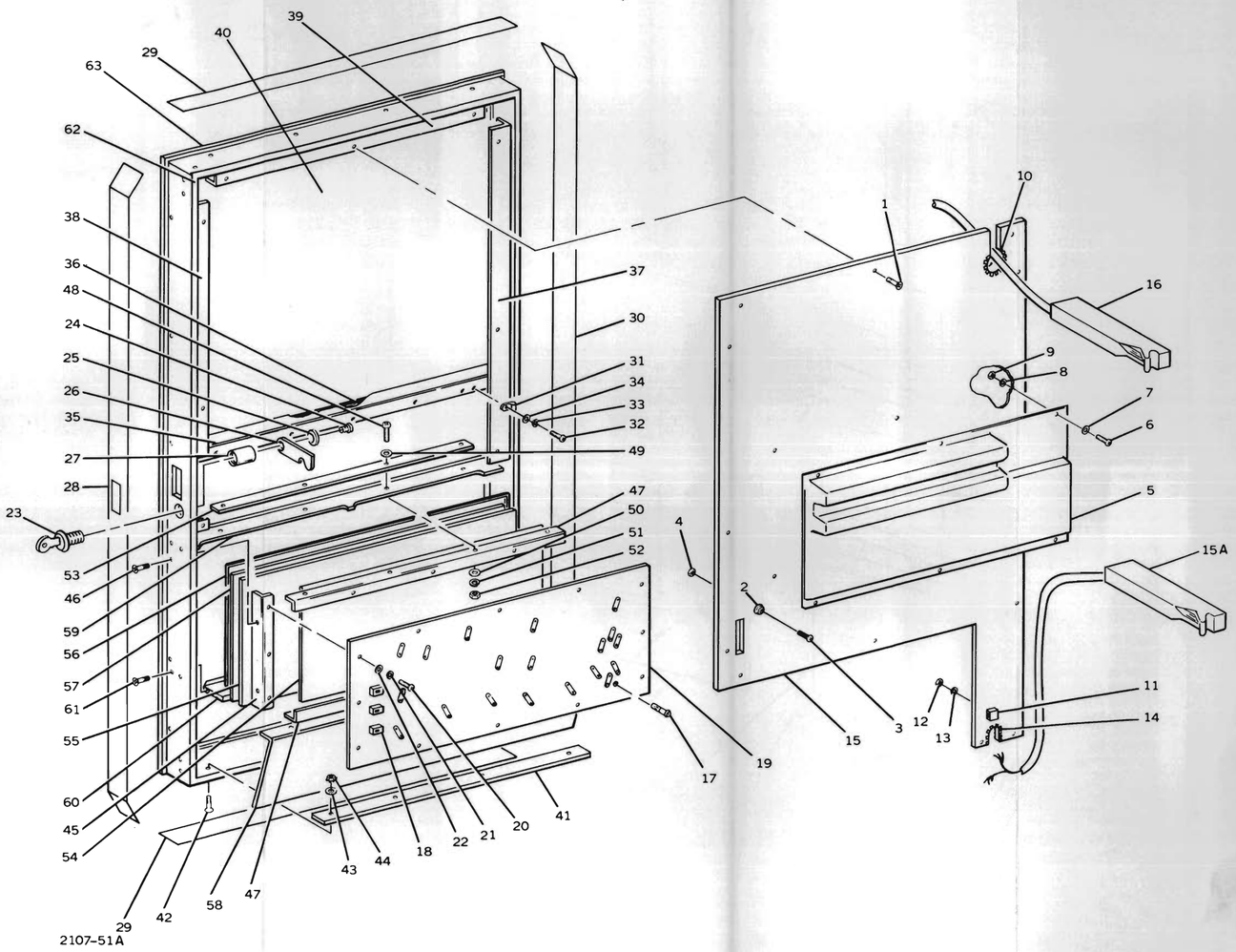


Figure 6-2. A500 Door Assembly (02116-63219), Replaceable Parts

Table 6-3. A502 Control Panel Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-3-	No Number	CONTROL PANEL ASSEMBLY (A502) (58, fig. 6-2)		NSR	1
1	1400-0127	* Cable Clamp	00000	OBD	1
		(Attaching Parts)			
2	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	1
3	2190-0006	* Washer, Lock, split, No. 6	00000	OBD	1
4	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
		– – – x – – –			
5	0360-0268	* Terminal Lug, No. 6	00000	OBD	1
		(Attaching Parts)			
6	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
		– – – x – – –			
7†	3101-0005	* Switch, Toggle, dpdt, 125V, 6A (S109)	28480	3101-0005	1
		(Attaching Parts)			
8†	2190-0102	* Washer, Lock, int-tooth (furnished with item 10)	28480	2190-0102	1
9†	2950-0035	* Nut, Plain, Hexagon (furnished with item 10)	28480	2950-0035	1
10†	0590-0012	* Nut, Plain, Knurled	28480	0590-0012	1
		– – – x – – –			
11†	3101-0718	* Lens (PRESET)	28480	3101-0718	1
12†	3101-0716	* Lens (RUN)	28480	3101-0716	1
13†	3101-0721	* Lens (HALT)	28480	3101-0721	1
14†	3101-0723	* Lens (LOAD MEMORY)	28480	3101-0723	1
15†	3101-0724	* Lens (LOAD A)	28480	3101-0724	1
16†	3101-0722	* Lens (LOAD B)	28480	3101-0722	1
17†	3101-0717	* Lens (LOAD ADDRESS)	28480	3101-0717	1
18†	3101-0725	* Lens (DISPLAY MEMORY)	28480	3101-0725	1
19†	3101-0720	* Lens (SINGLE CYCLE)	28480	3101-0720	1
20†	3101-0715	* Switch, Lighted Pushbutton (S100 thru S108)	28480	3101-0715	9
		(Attaching Parts)			
21	No Number	* Washer, Lock, int-tooth (furnished with item 20)			1
22	No Number	* Nut, Plain, Hexagon (furnished with item 20)			1
		– – – x – – –			
23	2140-0035	* Lamp, Incand, 6V, 0.04A (DS106 thru DS108)	71744	345	3
24†	02116-01114	* Subpanel	28480	02116-01114	1
		(Attaching Parts)			
25	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	1
26	2190-0006	* Washer, Lock, split, No. 6	00000	OBD	1
		– – – x – – –			
27	3101-1051	* Switch, Toggle, spst, 125V, 3A (S1 thru S16,S116)	88140	8908K507	17
		(Attaching Parts)			
28	3130-0130	* Nut, Face, 1/2 in. ID	28480	3130-0130	17
29	2190-0043	* Washer, Lock, int-tooth, 1/2 in. ID	00000	OBD	17
30	2950-0035	* Nut, Plain, Hexagon, 15/32-32	00000	OBD	17
		– – – x – – –			
31†	02116-01115	* Front Panel	28480	02116-01115	1
		– – – x – – –			
32††	3101-0719	* Lens (POWER)	28480	3101-0719	1
33††	2140-0035	* Lamp, Incand, 6V, 0.04A (DS109)	71744	345	1
34††	0362-0188	* Cover, Power Switch	28480	0362-0188	1
35††	3101-0714	* Switch, Lighted Pushbutton (S109)	28480	3101-0714	1
		(Attaching Parts)			
36††	No Number	* Washer, Lock, int-tooth (furnished with item 33)			1
37††	No Number	* Nut, Plain, Hexagon (furnished with item 33)			1
		– – – x – – –			
38††	02116-0080	* Subpanel (partially shown)	28480	02116-0080	1
39††	02116-0005	* Front Panel (partially shown)	28480	02116-0005	1

†Applies to late model computers with serial number prefix 980– only.
††Applies to early model computers with serial number prefix 980– only.

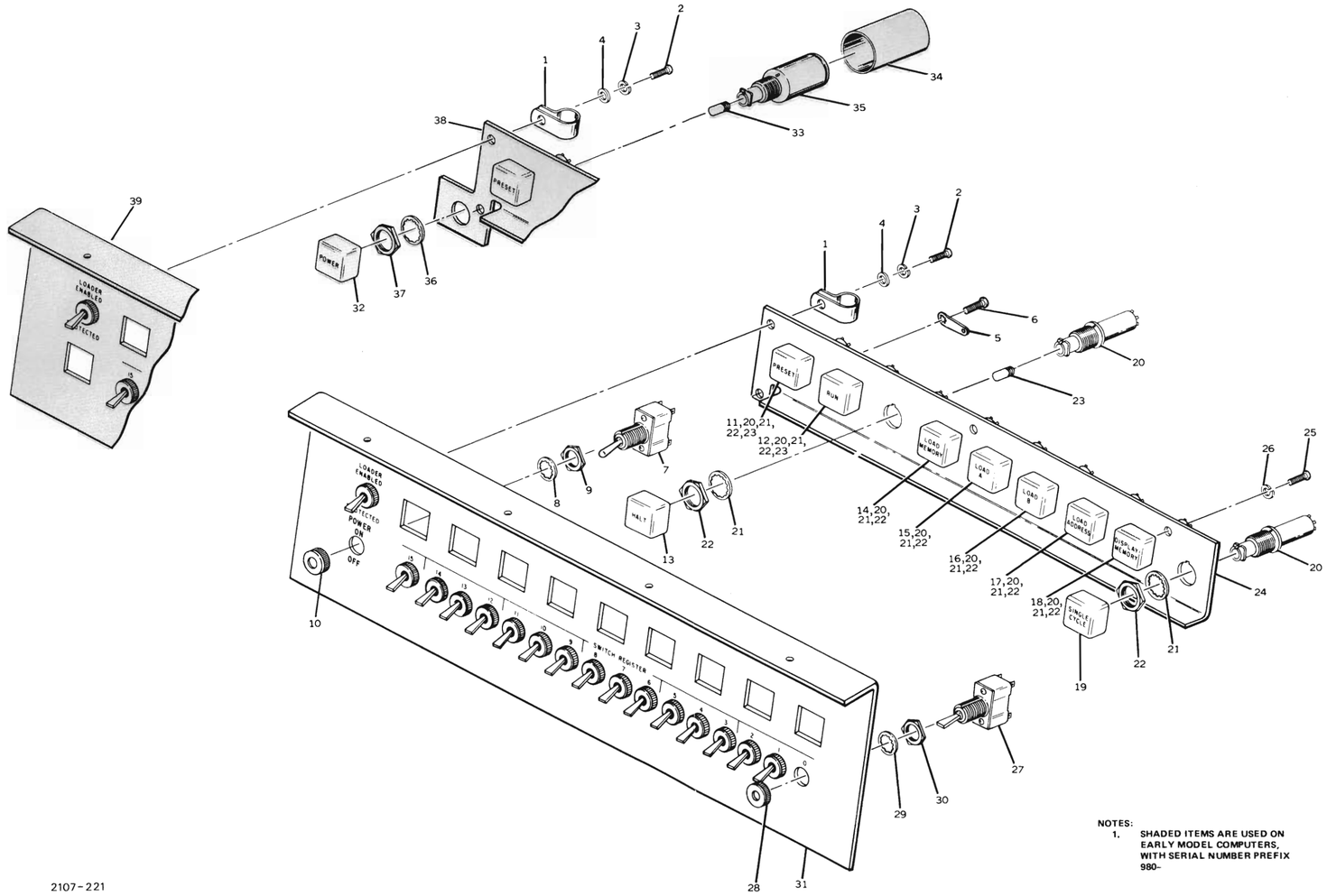


Figure 6-3. A502 Control Panel Assembly, Replaceable Parts

Table 6-4. Card Cage Assembly (02116-63223), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-4-	02116-63223	CARD CAGE ASSEMBLY (22, fig. 6-1)	28480	02116-63223	1
1	02116-6175	* Power Fail Interrupt Card (A6) (see table 7-11)	28480	02116-6175	1
2	02116-63248	* Memory Data Buffer Card (A13) (see table 7-27)	28480	02116-63248	1
3	02116-63212	* Memory Address Decoder Card (A14) (see table 7-29)	28480	02116-63212	1
4	02116-63207	* Sense Amplifier Card (A20) (see Note 1)	28480	02116-63207	Note 2
4 (Note 2)	5060-8320	* Sense Amplifier Card (A20) (see Note 1)	28480	5060-8320	1
5	02116-63211	* X-Y Driver/Switch Card (A21) (see table 7-21)	28480	02116-63211	1
6	02116-63210	* Inhibit Driver Card (A22) (see table 7-16)	28480	02116-63210	1
7	02116-63244	* Connector Assembly	28480	02116-63244	2
8	02116-0085	* Card Retainer	28480	02116-0085	1
9	02116-2080	* Door Catch	28480	02116-2080	1
10	02116-6047	* Resistance Load Card (A218) (see table 7-54)	28480	02116-6047	1
11	1400-0126	* Cable Clamp	00000	OBD	1
		(Attaching Parts)			
	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	1
	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
	2190-0006	* Washer, Lock, split, No. 6	00000	OBD	1
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	1
		– – – x – – –			
12	8120-1214	* Ground Cable, 27.5 in.	28480	02116-2080	1
13	02116-6194	* I/O Address Card (A202) (see table 7-52)	28480	02116-6194	1
14	02116-6041	* I/O Control Card (A201) (see table 7-50)	28480	02116-6041	1
15	02116-6029	* Shift Card (A108) (see table 7-44)	28480	02116-6029	1
16	02116-6027	* Instruction Decoder Card (A107) (see table 7-42)	28480	02116-6027	1
17	02116-63220	* Timing Generator Card (A106) (see table 7-40)	28480	02116-63220	4
18	02116-6026	* Arithmetic Card (A102 thru A105) (see table 7-38)	28480	02116-6026	1
19	02116-6208	* Front Panel Coupler Card (A101) (see table 7-33)	28480	02116-6208	1
20	02116-01112	* Plate, Top	28480	02116-01112	1
		(Attaching Parts)			
21	2510-0103	* Screw, Machine, FH, No. 8-32, 3/8 in.	00000	OBD	3
		– – – x – – –			
22	02116-0089	* Top Panel	28480	02116-0089	1
		(Attaching Parts)			
23	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	6
24	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	6
25	3050-0139	* Washer, Flat, No. 8	00000	OBD	6
		– – – x – – –			
26	3103-0004	* Thermostat Switch (A100S1)	28480	3103-0004	1
27	02116-0033	* Switch Bracket	28480	02116-0033	1
		(Attaching Parts)			
28	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
29	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	2
30	3050-0139	* Washer, Flat, No. 8	00000	OBD	2
		– – – x – – –			
31	0811-2031	* Resistor, Fxd, WW, 815 ohms, 3.0%, 1/4W (A100R220)	01686	7010	1
32	0360-0279	* Standoff	00000	OBD	2
		(Attaching Parts)			
	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
	2190-0108	* Washer, Lock, split, No. 4	00000	OBD	2
		– – – x – – –			
33	02116-0088	* Filler Plate	28480	02116-0088	2
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	8
	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	8
	3050-0139	* Washer, Flat, No. 8	00000	OBD	8
		– – – x – – –			

Note 1. These cards must not be repaired by the customer. Field removal or replacement of any component voids the warranty on the card.
2. Part number 02116-63207 is interchangeable with part number 5060-8320.

Table 6-4. Card Cage Assembly (02116-63223), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-4-					
34	02116-63228	* Overvoltage Protection Assembly (A121) (see fig. 6-5)	28480	02116-63228	1
		(Attaching Parts)			
	2360-0196	* Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	4
	2190-0047	* Washer, Recessed, No. 6	00000	OBD	4
		– – – x – – –			
35	02116-2072	* Support Bar	28480	02116-2072	1
		(Attaching Parts)			
	2530-0017	* Screw, Machine, FH, No. 8-32, 1/4 in.	00000	OBD	2
	2190-0048	* Washer, Recessed, No. 8	00000	OBD	2
		– – – x – – –			
36	0360-1255	* Terminal Board (A100TB1, A100TB2)	00000	OBD	2
		(Attaching Parts)			
37	2370-0030	* Screw, Machine, FH, No. 6-32, 1-1/2 in.	00000	OBD	2
38	2190-0047	* Washer, Recessed, No. 6	00000	OBD	2
39	0380-0002	* Spacer, 1/4 in.	00000	OBD	2
40	2420-0001	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
		– – – x – – –			
41	02116-0032	* Bottom Panel	28480	02116-0032	1
		(Attaching Parts)			
42	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
43	2190-0017	* Washer, Lock, split. No. 8	00000	OBD	4
44	2580-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
		– – – x – – –			
45	02116-2040	* Bezel	28480	02116-2040	1
		(Attaching Parts)			
46	2510-0102	* Screw, Machine, FH, No. 8-32, 3/8 in.	00000	OBD	18
		– – – x – – –			
47	No Number	* Card Rack Assembly		NSR	4
		(Attaching Parts)			
48	2360-0200	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	16
49	2190-0147	* Washer, Recessed, No. 6	00000	OBD	16
		– – – x – – –			
50	02116-2075	** PC Guide Support	28480	02116-2075	2
51	02116-4007	** PC Guide	28480	02116-4007	22
52	02116-8199	* Indicator, Strip, Top	28480	02116-8199	1
53	02116-8200	* Indicator, Strip, Middle	28480	02116-8200	1
54	02116-8201	* Indicator, Strip, Bottom	28480	02116-8201	1
55	0360-1264	* Terminal Lug	28480	0360-1264	2
56	0360-1260	* Terminal Lug	28480	0360-1260	7
57	0360-1256	* Terminal Board (A200TB1)	28480	0360-1256	1
		(Attaching Parts)			
	2360-0205	* Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
58	3160-0099	* Fan Grille	23936	5504	3
		(Attaching Parts)			
59①	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	12
59②	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	12
60①	3050-0139	* Washer, Flat, No. 8	00000	OBD	12
60②	3050-0228	* Washer, Flat, No. 6	00000	OBD	12
61①	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	12
61②	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	12
		– – – x – – –			
62①	3610-0072	* Fan Assembly, 115V, 60 Hz (A200B1, B2, B3)	28480	3160-0072	3
62②	3160-0224	* Fan Assembly, 115V, 60 Hz (A200B1, B2, B3)	28480	3160-0224	3
		(Attaching Parts)			

Table 6-4. Card Cage Assembly (02116-63223), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-4-					
63①	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	12
63②	2360-0205	* Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	12
64	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	12
		– – – x – – –			
②	8120-1478	* Cable Assembly (Not shown in figure 6-4)	28480	8120-1478	3
65	02116-0010	* Fan Panel	28480	02116-0010	1
		(Attaching Parts)			
66	2510-0106	* Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	4
67	2190-0048	* Washer, Recessed, No. 8	00000	OBD	4
	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	4
	2580-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
68	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	3
	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	3
	2580-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	3
		– – – x – – –			
69	02116-01111	* Side Panel, Right	28480	02116-01111	1
70	02116-01110	* Side Panel, Left	28480	02116-01110	1
		(Attaching Parts for items 69 and 70)			
71	2530-0017	* Screw, Machine, FH, No. 8-32, 1/4 in.	00000	OBD	12
72	2190-0048	* Washer, Recessed, No. 8	00000	OBD	12
		– – – x – – –			
73③	02116-01126	* Filler Plate, small	28480	02116-01126	1
74③	02116-01125	* Filler Plate, large	28480	02116-01125	1
75	02116-6282	* Back Panel Assembly, Card Cage	28480	02116-6282	1
76	No Number	** Connector Pin	00779	67628-2	AR
77	3050-0238	** Washer, Nonmetallic, shouldered, No. 8	00000	OBD	4

① Used on computers with serial number prefix below 1108A.
② First used on computers with serial number prefix 1108A.
③ Back panel assemblies may be equipped with either spare connectors or filler plates.

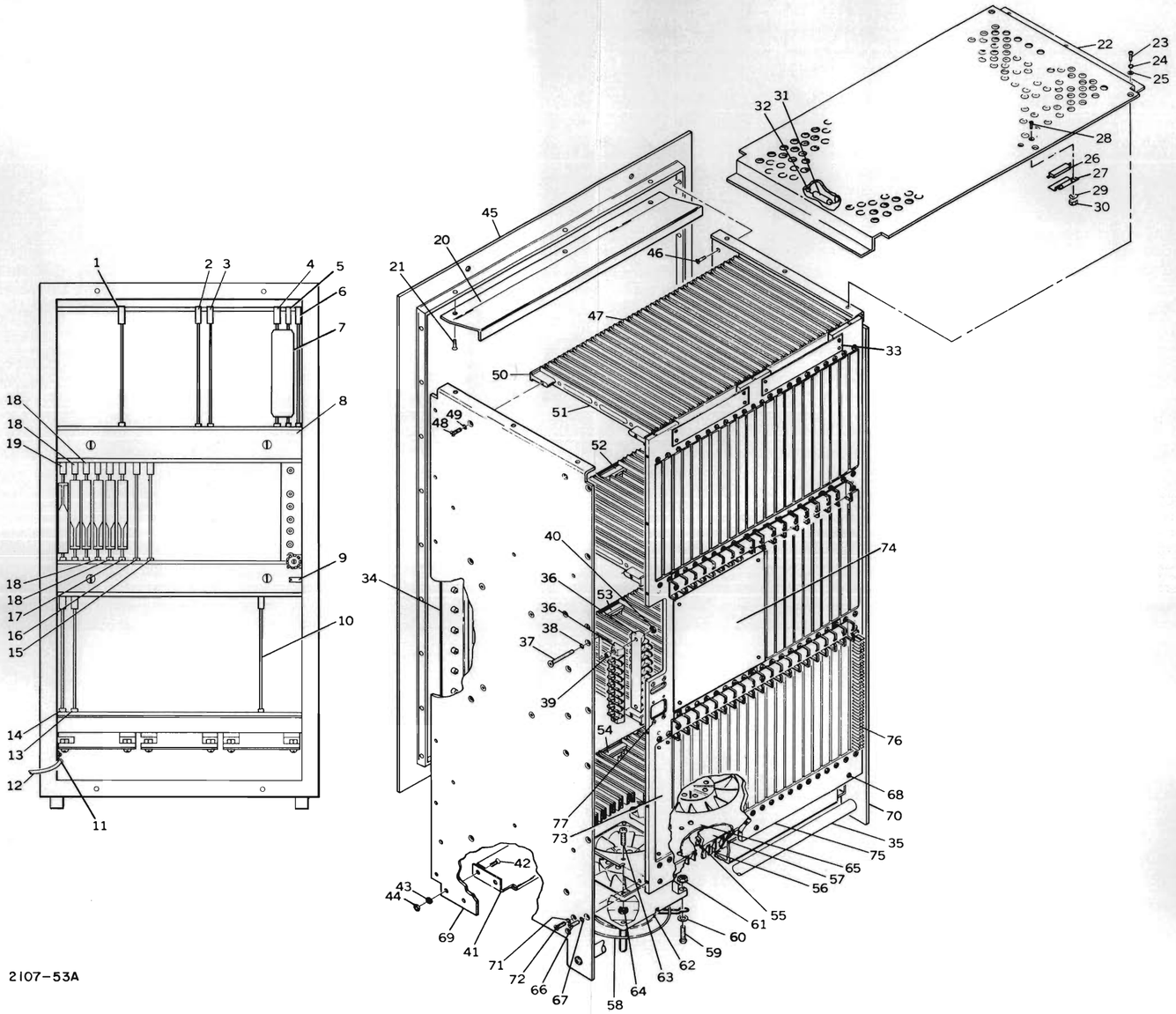


Figure 6-4. Card Cage Assembly (02116-63223), Replaceable Parts

Table 6-5. A121 Overvoltage Protection Assembly (02116-63218), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-5-	02116-63218	OVERVOLTAGE PROTECTION ASSEMBLY (A121) (34, figure 6-4)	28480	02116-63218	1
1	1251-0367	* Jack, Tip (TP1 thru TP8)	28480	1251-0367	7
2	4320-0002	* Gasket, rubber	28480	4320-0002	1
3	02116-01108	* Cover, Overvoltage Protection Assembly	28480	02116-01108	1
		(Attaching Parts)			
4	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	6
5	2190-0017	* Washer, Lock, split, No. 8	00000	OBD	6
		- - - x - - -			
6	02116-63213	* Overvoltage, Component Board Assembly (see fig. 6-6)	28480	02116-63213	1
		(Attaching Parts)			
7	2360-0109	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	4
8	2190-0007	* Washer, Lock, int-tooth, No. 6	00000	OBD	4
9	3050-0247	* Washer, Nonmetallic, No. 6	00000	OBD	4
		- - - x - - -			
10	1901-0343	* Diode, Si, 50 PIV, 18A, (CR2, CR4, CR14)	04713	IN3491R	3
11	1902-1228	* Diode, Breakdown, 27V, 10%, 10W (CR3)	28480	1902-1228	1
		(Attaching Parts)			
12	1200-0080	* Washer, Flat, Anodized, No. 10	28480	1200-0080	2
13	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
14	3050-0270	* Terminal Lug, No. 10	00000	OBD	1
15	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			
16	1884-0046	* Thyristor, SCR, 50V, 25A (Q1, Q2)	28480	1884-0046	2
		(Attaching Parts)			
17	1200-0088	* Washer, Flat, Anodized	28480	1200-0088	4
18	3050-0225	* Washer, Flat, 1/4 ID	00000	OBD	2
19	0360-0271	* Terminal Lug, 1/4 ID	00000	OBD	2
20	2950-0036	* Nut, Plain, Hexagon, 1/4-28	00000	OBD	2
		- - - x - - -			
21	1902-1205	* Diode, Breakdown, 15V, +2% (CR1)	04713	IN2979RB	1
		(Attaching Parts)			
22	1200-0080	* Washer, Flat, Anodized, No. 10	28480	1200-0080	2
23	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
24	3050-0270	* Terminal Lug, No. 10	00000	OBD	1
25	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			
26	02116-2060	* Mounting Bar, Front	28480	02116-2060	1
27	1902-1217	* Diode, Breakdown, 6.2V, 5% (CR13)	04713	SZ11746	1
		(Attaching Parts)			
28	1200-0080	* Washer, Flat, Anodized, No. 10	28480	1200-0080	2
29	3050-0226	* Washer, Flat, No. 10	00000	OBD	1
30	3050-0270	* Terminal Lug, No. 10	00000	OBD	1
31	2470-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
		- - - x - - -			
32	1901-0406	* Diode, Si, 50PIV, 18A (CR5, CR7, CR9)	04713	IN3491MR-322	3
33	1880-0047	* Thyristor, SCR, 25V, 55A (Q6)	28480	1884-0047	1
		(Attaching Parts)			
34	1200-0089	* Washer, Flat, Anodized	28480	1200-0089	2
35	0362-0128	* Crimp Lug, Termination	00000	OBD	1
36	0360-1089	* Terminal Lug, 1/2 in. ID	00000	OBD	1
37	2190-0043	* Washer, Lock, split, 1/2 in. ID	00000	OBD	1
38	2950-0024	* Nut, Plain, Hexagon, 1/2-20	00000	OBD	1
		- - - x - - -			

Table 6-5. A121 Overvoltage Protection Assembly (02116-63218), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-5-					
39	02116-2059	* Mounting Bar, Upper	28480	02116-2059	1
		(Attaching Parts)			
40	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
41	2190-0851	* Washer, Lock, split, 1/2 in. ID	00000	OBD	2
		- - - x - - -			
42	1884-0047	* Thyristor, SCR, 25V, 55A (Q5)	28480	1884-0047	1
		(Attaching Parts)			
43	0362-0128	* Crimp Lug, Termination	00000	OBD	1
44	0360-1089	* Terminal Lug, 1/2 in. ID	00000	OBD	1
45	2190-0043	* Washer, Lock, split, 1/2 in. ID	00000	OBD	1
46	2950-0024	* Nut, Plain, Hexagon, 1/2-20	00000	OBD	1
		- - - x - - -			
47	02116-2064	* Mounting Bar, Lower	28480	02116-2064	1
		(Attaching Parts)			
48	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
49	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	2
		- - - x - - -			
50	1884-0046	* Thyristor, SCR, 50V, 25A (Q3, Q4)	28480	1884-0046	2
		(Attaching Parts)			
51	2190-0070	* Washer, Lock, ext-tooth, 1/4 in. ID	00000	OBD	2
52	2950-0036	* Nut, Plain, Hexagon, 1/4-28	00000	OBD	2
		- - - x - - -			
53	1902-1205	* Diode, Breakdown, 15V, +2% (CR6)	04713	IN2979RB	1
		(Attaching Parts)			
54	2740-0003	* Nut, Assembled Washer, No. 10-32	00000	OBD	1
		- - - x - - -			
55	1902-1228	* Diode, Breakdown, 27V, 10W, 5% (CR8)	28480	1902-1228	1
		(Attaching Parts)			
56	2740-0003	* Nut, Assembled Washer, No. 10-32	00000	OBD	1
		- - - x - - -			
57	02116-2061	* Mounting Bar, Rear	28480	02116-2061	1

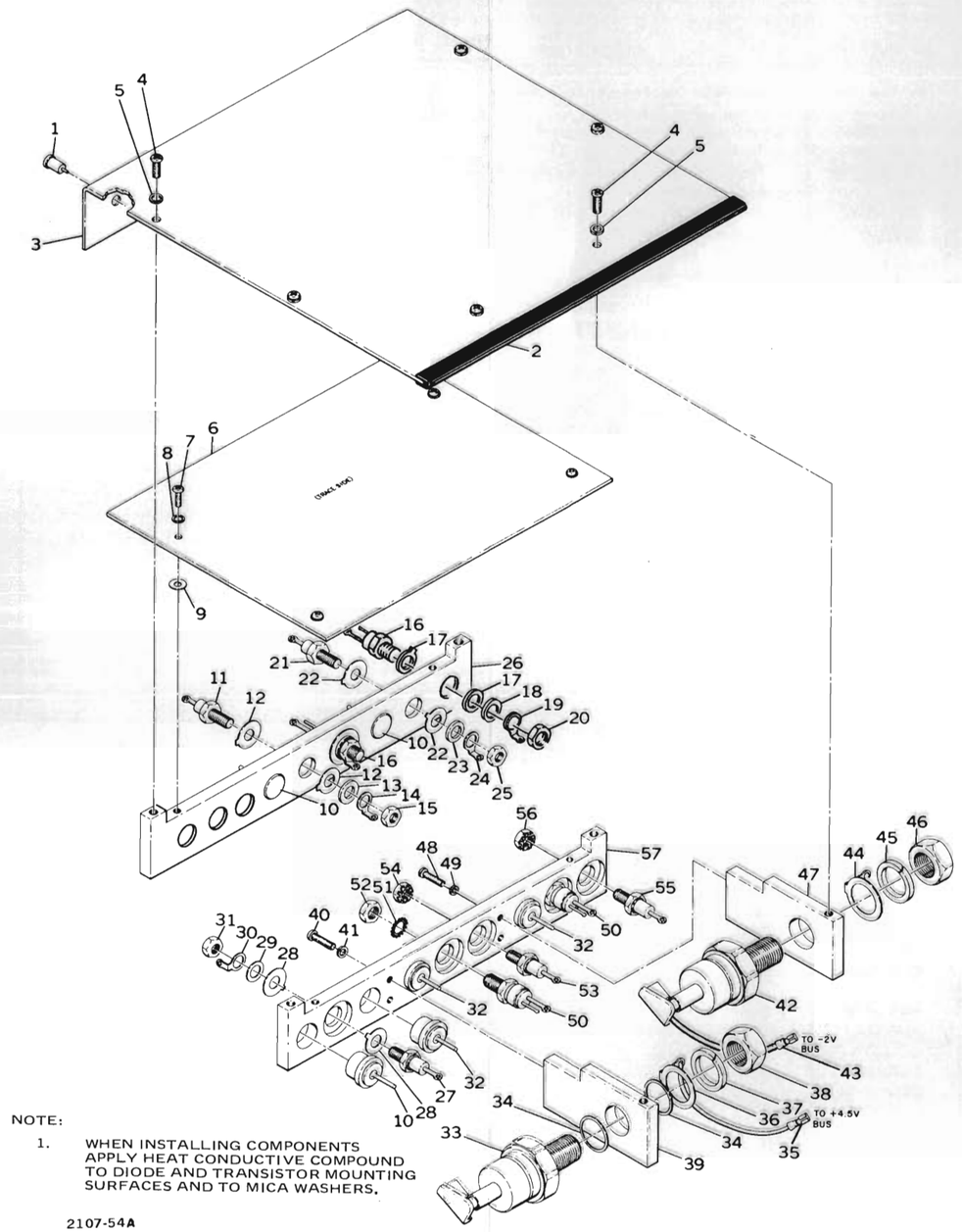


Figure 6-5. A121 Overvoltage Protection Assembly (02116-63218), Replaceable Parts

Table 6-6. A121A1 Overvoltage Component Board Assembly (02116-63213), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-6-	02116-63213	OVERVOLTAGE COMPONENT BOARD ASSEMBLY (A121A1) (6, fig. 6-5)	28480	02116-63213	1
1	0160-2055	* Capacitor, Fxd, Cer, 0.01 uF, +80 -20% 100 VDCW (C1 thru C6)	56289	CO23F101F103-ZE12-CDH	6
2	0689-1505	* Resistor, Fxd, Comp, 15 ohms, 5%, 1W (R20,R21)	01121	GB1505	2
3	0698-3315	* Resistor, Fxd, Comp, 220 ohms, 5%, 1W (R19,22)	01121	EB2215	2
4	1901-0191	* Diode, Si, 0.75A, 100 PIV (CR10, CR11, CR12)	04713	SR1358-2	3
5	0813-0038	* Resistor, Fxd, WW, 0.5 ohms, 10%, 5W (R3, R4, R7, R8, R10, R11, R15, R16)	28480	0813-0038	8
6	0686-2205	* Resistor, Fxd, Comp, 22 ohms, 5%, 1W (R1, R5, R13, R18)	01121	EB2205	4
7	0686-4715	* Resistor, Fxd, Comp, 470 ohms, 5%, 1W (R2, R6, R12, R17)	01121	EB4715	4
8	0811-1857	* Resistor, Fxd, WW, 400 ohms, 5%, 5W (R9, R14)	28480	0811-1857	2

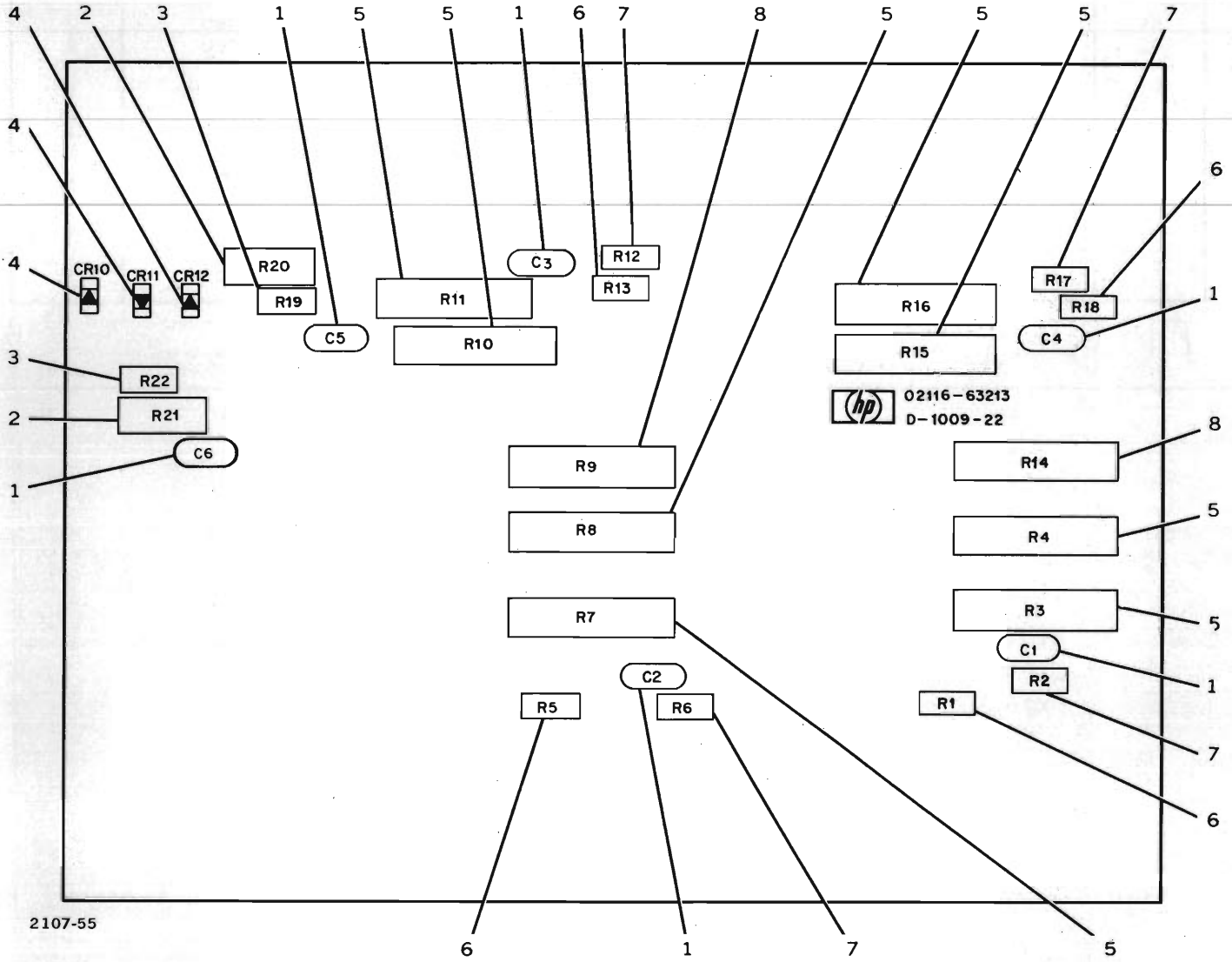


Figure 6-6. A121A1 Overvoltage Component Board Assembly (02116-63213), Replaceable Parts

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-63217), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-7-	02116-63217	POWER SUPPLY AND BACK PANEL ASSEMBLY (A300) (55, fig. 6-1)	28480	02116-63217	1
1	02116-63242	* Component Board Assembly (A307) (see fig. 6-10)	28480	02116-63242	1
		(Attaching Parts)			
	2360-0207	* Screw, Machine, PH, No. 6-32, 7/8 in.	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	2
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
		– – – x – – –			
2	02116-63229	* Component Board Assembly (A306) (see fig. 6-10)	28480	02116-63229	1
		(Attaching Parts)			
	2360-0207	* Screw, Machine, PH, No. 6-32, 7/8 in.	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	2
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
		– – – x – – –			
3	3160-0099	* Grille, Fan	23936	5504	1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
	2580-0003	* Nut, Assembled Washer, No. 8	00000	OBD	4
		– – – x – – –			
4 ①	3160-0072	* Fan Assembly, 115V, 60 Hz (A300B1)	28480	3160-0072	1
4 ②	3160-0224	* Fan Assembly, 115V, 60 Hz (A300B1)	28480	3160-0224	1
		(Attaching Parts)			
4A①	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	4
4A②	2360-0206	* Screw, Machine, FH, No. 6-32, 7/8 in.	00000	OBD	2
②	2190-0047	* Washer, Recessed, No. 6	00000	OBD	2
①	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	4
②	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
4B②	0624-0284	* Screw, Tapping, Thread Cutting, No. 6	00000	OBD	2
		– – – x – – –			
4C②	5000-8015	* Fan Guard	28480	5000-8015	1
②	8120-1478	* Cable Assembly (Not shown in figure 6-7)	28480	8120-1478	1
5	2200-0141	* Screw, Machine, PH, No. 4-40, 5/16 in.	00000	OBD	1
6	2190-0003	* Washer, Lock, split, No. 4	00000	OBD	1
7	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	1
8	2190-0108	* Washer, Lock, split, No. 4	00000	OBD	1
9	5020-1922	* Spacer, Nylon	28480	5020-1922	1
10	2200-0144	* Screw, Machine, FH, No. 4-40, 3/8 in.	00000	OBD	3
11	02116-0074	* Bus Bar Brace	28480	02116-0074	1
12	02116-2069	* Bakelite Space	28480	02116-2069	2
13	02116-0075	* Bus Bar Brace	28480	02116-0075	1
		(Attaching Parts)			
	2360-0204	* Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	2
		– – – x – – –			
14	02116-2056	* Bus Bar, -2V	28480	02116-2056	1
15	02116-0093	* Bus Bar (End Output)	28480	02116-0093	1
16	02116-2055	* Bus Bar, 4.5V	28480	02116-2055	1
17	02116-0077	* Side Bracket	28480	02116-0077	2
		(Attaching Parts)			
18	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	4
19	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	4
		– – – x – – –			
20	02116-63241	* Component Board Assembly (A310) (see fig. 6-10)	28480	02116-63241	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	2
		– – – x – – –			

① Used on computers with serial number prefix below 1108A.
② First used on computers with serial number prefix 1108A.

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-63217), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-7-					
21	02116-0023	* Bracket, Mounting, Bus Bar	28480	02116-0023	1
		(Attaching Parts)			
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	1
		– – – x – – –			
22	02116-2035	* Bracket, Capacitor Board, large	28480	02116-2035	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	3
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	3
	3050-0228	* Washer, Flat, No. 6	00000	OBD	3
	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	3
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	3
		– – – x – – –			
23	02166-2058	* Bracket, Capacitor Board, small	28480	02116-2058	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	2
	2360-0201	* Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		– – – x – – –			
24	02116-63214	* Memory Supply Regulator Card (A302) (see fig. 6-9)	28480	02116-63214	1
	or			or	
③	02116-63267		28480	02116-63267	–
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	1
	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
		– – – x – – –			
25	02116-6014	* Logic Supply Regulator Card (A301) (see fig. 6-8)	28480	02116-6014	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	1
	3050-0228	* Washer, Flat, No. 6	00000	OBD	1
		– – – x – – –			
26	1251-0233	* Connector, Receptacle (XA301)	28480	1251-0233	1
27	1251-0335	* Connector, Receptacle (XA302)	28480	1251-0335	1
		(Attaching Parts for items 26, 27)			
	2200-0149	* Screw, Machine, PH, No. 4-40, 5/8 in.	00000	OBD	4
	3050-0002	* Washer, Flat, No. 4	00000	OBD	4
	0590-0076	* Nut, Self-Locking, Hexagon, No. 4	00000	OBD	4
		– – – x – – –			
28	02116-63236	* Capacitor Board Assembly (A303) (see fig. 6-11)			1
		(Attaching Parts)			
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	4
		– – – x – – –			
29	02116-0047	* Capacitor Board Bracket	28480	02116-0047	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	3
		– – – x – – –			
30	02116-0025	* Deck, Blank, Power Supply	28480	02116-0025	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	5
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	5
		– – – x – – –			
31	02116-01116	* Transformer Cover	28480	02116-01116	1
		(Attaching Parts)			
32	0510-0736	* Latch, Male	28480	0510-0736	6
33	0510-0735	* Latch, Female	28480	0510-0735	6
		– – – x – – –			

③ Computers with serial number prefix 1127A and above use the Memory Supply Regulator Card with part no. 02116-63267. **These cards are not interchangeable.**

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-63217), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-7-34	0811-2140	* Resistor, Fxd, ww, 2 ohms, 5%, 5W (A300R1)	28480	0811-2140	1
		(Attaching Parts)			
	2510-0111	* Screw, Machine, PH, No. 8-32, 3/4 in.	00000	OBD	2
	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	2
		– – – x – – –			
35	02116-0022	* Left Brace	28480	02116-0022	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	3
		– – – x – – –			
36	02116-63228	* AC Input Section (A312) (see fig. 6-12)	28480	02116-63228	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	2
		– – – x – – –			
37	02116-63225	* Transformer Assembly (A311) (see fig. 6-13)	28480	02116-63225	1
		(Attaching Parts)			
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	4
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	4
		– – – x – – –			
38	02116-63238	* Small Heat Sink Assembly (A305) (see fig. 6-14)	28480	02116-63238	1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	4
	0590-0843	* Nut, Self-Locking, Hexagon, No. 8-32	00000	OBD	4
		– – – x – – –			
39	02116-63237	* Large Heat Sink Assembly (A304) (see fig. 6-16)	28480	02116-63237	1
		(Attaching Parts)			
	2510-0107	* Screw, Machine, PH, 8-32, 1/2 in.	00000	OBD	4
	0590-0843	* Nut, Self-Locking, Hexagon, No. 8-32	00000	OBD	4
		– – – x – – –			
40	02116-63235	* Component Board Assembly (A308) (see fig. 6-15)	28480	02116-63235	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	4
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	4
		– – – x – – –			
41	1251-0136	* Connector, Receptacle (XA304, XA305)	28480	1251-0136	2
		(Attaching Parts)			
	2200-0149	* Screw, Machine, PH, No. 4-40, 5/8 in.	00000	OBD	4
	3050-0222	* Washer, Flat, No. 4	00000	OBD	4
	0590-0076	* Nut, Self-Locking, Hexagon, No. 4-40	00000	OBD	4
		– – – x – – –			
42	02116-0053	* Connector Bracket	28480	02116-0053	2
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, 6-32, 3/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
43	02116-0020	* Center Brace	28480	02116-0020	1
		(Attaching Parts)			
44	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
45	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	3
		– – – x – – –			
46	02116-63240	* Component Board Assembly (A309) (see fig. 6-17)	28480	02116-63240	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	3
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	3
		– – – x – – –			

Table 6-7. A300 Power Supply and Back Panel Assembly (02116-63217), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-7-					
47	02116-2068	** Mount, Bus Bar	28480	02116-2068	1
		(Attaching Parts)			
48	2510-0063	** Screw, Machine, FH, No. 8-32, 1-1/2 in.	00000	OBD	2
		- - - x - - -			
49	02116-0056	** Bracket, Diode	28480	02116-0056	1
50	2110-0255	** Fuse Mounting Bracket	28480	2110-0255	1
51	0160-3043	* Capacitor, Fxd, Cer, 2x0.005 uF, 20%, 250 VAC (A300C1A, C1B)	56289	29C147A-CDH	1
52†	1251-2660	* Connector, Receptable (A300J1)	28480	1251-2660	1
		(Attaching Parts)			
	2200-0147	* Screw, Machine, PH, No. 4-40, 1/2 in.	00000	OBD	4
	2260-0009	* Nut, Assembled Washer, No. 4-40	00000	OBD	4
		- - - x - - -			
52A††	1251-0315	* Connector, Receptacle (A300J1)	28480	1251-0315	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
	2360-0268	* Terminal Lug, No. 6 (not shown)	00000	OBD	2
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	1
		- - - x - - -			
53	1251-0143	* Connector, Receptacle, Power (A300J2)	74868	32-2907-3	1
		(Attaching Parts)			
	0520-0103	* Screw, Machine, PH, No. 2-56, 2/8 in.	00000	OBD	2
	3050-0098	* Washer, Flat, No. 2	00000	OBD	2
	2190-0045	* Washer, Lock, split, No. 2	00000	OBD	2
	0610-0001	* Nut, Plain, Hexagon, No. 2-56	00000	OBD	2
		- - - x - - -			
54	02116-01113	* Back Panel, Power Supply	28480	02116-01113	1

† Used on Computers with serial number prefixes above 1047A.

†† Used on Computers with serial number prefixes below 1047A.

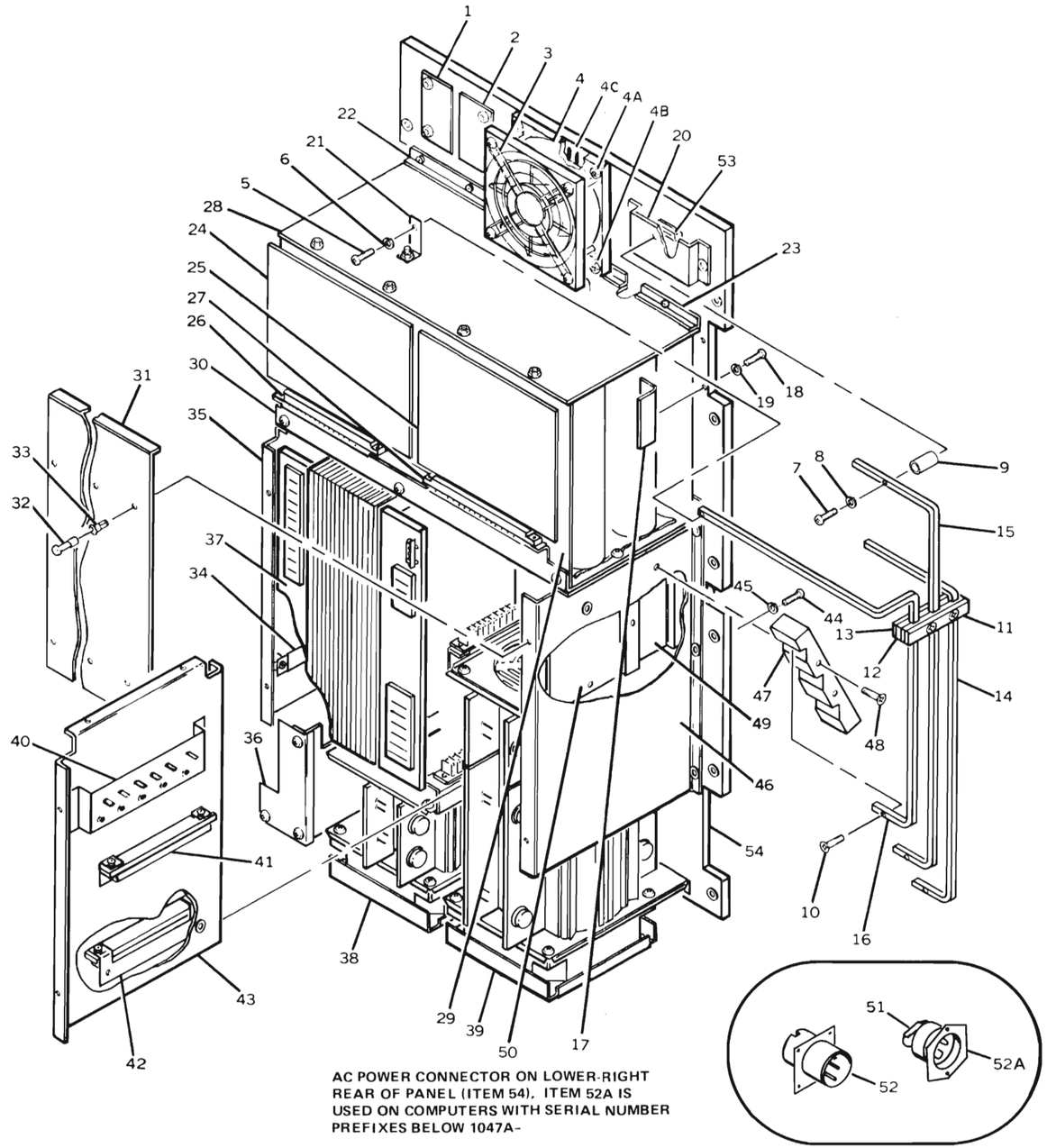


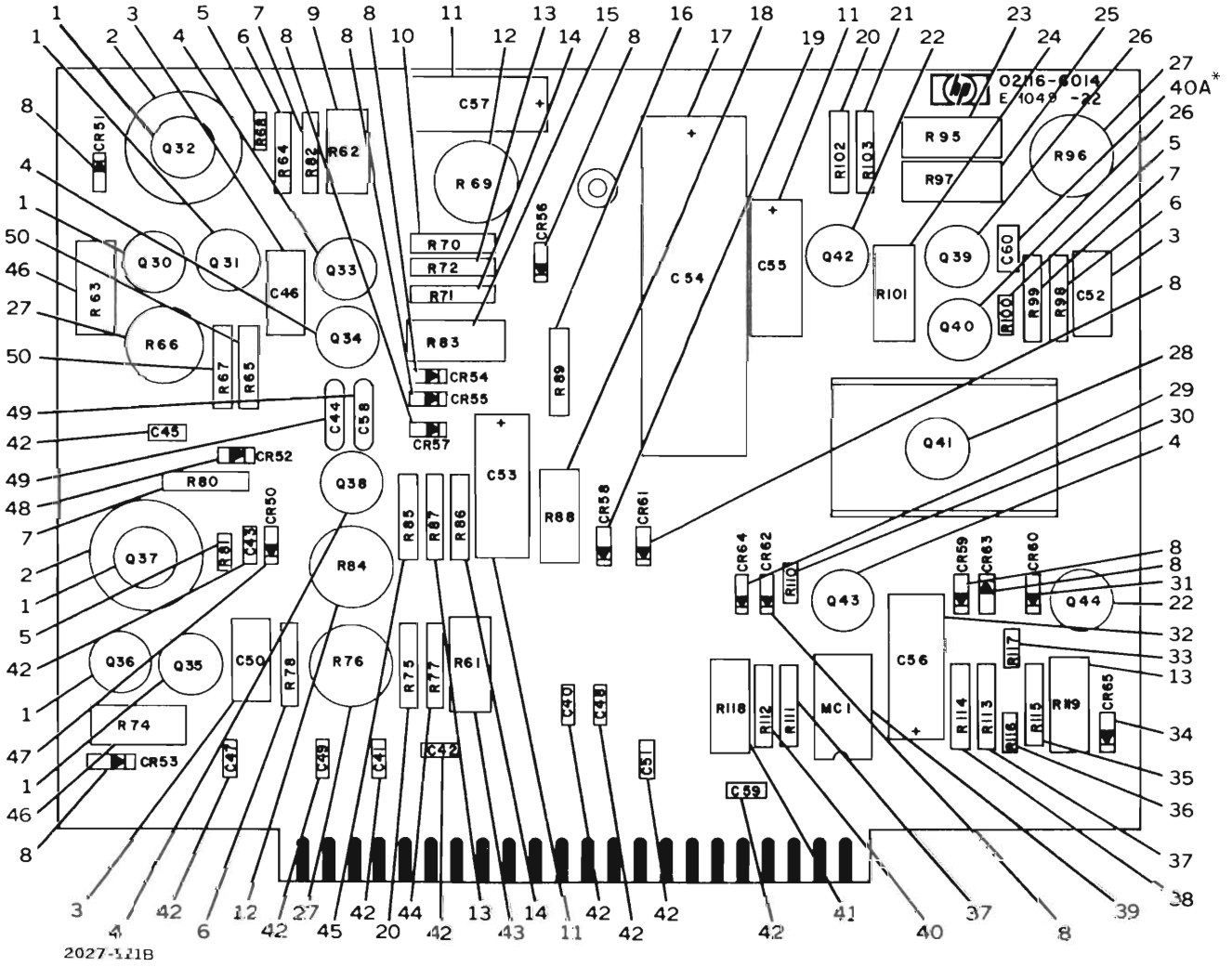
Figure 6-7. A300 Power Supply and Back Panel Assembly (02116-63217), Replaceable Parts

Table 6-8. A301 Logic Supply Regulator Card (02116-6014), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-8-	02116-6014	LOGIC SUPPLY REGULATOR CARD (A301) (25, fig. 6-7)	28480	02116-6014	1
1	1853-0001	* Transistor, Si, PNP (Q30,Q31,Q32,Q35,Q36,Q37)	28480	1853-0001	6
2	1205-0033	* Heat Sink	28480	1205-0033	2
3	0160-0163	* Capacitor, Fxd, My, 0.033 uF, 10%, 200 VDCW, (C46, C50, C52)	56289	192P33392-PTS	3
4	1850-0062	* Transistor, Ge (Q33, Q34, Q38, Q43)	01295	GA287	4
5	0757-0924	* Resistor, Fxd, Flm, 1k, 2%, 1/8W, (R68,R81,R100)	28480	0757-0924	3
6	0757-0730	* Resistor, Fxd, Flm, 750 ohms, 1%, 1/4W (R64, R78, R98)	28480	0757-0730	3
7	0757-0743	* Resistor, Fxd, Flm, 3.32k, 1%, 1/4W (R80, R82, R99)	28480	0757-0743	3
8	1901-0025	* Diode, Si, 100 mA, 1V (CR51, CR53, CR54, CR55, CR56, CR57, CR59, CR61, CR62, CR63)	07263	FD2387	10
9	0761-0068	* Resistor, Fxd, Met Ox, 510 ohms, 5%, 1W (R62)	28480	0761-0008	1
10	0757-0728	* Resistor, Fxd, Flm, 619 ohms, 1%, 1/4W (R70)	28480	0757-0728	1
11	0180-0064	* Capacitor, Fxd, Elect, 35 uF, +100 -10%, 6 VDCW (C53, C55, C57)	56289	30D15G006BB4	3
12	2100-1772	* Resistor, Var, WW, 500 ohms, 5%, (R69, R84)	28480	2100-1772	2
13	0757-0244	* Resistor, Fxd, Flm, 499 ohms, 1%, 1/4W (R72, R87, R119)	28480	0757-0244	3
14	0757-0715	* Resistor, Fxd, Flm, 150 ohms, 1%, 1/4W (R71, R86)	28480	0757-0715	2
15	0686-2215	* Resistor, Fxd, Comp, 220 ohms, 5%, 1/2W (R83)	01121	EB2215	1
16	0757-0739	* Resistor, Fxd, Flm, 2.00k, 1%, 1/4W (R89)	28480	0757-0739	1
17	0180-1867	* Capacitor, Fxd, Elect, 1600 uF, +75 -10%, 10 VDCW (C54)	28480	0180-1867	1
18	0761-0026	* Resistor, Fxd, Met Ox, 220 ohms, 5%, 1W (R88)	28480	0761-0026	1
19	1902-3079	* Diode, Breakdown, Si, 453V (CR58)	28480	1902-3079	1
20	0757-0711	* Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/4W (R75, R102)	28480	0757-0711	2
21	0698-3134	* Resistor, Fxd, Flm, 1.33k, 1%, 1/4W (R103)	28480	0811-3134	1
22	1851-0017	* Transistor, Ge, NPN (Q42, Q44)	01295	2N130A	2
23	0757-0814	* Resistor, Fxd, Flm, 511 ohms, 1%, 1/2W (R95)	28480	0757-0814	1
24	0761-0011	* Resistor, Fxd, Met Ox, 3300 ohms, 5%, 1W (R101)	28480	0761-0011	1
25	0757-0158	* Resistor, Fxd, Flm, 619 ohms, 1%, 1/2W (R97)	28480	0757-0158	1
26	1854-0003	* Transistor, Si, NPN (Q39, Q40)	28480	1854-0003	2
27	2100-1770	* Resistor, Var, WW, 100 ohms, 5% (R66, R76, R96)	28480	2100-1770	3
28	1854-0265	* Transistor, Si, NPN (Q41)	28480	1854-0265	1
29	1902-3224	* Diode, Breakdown, 17.8V, 5%, 400 mW (CR64)	28480	1902-3224	1
30	0757-0912	* Resistor, Fxd, Flm, 330 ohms, 2%, 1/8W (R110)	28480	0757-0912	1
31	1902-0184	* Diode, Breakdown, Si, 16.2V, 5%, (CR60)	28480	1902-0184	1
32	0180-1714	* Capacitor, Fxd, Elect, 330 uF, 10%, 6 VDCW (C56)	28480	0180-1714	1
33	0683-5115	* Resistor, Fxd, Comp, 510 ohms, 5%, 1/4W (R117)	01121	CB5115	1
34	1902-0017	* Diode, Breakdown, 6.81V, 10%, 400 mW (CR65)	28480	1902-0017	1
35	0757-0340	* Resistor, Fxd, Flm, 10.0k, 1%, 1/4W (R115)	28480	0757-0340	1
36	0683-1025	* Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W (R116)	01121	CB1025	1
37	0757-0338	* Resistor, Fxd, Flm, 1.00k, 1%, 1/4W (R111, R113)	28480	0757-0338	2
38	0757-0705	* Resistor, Fxd, Flm, 47.5 ohms, 1%, 1/4W (R114)	28480	0757-0705	1
39	1820-0954	* Integrated Circuit, CTL (MC1)	07263	SL3457	1
40	0757-0759	* Resistor, Fxd, Flm, 18.2k, 1%, 1/4W (R112)	28480	0757-0759	1
40A	0160-0153	* Capacitor, Fxd, My, 0.001 uF, 10%, 200 VDCW (C60)	56289	192P10292-PTS	1

Table 6-8. A301 Logic Supply Regulator Card (02116-6014), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-8-					
41	0757-0197	* Resistor, Fxd, Flm, 1500 ohms, 1%, 1/2W (R118)	28480	0757-0197	1
42	0150-0121	* Capacitor, Fxd, Cer, 0.1 uF, +80 -20%, 50 VDCW (C40 thru C43, C45, C47, C48, C49, C51, C59)	56289	5C50BIS-CML	10
43	0757-0808	* Resistor, Fxd, Flm, 301 ohms, 1%, 1/4W (R61)	28480	0757-0808	1
44	0757-0727	* Resistor, Fxd, Flm, 562 ohms, 1%, 1/4W (R77)	28480	0757-0727	1
45	0757-0732	* Resistor, Fxd, Flm, 909 ohms, 1%, 1/4W (R85)	28480	0757-0732	1
46	0757-0821	* Resistor, Fxd, Flm, 1.21k, 1%, 1/2W (R63,R74)	28480	0757-0821	2
47	1902-0071	* Diode, Breakdown, 9.0V, 5%, (CR50)	28480	1902-0071	1
48	1902-0556	* Diode, Breakdown, 20.0V, 5%, 1W (CR52)	28480	1902-0556	1
49	0150-0050	* Capacitor, Fxd, Cer, 1000 pF, +80 -20%, 1000 VDCW (C44, C58)	56289	C067B102E102-ZE19CDH	2
50	0757-0071	* Resistor, Fxd, Flm, 247.5 ohms, 1%, 1/4W (R65, R67)	28480	0757-0071	2



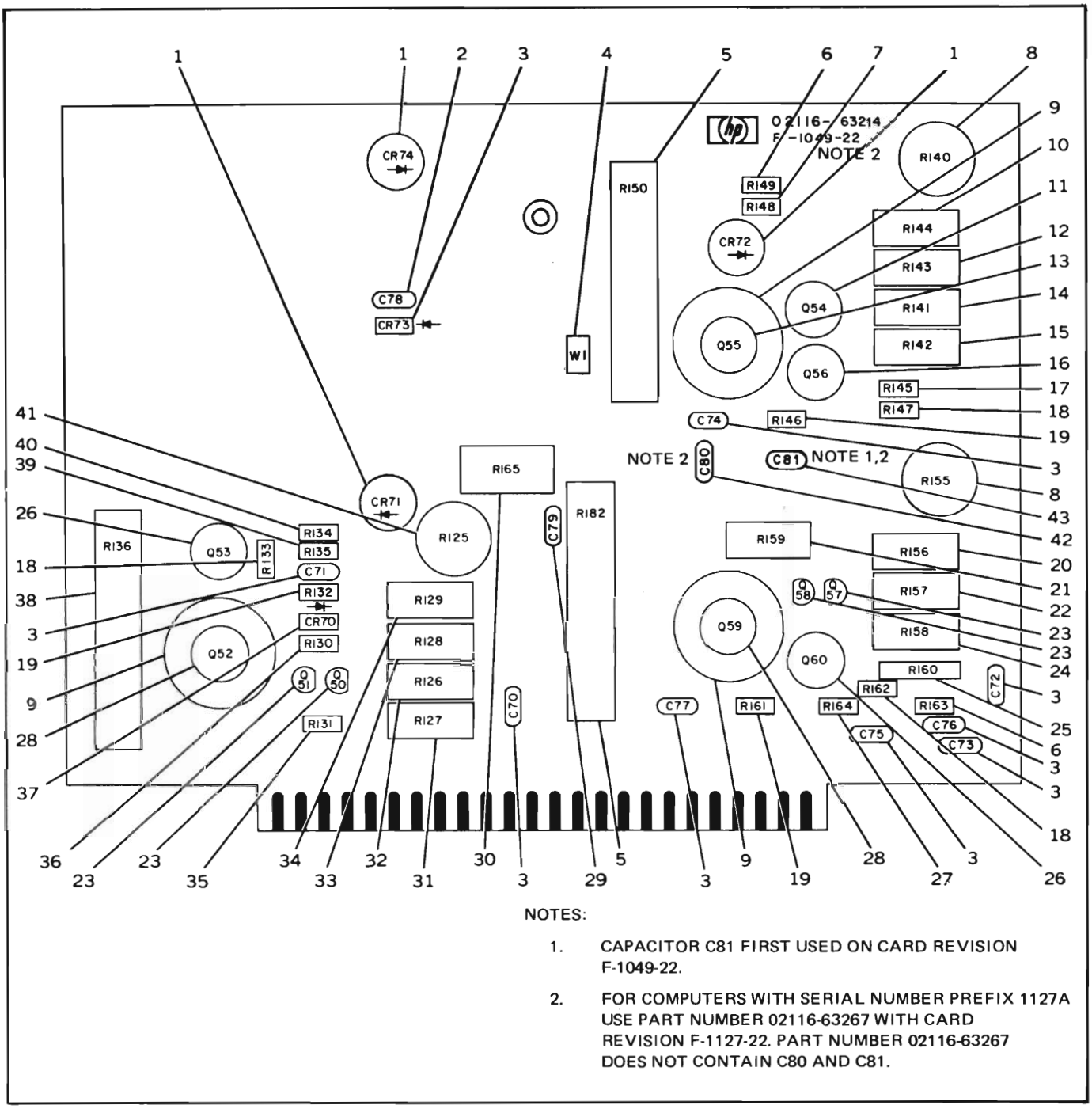
*CAPACITOR C60 FIRST USED ON CARD REVISION E-1049-22.

Figure 6-8. A301 Logic Supply Regulator Card (02116-6014), Replaceable Parts

Table 6-9. A302 Memory Supply Regulator Card (02116-63214 or 02116-63267), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-9-	02116-63214①	MEMORY SUPPLY REGULATOR CARD (A302) (24, fig. 6-7)	28480	02116-63214①	1
1	1902-0379	* Diode, Breakdown, 20V, 10%, 1.5W (CR71, CR72, CR74)	28480	1901-0379	3
2	0150-0121	* Capacitor, Fxd, Cer, 0.1 uF, +80 -20%, 50 VDCW (C70 thru C78)	56289	5C50BIS-CML	9
3	1902-3182	* Diode, Breakdown, Si, 12.1V, 5% (CR73)	28480	1902-3182	1
4	8159-0005	* Jumper Wire (W1)	28480	8159-0005	1
5	0770-0002	* Resistor, Fxd, Met Ox, 2400 ohms, 5%, 4W (R150,R182)	28480	0770-0002	2
6	0757-0442	* Resistor, Fxd, Flm, 10.0k, 1%, 1/8W (R149, R163)	28480	0757-0442	2
7	0757-0417	* Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W (R148)	28480	0757-0417	1
8	2100-1429	* Resistor, Var, ww, 2000 ohms, 5%, 1W (R140, R155)	28480	2100-1429	2
9	1205-0033	* Heat Sink	28480	1205-0033	3
10	0757-0196	* Resistor, Fxd, Flm, 6.19k, 1%, 1/2W (R144)	28480	0757-0196	1
11	1854-0221	* Transistor, Si, NPN (Q54)	28480	1854-0221	1
12	0757-0159	* Resistor, Fxd, Flm, 1000 ohms, 1%, 1/2W (R143)	28480	0757-0159	1
13	1854-0022	* Transistor, Si, NPN (Q55)	07263	S17843	1
14	0757-0839	* Resistor, Fxd, Flm, 10k, 1%, 1/2W (R142)	28480	0757-0839	1
15	0698-3411	* Resistor, Fxd, Flm, 3.48k, 1%, 1/2W (R141)	28480	0698-3411	1
16	1851-0017	* Transistor, Ge, NPN (Q56)	80131	2N1304	1
17	0757-0931	* Resistor, Fxd, Flm, 2k, 2%, 1/8W (R145)	28480	0757-0931	1
18	0757-0900	* Resistor, Fxd, Flm, 100 ohms, 2%, 1/8W (R133, R147, R162)	28480	0757-0900	3
19	0757-0924	* Resistor, Fxd, Flm, 1k, 2%, 1/8W (R132, R146, R161)	28480	0757-0924	3
20	0811-2039	* Resistor, Fxd, ww, 8000 ohms, 1%, 1/4W (R156)	28480	0811-2039	1
21	0698-3411	* Resistor, Fxd, Flm, 3.48k, 1%, 1/2W (R159)	28480	0698-3411	1
22	0811-2098	* Resistor, Fxd, ww, 2.78 ohms, 1%, 1/4W (R157)	28480	0811-2098	1
23	1853-0036	* Transistor, Si, PNP (Q50, Q51, Q57, Q58)	80131	2N3906	4
24	0811-2037	* Resistor, Fxd, ww, 2400 ohms, 1%, 1/4W (R158)	28480	0811-2037	1
25	0757-0744	* Resistor, Fxd, Flm, 3920 ohms, 1%, 1/4W (R160)	28480	0757-0744	1
26	1850-0062	* Transistor, Ge, Alloy Junction (Q53, Q60)	01295	GA287	2
27	0757-0920	* Resistor, Fxd, Flm, 680 ohms, 2%, 1/8W (R164)	28480	0757-0920	1
28	1853-0041	* Transistor, Si, PNP (Q52, Q59)	02735	38640	2
29	0160-0174	* Capacitor, Fxd, Cer, 0.47 uF, +80 -20%, 25 VDCW (C79)	56289	SC11B7S-CML	1
30	0764-0063	* Resistor, Fxd, Flm, 620 ohms, 5%, 2W (R165)	28480	0764-0063	1
31	0811-2032	* Resistor, Fxd, ww, 880 ohms, 1%, 1/4W (R127)	28480	0811-2032	1
32	0811-2033	* Resistor, Fxd, ww, 1100 ohms, 1%, 1/4W (R126)	28480	0811-2033	1
33	0811-2036	* Resistor, Fxd, ww, 1800 ohms, 1%, 1/4W (R128)	28480	0811-2036	1
34	0757-0834	* Resistor, Fxd, Flm, 5.62k, 2%, 1/2W (R129)	28480	0757-0834	1
35	0757-0914	* Resistor, Fxd, Flm, 390 ohms, 2%, 1/8W (R131)	28480	0757-0914	1
36	0757-1094	* Resistor, Fxd, Flm, 1.47k, 1%, 1/8W (R130)	28480	0757-1094	1
37	1902-0071	* Diode, Breakdown, 9.0V, 5% (CR70)	28480	1902-0003	1
38	0770-0003	* Resistor, Fxd, Flm, 3300 ohms, 5%, 4W (R136)	28480	0770-0003	1
39	0698-3154	* Resistor, Fxd, Flm, 4.22k, 1%, 1/8W (R135)	28480	0698-3154	1
40	0757-0910	* Resistor, Fxd, Flm, 270 ohms, 2%, 1/8W (R134)	28480	0757-0910	1
41	2100-0755	* Resistor, Var, ww, 1k, 5%, 1W (R125)	28480	2100-0755	1
42①	0150-0093	* Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW (C80)	28480	0150-0093	1
43①	0160-0153	* Capacitor, Fxd, My, 0.001 uF, 10%, 200 VDCW (C81)	56289	192P10292-PTS	1

① For computers with serial number prefix 1127A and above, part number 02116-63214 is replaced by part number 02116-63267 and index numbers 42 and 43 (capacitors C80 and C81) are deleted.

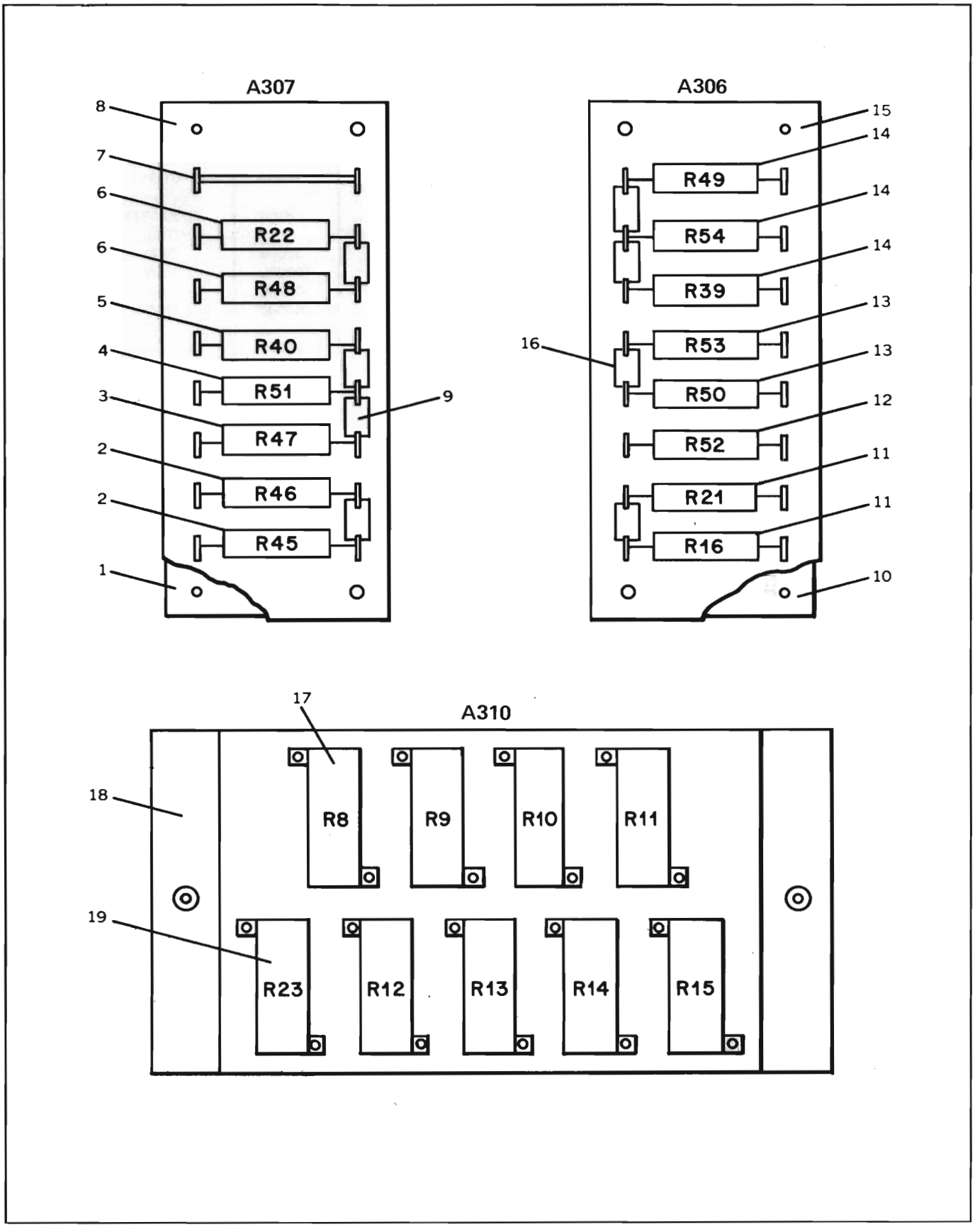


2107-59B

Figure 6-9. A302 Memory Supply Regulator Card (02116-63214 or 02116-63267), Replaceable Parts

Table 6-10. A306, A307, and A310 Component Board Assemblies, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-10-		COMPONENT BOARD ASSEMBLIES (A306, A307, A310)			3
	02116-63242	COMPONENT BOARD ASSEMBLY (A307) (1, fig. 6-7)	28480	02116-63242	1
1	5020-0244	* Bracket	28480	5020-0244	2
2	0761-0058	* Resistor, Fxd, Met Ox, 750 ohms, 5%, 1W (R45, R46)	28480	0761-0058	2
3	0811-1858	* Resistor, Fxd, ww, 500 ohms, 5%, 5W (R47)	28480	0811-1858	1
4	0767-0003	* Resistor, Fxd, Met Ox, 1.20k, 5%, 3W (R51)	28480	0767-0003	1
5	0811-1339	* Resistor, Fxd, ww, 500 ohms, 5%, 5W (R40)	28480	0811-1339	1
6	0811-2097	* Resistor, Fxd, ww, 0.25 ohm, 3%, 5W (R22, R48)	28480	0811-2097	2
7	No Number	* Bus Wire, No. 18	00000	OBD	AR
8	5080-1543	* Component Board	28480	5080-1548	1
9	5000-0207	* Shorting Bar	28480	5000-0207	4
	02116-63229	COMPONENT BOARD ASSEMBLY (A306) (2, fig. 6-7)	28480	02116-63229	1
10	5020-0244	* Bracket	28480	5020-0244	2
11	0811-2097	* Resistor, Fxd, ww, 0.25 ohm, 3%, 5W (R16,R21)	28480	0811-2097	2
12	0812-0046	* Resistor, Fxd, ww, 2.0 ohms, 5%, 5W (R52)	28480	0812-0046	1
13	0813-0038	* Resistor, Fxd, ww, 0.5 ohm, 10%, 5W (R50,R53)	28480	0813-0038	2
14	0811-2139	* Resistor, Fxd, ww, 2.2k, 5%, 3W (R39,R49,R54)	28480	0811-2139	3
15	5080-1543	* Component Board	28480	5080-1543	1
16	5000-0207	* Shorting Bar	28480	5000-0207	4
	02116-63241	COMPONENT BOARD ASSEMBLY (A310) (20, fig. 6-7)	28480	02116-63241	1
17	0811-2078	* Resistor, Fxd, ww, 0.15 ohm, 3%, 12W (R8 thru R15)	28480	0811-2078	8
18	0811-2648	* Resistor, Fxd, ww, 5 ohms, 3%, 12.5W (R23)	28480	0811-2648	1
		(Attaching Parts for items 17 and 18)			
	0520-0065	* Screw, Machine, PH, No. 2-56, 1/4 in.	00000	OBD	9
	2190-0045	* Washer, Lock, split, No. 2	00000	OBD	9
	0610-0001	* Nut, Plain, Hexagon, No. 2-56	00000	OBD	9
		— — — x — — —			
19	02116-0091	* Bracket, Resistor	28480	02116-0091	1



2107-57

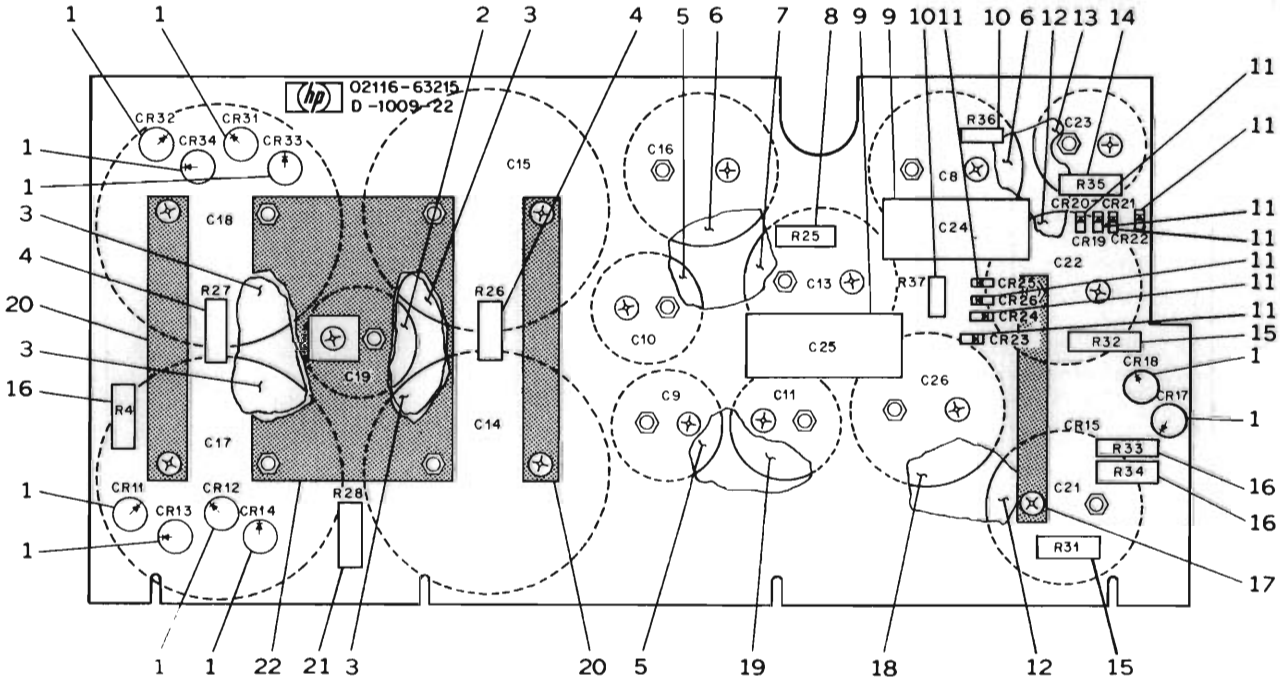
Figure 6-10. A306, A307, A310 Component Board Assemblies, Replaceable Parts

Table 6-11. A303 Capacitor Board Assembly (02116-63236), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-11-	02116-63236	CAPACITOR BOARD ASSEMBLY (A303) (28, fig. 6-7)	28480	02116-63236	1
1	1901-0416	* Diode, Si, 200 PIV, 3A (CR11 thru CR14, CR17, CR18, CR31 thru CR34)	28480	1901-0416	10
2	0180-1871	* Capacitor, Fxd, Elect, 12,000 uF, +75 -10%, 25 VDCW (C19)	28480	0180-1871	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	1
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	1
		- - - x - - -			
3	0180-1875	* Capacitor, Fxd, Elect, 100,000 uF, +75 -10% 20 VDCW (C14, C15, C17, C18)	56289	36D274G003-DF2A-DQB	4
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	4
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	8
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	4
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	4
		- - - x - - -			
4	0811-2138	* Resistor, Fxd, WW, 120 ohms, 5%, 5W (R26,R27)	28480	0811-2138	2
5	0180-1870	* Capacitor, Fxd, Elect, 10,000 uF, +75 -10%, 20 VDCW (C9, C10)	28480	0180-1870	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
6	0180-1874	* Capacitor, Fxd, Elect, 51,000 uF, +75 -10% 7.5 VDCW (C8, C16)	28480	0180-1874	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
7	0180-1869	* Capacitor, Fxd, Elect, 8700 uF, +75 -10%, 20 VDCW (C13)	28480	0180-1869	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	1
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	1
		- - - x - - -			
8	0764-0017	* Resistor, Fxd, Met Ox, 1.6k, 5%, 2W (R25)	28480	0764-0017	1
9	0180-1866	* Capacitor, Fxd, Elect, 500 uF, +75 -10%, 75 VDCW (C24, C25)	56289	39D507G75-HL4-DSB	2
10	0686-1235	* Resistor, Fxd, Comp, 12k, 5%, 1/2W (R36, R37)	01121	EB1235	2
11	1901-0191	* Diode, Si, 0.75A, 100 PIV (CR19 thru CR26)	04713	SR1358-2	8
12	0180-1873	* Capacitor, Fxd, Elect, 21,000 uF, +75 -10%, 30 VDCW (C21, C22)	28480	0180-1873	2
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	2
		- - - x - - -			

Table 6-11. A303 Capacitor Board Assembly (02116-63236), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-11-					
13	0180-1977	* Capacitor, Fxd, Elect, 5900 uF, +75 -10%, 50 VDCW (C23)	28480	0180-1977	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	2
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	2
	2680-0103	* Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	2
		- - - x - - -			
14	0812-0099	* Resistor, Fxd, WW, 1k, 5%, 5W (R35)	28480	0812-0099	1
15	0811-1857	* Resistor, Fxd, WW, 400 ohms, 5%, 5W (R31,R32)	28480	0811-1857	2
16	0813-0038	* Resistor, Fxd, WW, 0.5 ohm, 10%, 5W (R4, R33, R34)	28480	0813-0038	3
17	02116-0067	* Bus Bar	28480	02116-0067	1
18	0180-1978	* Capacitor, Fxd, Elect, 8800 uF, +50 -10%, 75 VDCW (C26)	28480	0180-1978	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	1
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2680-0103	* Screw, Machine, No. 10-32, 1/2 in.	00000	OBD	1
		- - - x - - -			
19	0180-1868	* Capacitor, Fxd, Elect, 4900 uF, +75 -10% 40 VDCW (C11)	28480	0180-1868	1
		(Attaching Parts)			
	3030-0248	* Setscrew, No. 10-32, 3/4 in.	00000	OBD	1
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	1
	2680-0103	* Screw, Machine, No. 10-32, 1/2 in.	00000	OBD	1
		- - - x - - -			
20	02116-0068	* Bus Bar	28480	02116-0068	1
21	0811-1858	* Resistor, Fxd, WW, 500 ohms, 5%, 5W (R28)	28480	0811-1858	1
22	02116-0069	* Bus Bar	28480	02116-0069	1



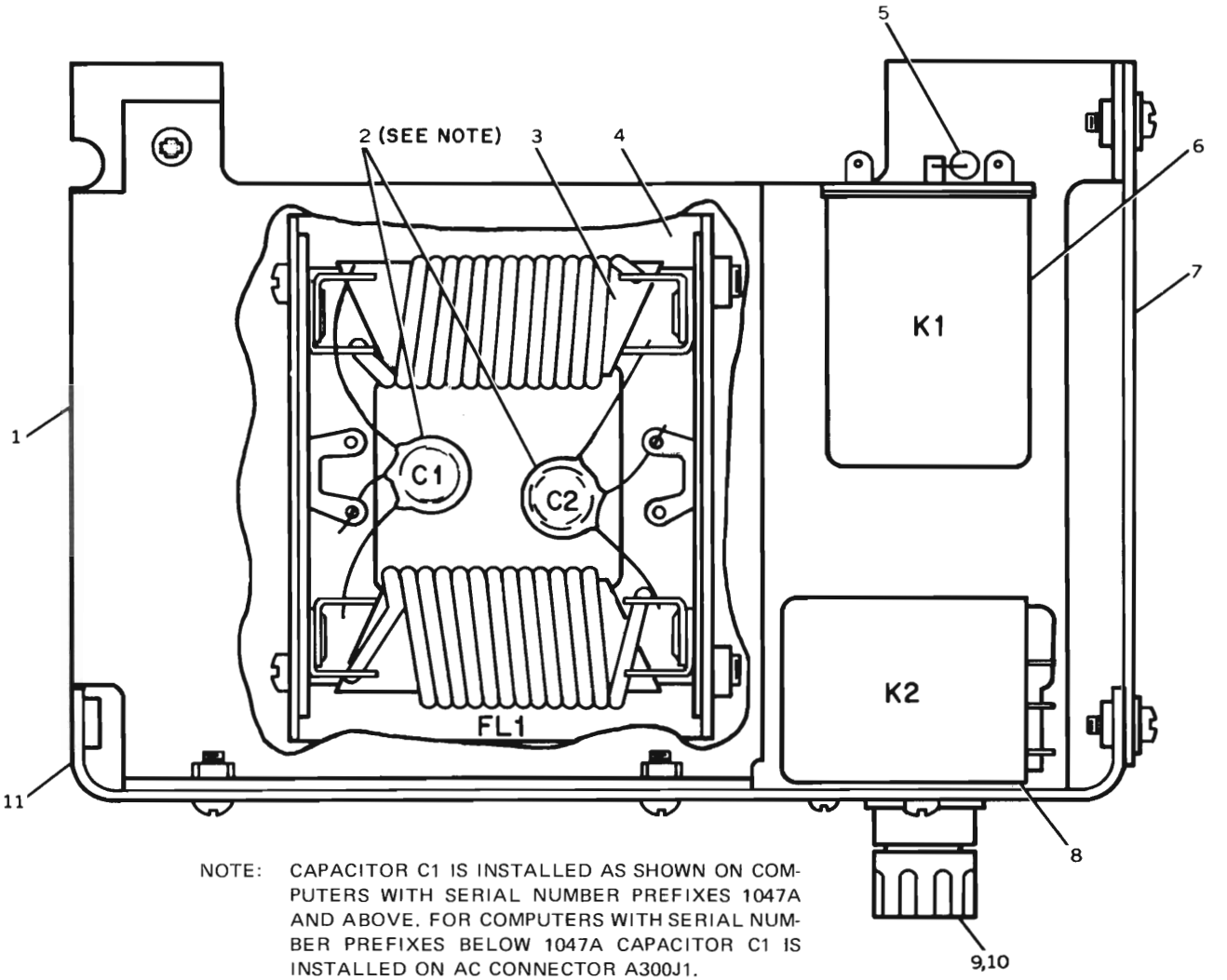
2107-60

Figure 6-11. A303 Capacitor Board Assembly (02116-63236), Replaceable Parts

Table 6-12. A312 AC Input Section (02116-63228), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-12-	02116-63228	AC INPUT SECTION (A312) (36, fig. 6-7)	28480	02116-63228	1
1	02116-0078	* Shield, Filter	28480	02116-0078	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	3
	2190-0851	* Washer, Lock, Split, No. 6	00000	OBD	1
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		– – – x – – –			
2†	0160-3043	* Capacitor, Fxd, Cer, 2x0.005 uF, 20%, 250 VACW (C1A, C1B)	56289	29C147A-CHD	1
2	0160-3043	* Capacitor, Fxd, Cer, 2x0.005 uF, 20%, 250 VACW (C2A, C2B)	56289	29C147A-CHD	1
3	9100-1834	* Line Filter, 20A, AC (FL1)	28480	9100-1834	1
4	5000-5722	* Bracket, Mounting, Filter	28480	5000-5722	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	4
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	4
		– – – x – – –			
5	1901-0045	* Diode, Si, 0.75A, 100 PIV (CR10)	04713	SR1358-7	1
6	0490-0372	* Relay, 50 ohm coil (K1)	04009	WHU012D5-503	1
		(Attaching Parts)			
	2580-0003	* Nut, Assembled Washer, No. 8-32	00000	OBD	1
		– – – x – – –			
7	02116-01117	* Cover, AC Housing	28480	02116-01117	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	3
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	3
	3050-0228	* Washer, Flat, No. 6	00000	OBD	3
		– – – x – – –			
8	0490-0892	* Relay, 250V (K2)	28480	0490-0892	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	1
	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	1
		– – – x – – –			
9	2110-0327	* Fuse, 15A, S-B (F1)	00000	OBD	1
10	1400-0084	* Fuseholder (XF1)	00000	OBD	1
11	02116-01109	* Housing, AC Input	28480	02116-01109	1

† For Computers with serial number prefixes below 1047A Capacitor C1 is installed on AC Connector A300J1 (see fig. 7-33).



NOTE: CAPACITOR C1 IS INSTALLED AS SHOWN ON COMPUTERS WITH SERIAL NUMBER PREFIXES 1047A AND ABOVE. FOR COMPUTERS WITH SERIAL NUMBER PREFIXES BELOW 1047A CAPACITOR C1 IS INSTALLED ON AC CONNECTOR A300J1.

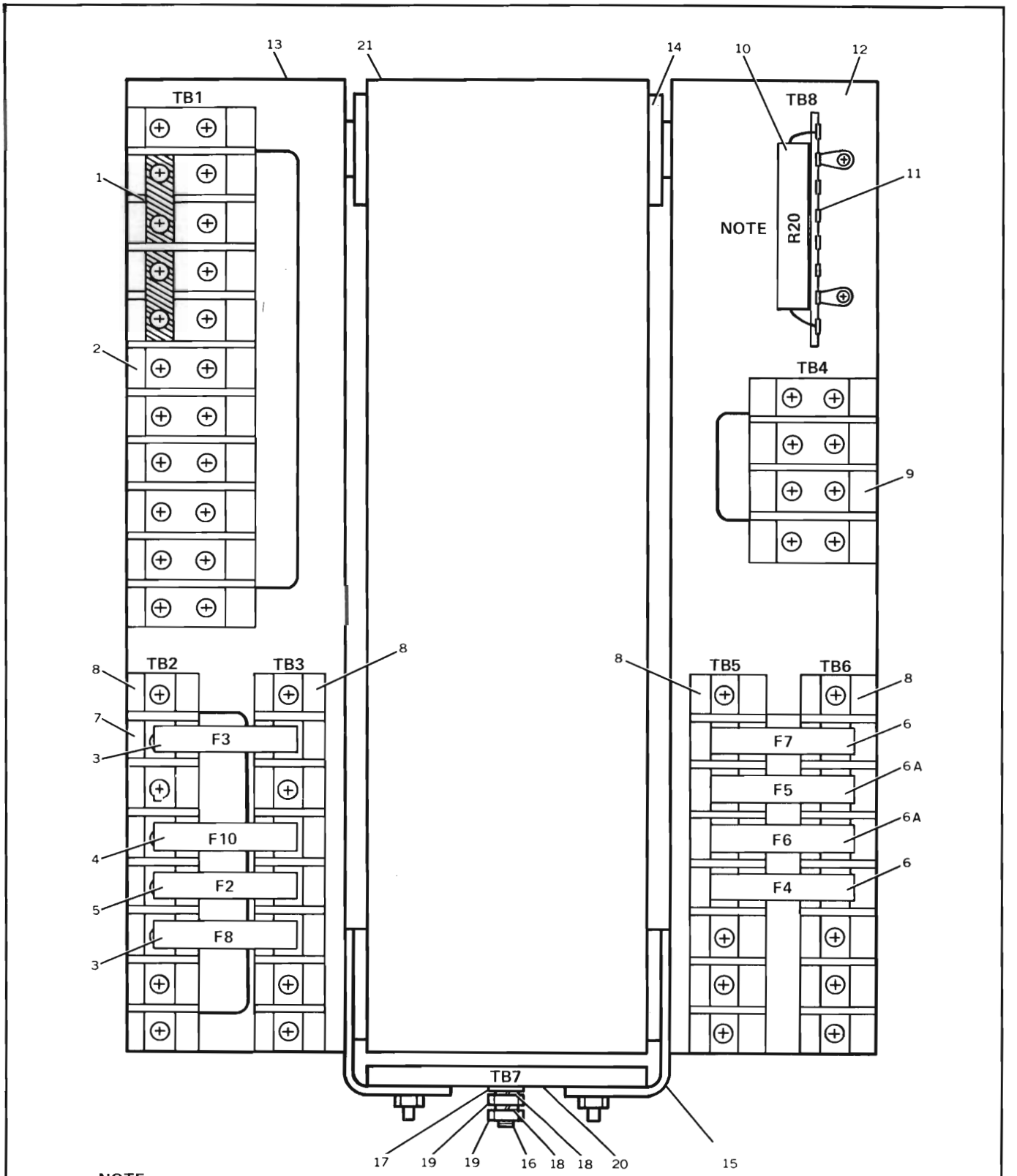
2107-61A

Figure 6-12. A312 AC Input Section (02116-63228), Replaceable Parts

Table 6-13. A311 Transformer Assembly (02116-63225), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-13-	02116-63225	TRANSFORMER ASSEMBLY (A311) (37, fig.6-7)	28480	02116-63225	1
1	0360-1279	* Shorting Strip	28480	0360-1279	2
2	0360-1256	* Terminal Board (TB1)	28480	0360-1256	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	4
		– – – x – – –			
3	2110-0044	* Fuse, 0.3A, S-B (F3, F8)	00000	OBD	2
4	2110-0014	* Fuse, 4A, S-B (F10)	00000	OBD	1
5	2110-0013	* Fuse, 3.2A, S-B (F2)	00000	OBD	1
6	2110-0035	* Fuse, 8.0A, S-B (F4, F7)	00000	OBD	2
6A	2110-0025	* Fuse, 15A, 32V, S-B (F5, F6)	00000	OBD	2
7	2110-0293	* Fuseholder Clip	00000	OBD	18
8	0360-1254	* Terminal Board (TB2, TB3, TB5, TB6)	28480	0360-1254	4
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	8
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	8
		– – – x – – –			
9	0360-1130	* Terminal Board (TB4)	28480	0360-1130	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	4
10①	0811-2735	* Resistor, Fxd, WW, 2500 ohms, 3%, 10W (R20)	28480	0811-2735	1
10②	0764-0003	* Resistor, Fxd, Met Ox, 3300 ohms, 5%, 2W, (R22,R21)	28480	0764-0003	2
11	0360-1589	* Terminal Board (TB8)	28480	0360-1589	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	3050-0228	* Washer, Flat, No. 6	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6	00000	OBD	2
		– – – x – – –			
12	02116-0060	* Bracket, Terminal Mounting, Right	28480	02116-0060	1
13	02116-0059	* Bracket, Terminal Mounting, Left	28480	02116-0059	1
		(Attaching Parts for items 12 and 13)			
	0570-0070	* Bolt, Machine, Hexagon Head, 1/4-20, 3-1/2 in.	00000	OBD	2
	3050-0234	* Washer, Flat, 1/4 in. ID	00000	OBD	6
	2190-0032	* Washer, Lock, split, 1/4 in. ID	00000	OBD	2
	2950-0004	* Nut, Plain, Hexagon, 1/4-20	00000	OBD	2
		– – – x – – –			
14	02116-0002	* Bracket, Transformer	28480	02116-0002	4
		(Attaching Parts)			
	0570-1003	* Bolt, Machine, Hexagon Head, 1/4-20, 3-1/4 in.	00000	OBD	2
	3050-0234	* Washer, Flat, 1/4 in. ID	00000	OBD	2
	2190-0032	* Washer, Lock, split, 1/4 in. ID	00000	OBD	2
	2740-0002	* Nut, Plain, Hexagon, 1/4 in. ID	00000	OBD	2
		– – – x – – –			
15	02116-0063	* Bracket, Terminal Board	28480	02116-0063	4
		(Attaching Parts)			
	2680-0104	* Screw, Machine, FH, No. 10-32, 1/2 in.	00000	OBD	4
	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	4
	2740-0002	* Nut, Plain, Hexagon, No. 10-32	00000	OBD	4
		– – – x – – –			
16	2680-0108	* Screw, Machine, FH, No. 10-32, 3/4 in.	00000	OBD	5
17	3050-0226	* Washer, Flat, No. 10	00000	OBD	5
18	2190-0034	* Washer, Lock, split, No. 10	00000	OBD	10
19	2740-0002	* Nut, Plain, Hexagon, No. 10	00000	OBD	10
20	02116-01124	* Terminal Board (TB7)	28480	02116-01124	1
21	9100-2903	* Transformer, Power	28480	9100-2903	1

① Used on Computers with serial number prefix below 1131A.
② Used on computers with serial number prefix 1131A and above.



NOTE:

FOR COMPUTERS WITH SERIAL NUMBER PREFIX 1131A AND ABOVE, RESISTOR R21 IS ADDED IN SERIES WITH RESISTOR R20.

2107-62B

Figure 6-13. A311 Transformer Assembly (02116-63225), Replaceable Parts

Table 6-14. A305 Small Heat Sink Assembly (02116-63238), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-14-	02116-63238	SMALL HEAT SINK ASSEMBLY (A305) (38, fig. 6-7)	28480	02116-63238	1
1	1251-0137	* Connector, Receptacle, 32 contacts (P1)	71785	26-4200-325	1
		(Attaching Parts)			
	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
	0590-0076	* Nut, Self-Locking, No. 4-40	00000	OBD	2
		– – – x – – –			
1A③	0160-0161	* Capacitor, Fxd, My, 0.01 uF, 10%, 20 VDCW	56289	192P10392-PTS	1
2	02116-0054	* Bracket, Connector	28480	02116-0054	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		– – – x – – –			
3	1854-0264	* Transistor, Si, NPN (Q14, Q16, Q17)	04713	2N3715	3
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	0360-0268	* Terminal Lug, int-tooth, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
4	3103-0011	* Thermal Switch, 115V, 2A (S1)	28480	3103-0011	1
5	02116-0033	* Bracket, Thermal Switch	28480	02116-0033	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	2
	2190-0006	* Washer, Lock, split, No. 6	00000	OBD	2
		– – – x – – –			
6	1854-0264	* Transistor, Si, PNP (Q16)	04713	2N3715	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		– – – x – – –			
7	1853-0063	* Transistor, Si, PNP (Q12, Q15)	04713	MJ2268	2
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	0360-0268	* Terminal Lug, int-tooth, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
8	1853-0063	* Transistor, Si, NPN (Q21)	04713	MJ2268	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		– – – x – – –			
9①	02116-0057	* Filter, Air	28480	02116-0057	1
9②	02116-01128	* Filter, Air	28480	02116-01128	1
10②	1251-0013	* Plug, Banana	28480	1251-0013	4
		(Attaching Parts)			
②	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
②	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	4
		– – – x – – –			
11②	5000-8015	* Fan Guard	28480	5000-8015	1
12①	3160-0072	* Fan Assembly, 115V, 60 Hz (B3)	28480	3160-0072	1
12②	3160-0224	* Fan Assembly, 115V, 60 Hz (B3)	28480	3160-0224	1
		(Attaching Parts)			
①	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
②	2360-0205	* Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
②	8120-1478	* Cable Assembly (Not shown in figure 6-14)	28480	8120-1478	1
		– – – x – – –			

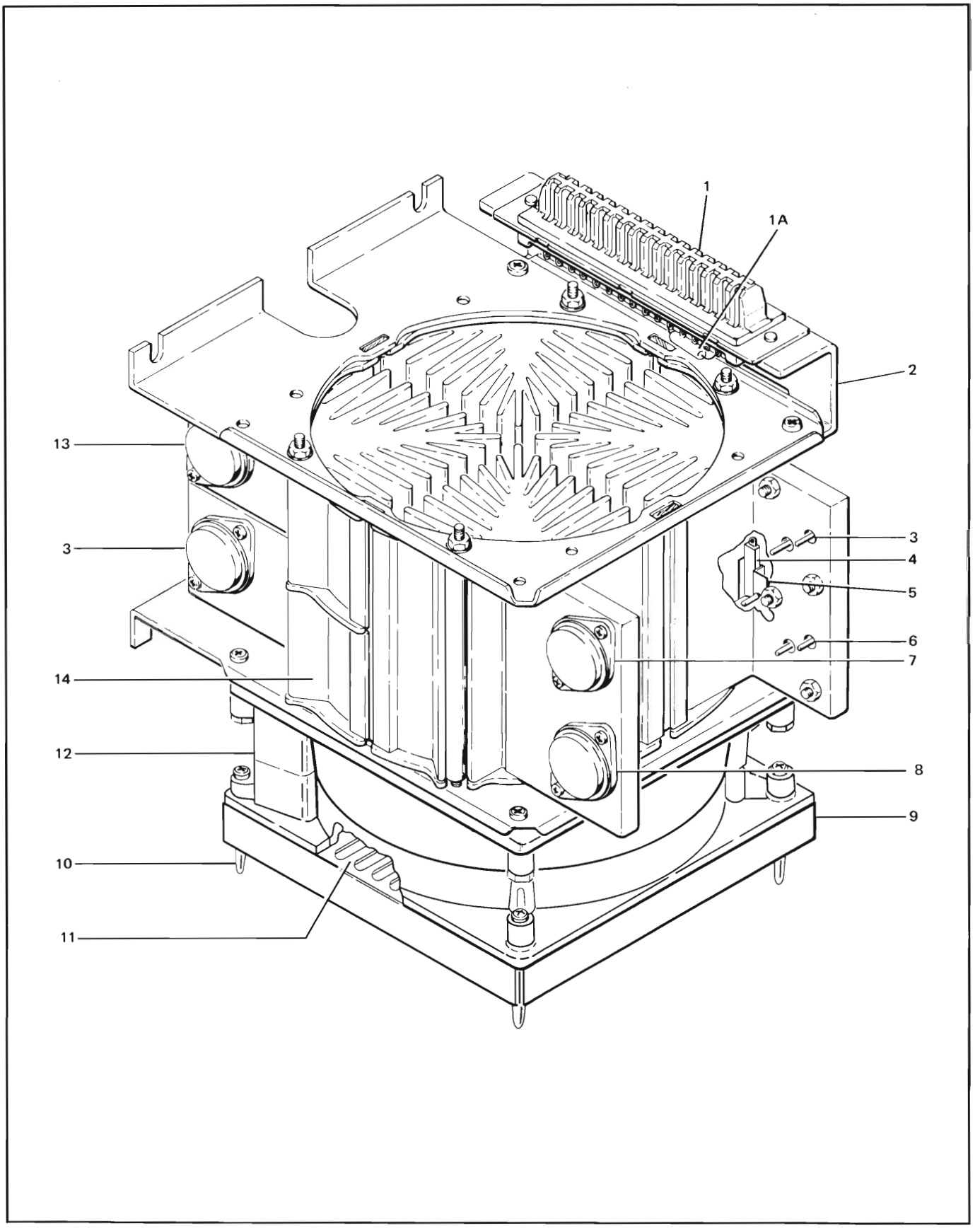
Table 6-14. A305 Small Heat Sink Assembly (02116-63238), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-14-					
13	1850-0098	* Transistor, Ge, PNP (Q13)	28480	1850-0098	1
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	2
	0360-0268	* Terminal Lug, Lock, int-tooth, No. 6	00000	OBD	1
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	2
		— — — x — — —			
14	1205-0067	* Heat Sink	28480	1205-0067	1

(1) Used on computers with serial number prefix below 1108A.

(2) First used on computers with serial number prefix 1108A.

(3) First used on computers with serial number prefix 1127A.



2107-63A

Figure 6-14. A305 Small Heat Sink Assembly (02116-63238), Replaceable Parts

Table 6-15. A308 Component Board Assembly (02116-63235), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-15-	02116-63235	COMPONENT BOARD ASSEMBLY (A308) (40, fig. 6-7)	28480	02116-63235	1
1	0815-0005	* Resistor, Fxd, WW, 62 ohms, 5%, 10W (R19)	28480	0815-0005	1
2	0811-2107	* Resistor, Fxd, WW, 75 ohms, 5%, 10W (R17, R18) (Attaching Parts for items 1 and 2)	28480	0811-2107	2
3	2510-0135	* Screw, Machine, PH, No. 8-32, 2-1/4 in.	00000	OBD	3
4	2190-0073	* Washer, Lock, split, No. 8	00000	OBD	3
5	3050-0139	* Washer, Flat, No. 8	00000	OBD	3
		– – – x – – –			
6	0811-2079	* Resistor, Fxd, WW, 0.5 ohm, 5%, 25W (R7)	28480	0811-2079	1
7	0811-2510	* Resistor, Fxd, WW, 0.1 ohm, 5%, 25W (R5, R6) (Attaching Parts for items 6 and 7)	28480	0811-2510	2
8	2510-0136	* Screw, Machine, PH, No. 8-32, 2-1/2 in.	00000	OBD	3
9	2190-0073	* Washer, Lock, split, No. 8	00000	OBD	3
10	3050-0088	* Washer, Concave, No. 8	00000	OBD	3
		– – – x – – –			
11	1902-1215	* Diode, Breakdown, 20V, 2%, 10W (CR9) (Attaching Parts)	04713	1N2984	1
12	2740-0002	* Nut, Plain, Hexagon, No. 10	00000	OBD	1
13	0360-0270	* Terminal Lug, No. 10	00000	OBD	1
		– – – x – – –			
14	1901-0496	* Diode, Si, 100 PIV, 12A (CR5 thru CR8, CR15, CR16) (Attaching Parts)	04713	MR1121	6
15	No Number	* Washer, Mica (furnished with diode)			12
16	No Number	* Insulator, Teflon (furnished with diode)			6
17	0360-0270	* Terminal Lug, No. 10	00000	OBD	6
18	3050-0019	* Washer, Flat, No. 10	00000	OBD	6
19	2740-0002	* Nut, Plain, Hexagon, No. 10	00000	OBD	6
		– – – x – – –			
20	0757-0159	* Resistor, Fxd, Flm, 1k, 1%, 1/2W (R2, R3)	28480	0757-0156	2
21	0360-0279	* Standoff, No. 4-40, internal threaded base (Attaching Parts)	28480	0360-0279	2
	2200-0139	* Screw, Machine, PH, No. 4-40, 1/4 in.	00000	OBD	2
	2190-0108	* Washer, Lock, split, No. 4	00000	OBD	2
		– – – x – – –			
22	02116-01107	* Bracket	28480	02116-01107	1

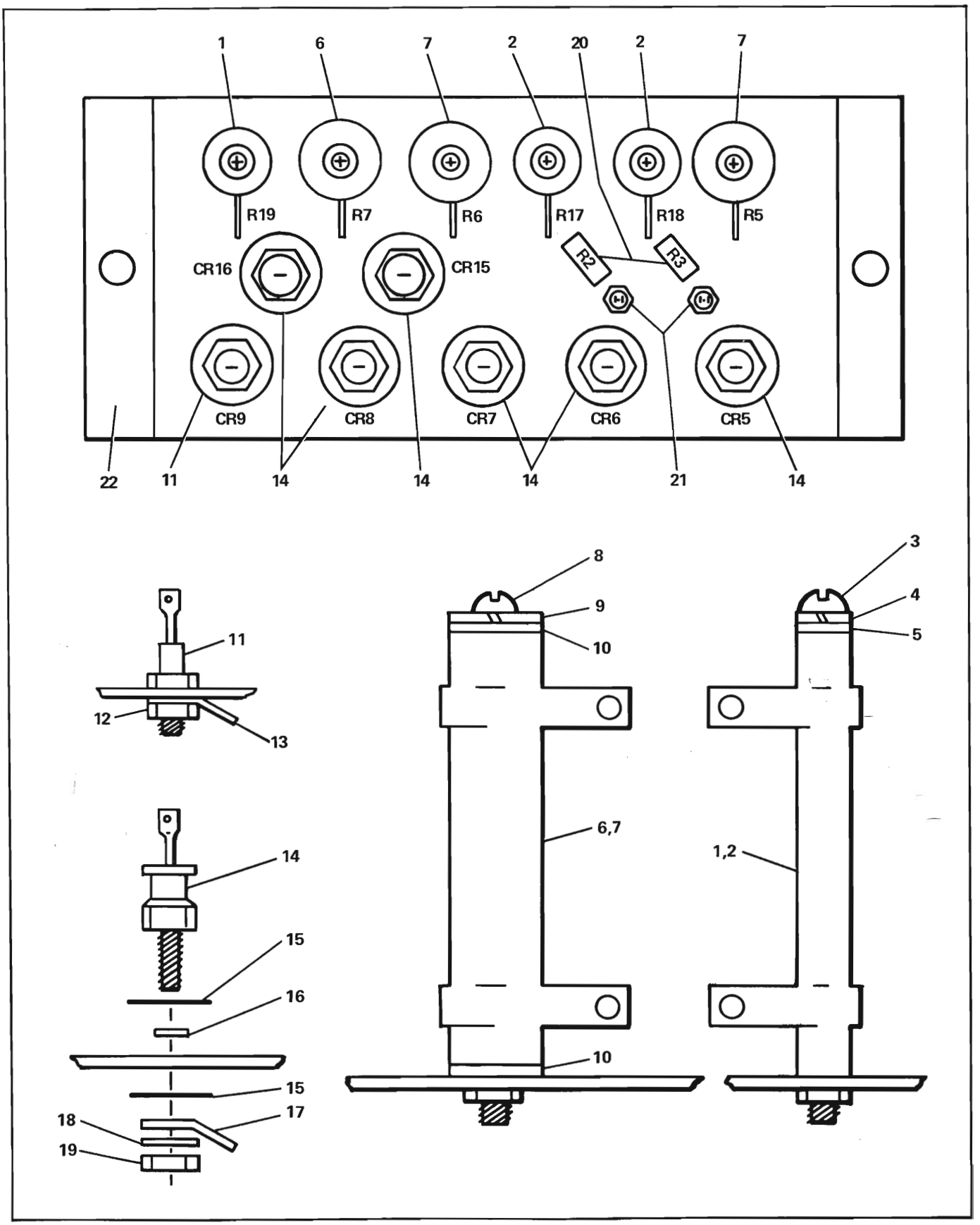


Figure 6-15. A308 Component Board Assembly (02116-63235), Replaceable Parts

Table 6-16. A304 Large Heat Sink Assembly (02116-63237), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-16-	02116-63237	LARGE HEAT SINK ASSEMBLY (A304) (39, fig. 6-7)	28480	02116-63237	1
1	1251-0137	* Connector, Receptacle, 32 contacts (P1)	71785	26-4200-32S	1
		(Attaching Parts)			
	2200-0143	* Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	2
	0590-0076	* Nut, Self-Locking, Hexagon, No. 4-40 in.	00000	OBD	2
		– – – x – – –			
2	02116-0054	* Bracket, Connector	28480	02116-0054	1
		(Attaching Parts)			
	2360-0197	* Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		– – – x – – –			
3	1854-0264	* Transistor, Si, NPN (Q9, Q20)	04713	2N3715	2
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	0360-0268	* Terminal Lug, int-tooth, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
4	1850-0098	* Transistor, Ge, PNP (Q10, Q11)	28480	1850-0098	2
		(Attaching Parts)			
	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
	0360-0268	* Terminal Lug, int-tooth, No. 6	00000	OBD	2
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
5	1850-0198	* Transistor, Ge, PNP (Q1, Q3, Q6, Q7)	04713	2N2156	4
		(Attaching Parts)			
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	0360-0268	* Terminal Lug, int-tooth, No. 6	00000	OBD	4
		– – – x – – –			
6	1850-0198	* Transistor, Ge, PNP (Q2, Q4, Q5, Q8)	04713	2N2156	4
		(Attaching Parts)			
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
7	3103-0004	* Thermal Switch, 115V, 2A (S1)	28480	3103-0004	1
8	02116-0033	* Bracket, Thermal Switch	28480	02116-0033	1
		(Attaching Parts)			
	2360-0193	* Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	2
	2190-0006	* Washer, Lock, split, No. 6	00000	OBD	2
		– – – x – – –			
9①	02116-0057	* Filter, Air	28480	02116-0057	1
9②	02116-01128	* Filter, Air	28480	02116-01128	1
10②		* Plug, Banana	28480	1251-0013	4
		(Attaching Parts)			
②	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
②	2190-0851	* Washer, Lock, split, No. 6	00000	OBD	4
		– – – x – – –			
11②	5000-8015	* Fan Guard	28480	5000-8015	1
12①	3160-0072	* Fan Assembly, 115V, 60 Hz (B2)	28480	3160-0072	1

Table 6-16. A304 Large Heat Sink Assembly (02116-63237), Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-16-					
12②	3160-0224	* Fan Assembly, 115V, 60 Hz (B2)	28480	3160-0224	1
		(Attaching Parts)			
①	2360-0203	* Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	4
②	2360-0205	* Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	4
	2420-0002	* Nut, Plain, Hexagon, No. 6-32	00000	OBD	4
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	4
		– – – x – – –			
②	8120-1478	* Cable Assembly (Not shown in figure 6-16)	28480	8120-1478	1
		– – – x – – –			
13	1205-0006	* Heat Sink	28480	1205-0006	1

① Used on computers with serial number prefix below 1108A.
② First used on computers with serial number prefix 1108A.

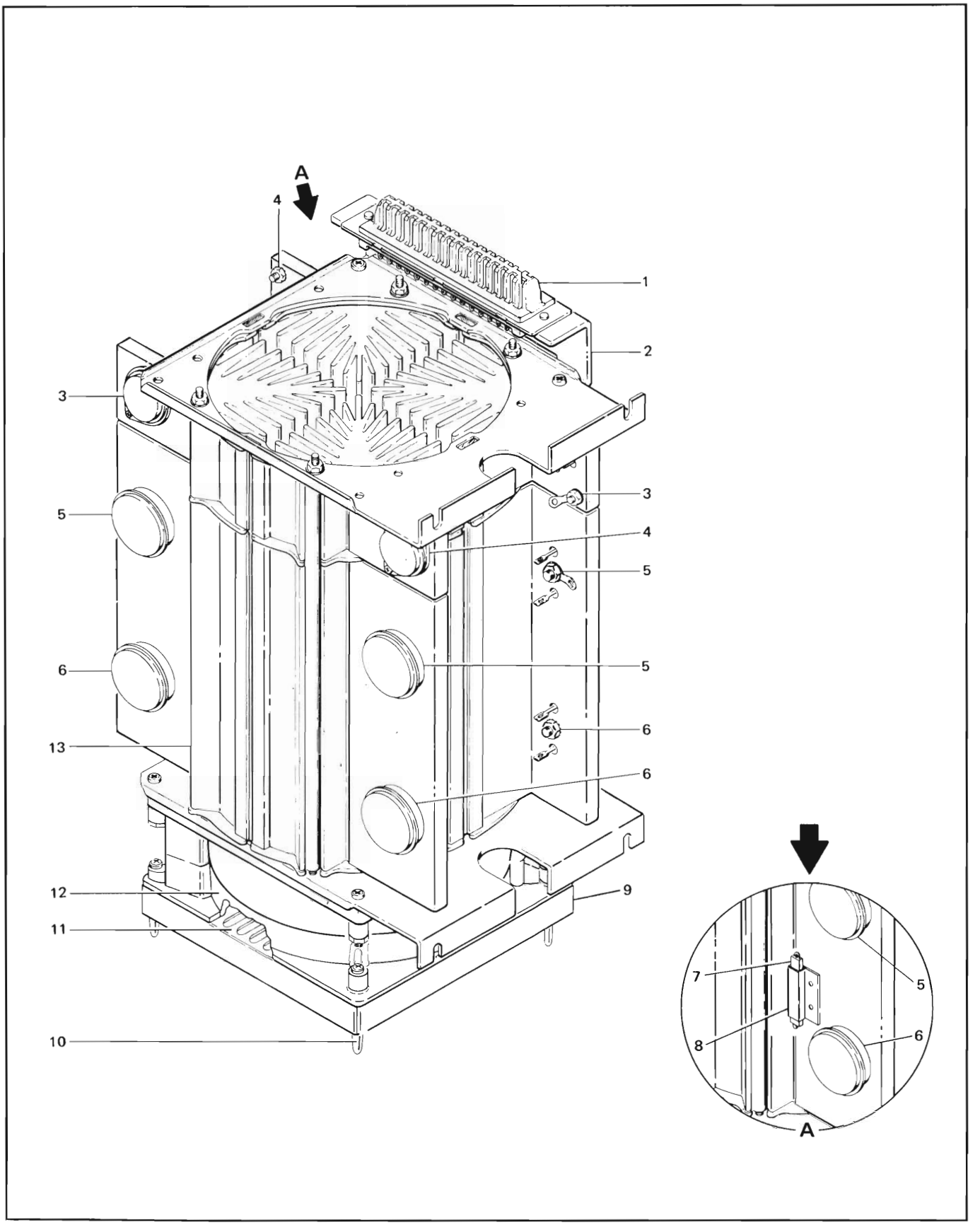


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Figure 6-16. A304 Large Heat Sink Assembly (02116-63237), Replaceable Parts

Table 6-17. A309 Component Board Assembly (02116-63240), Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-17-	02116-63240	COMPONENT BOARD ASSEMBLY (A309) (46, fig. 6-7)	28480	02116-63240	1
1	0150-0093	* Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW (C4 thru C7)	28480	0150-0093	4
2	02116-0066	* Shorting Bar	28480	02116-0066	2
		(Attaching Parts)			
	2480-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	4
	3050-0239	* Washer, Nonmetallic, No. 8	00000	OBD	4
	3050-0139	* Washer, Flat, No. 8	00000	OBD	4
	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	4
		- - - x - - -			
3	1901-0344	* Diode, Si, (CR1 thru CR4)	28480	1901-0344	4
		(Attaching Parts)			
	2480-0004	* Nut, Plain, Hexagon, No. 8-32	00000	OBD	4
	0360-0269	* Terminal Lug, No. 8	00000	OBD	4
	3050-0239	* Washer, Nonmetallic, No. 8	00000	OBD	4
	3050-0139	* Washer, Flat, No. 8	00000	OBD	4
	2510-0109	* Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	4
		- - - x - - -			
4	02116-0056	* Diode Mounting Bracket	28480	02116-0056	1
		(Attaching Parts)			
	2510-0103	* Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	2
	2190-0076	* Washer, Lock, split, No. 8	00000	OBD	2
	3050-0139	* Washer, Flat, No. 8	00000	OBD	2
		- - - x - - -			
5	2110-0256	* Fuse, 30A, 32V, S-B (F11, F12, F13, F14)	00000	OBD	4
6	2110-0293	* Fuseholder Clip	00000	OBD	8
7	2110-0255	* Fuse Mounting Bracket	28480	2110-0255	1
		(Attaching Parts)			
	2360-0201	* Screw, Machine, FH, No. 6-32, 1/2 in.	00000	OBD	2
	2420-0001	* Nut, Assembled Washer, No. 6-32	00000	OBD	2
		- - - x - - -			
8	02116-0021	* Right Brace	28480	02116-0021	1

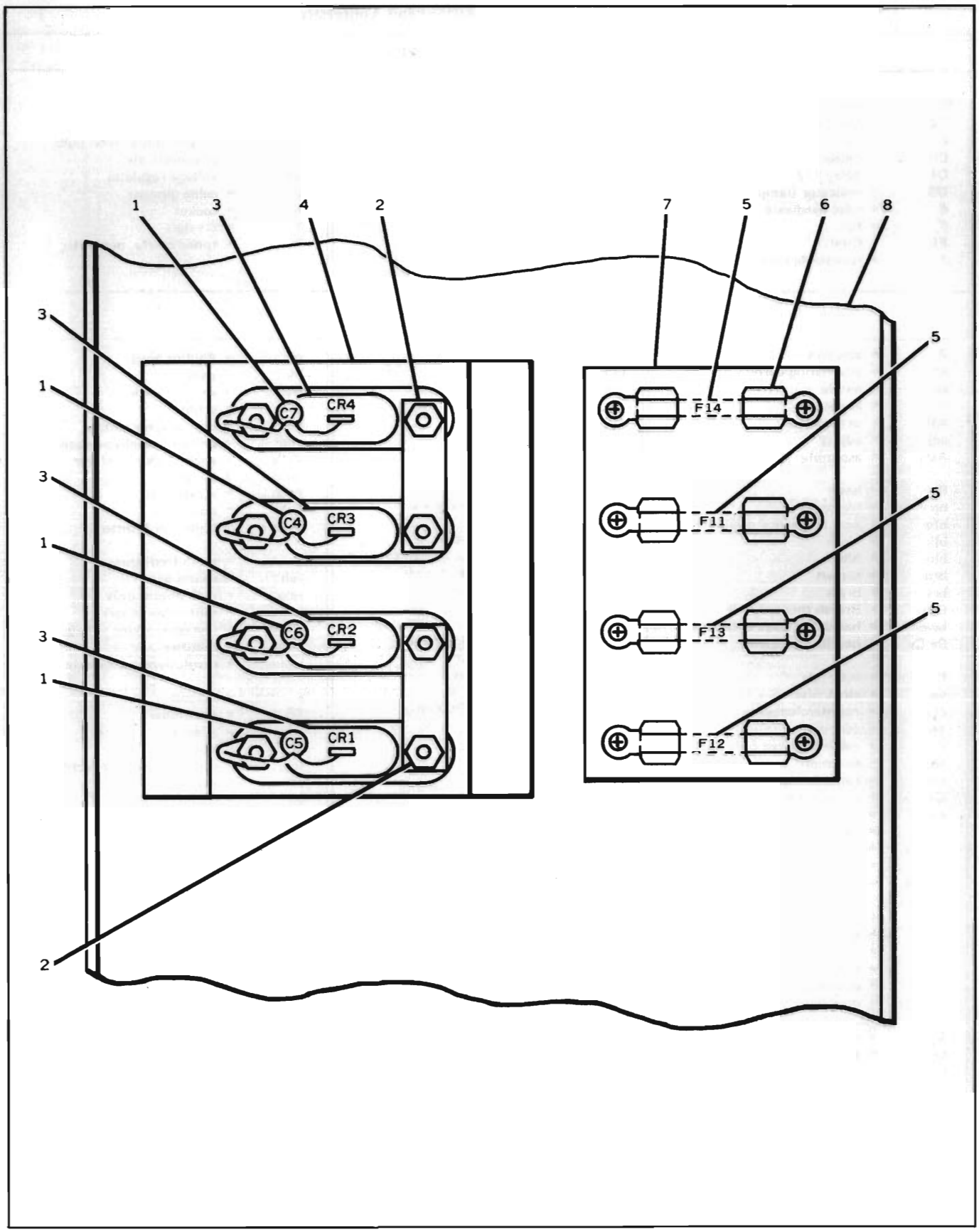

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Figure 6-17. A309 Component Board Assembly (02116-63240), Replaceable Parts

Table 6-18. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit
C	= capacitor	MC	= microcircuit	V	= vacuum tube, neon bulb, photocell, etc.
CR	= diode	P	= plug connector		
DL	= delay line	Q	= transistor	VR	= voltage regulator
DS	= indicator (lamp)	R	= resistor	W	= cable, jumper
E	= misc hardware	RT	= thermistor	X	= socket
F	= fuse	S	= switch	Y	= crystal
FL	= filter	T	= transformer	Z	= tuned cavity, network
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gnd	= ground(ed)	ph	= Phillips head
ac	= alternating current	gra	= gray	pk	= peak
ad	= anode	grn	= green	p-p	= peak-to-peak
Al	= aluminum			pt	= point
AR	= as required	H	= henries	PIV	= peak inverse voltage
adj	= adjust	Hg	= mercury	PNP	= positive-negative-positive
Assy	= assembly	hr	= hour(s)	PWV	= peak working voltage
		Hz	= hertz	porc	= porcelain
B	= base	hdw	= hardware	posn	= position(s)
bp	= bandpass	hex	= hexagon, hexagonal	pozi	= pozidrive
bfo	= beat frequency oscillator			ph brz	= phosphor bronze
blk	= black	ID	= inside diameter		
blu	= blue	IF	= intermediate frequency	rf	= radio frequency
brn	= brown	in.	= inch, inches	rdh	= round head
brs	= brass	I/O	= input/output	rmo	= rack mount only
Btu	= British thermal unit	int	= internal	rms	= root-mean-square
bwc	= backward wave oscillator	incl	= include(s)	RWV	= reverse working voltage
Be Cu	= beryllium copper	insul	= insulation, insulated	rect	= rectifier
		impgrg	= impregnated	r/min	= revolutions per minute
C	= collector	incand	= incandescent		
cw	= clockwise			s	= second
ccw	= counterclockwise	k	= kilo (10^3), kilohm	SB	= slow-blow
cer	= ceramic			Se	= selenium
cmo	= cabinet mount only	lp	= low pass	Si	= silicon
com	= common			scr	= silicon-controlled rectifier
crt	= cathode-ray tube	m	= milli (10^{-3})	sil	= silver
CTL	= capacitor-transistor logic	M	= mega (10^6), megohm	sst	= stainless steel
cath	= cathode	My	= Mylar	stl	= steel
cd pl	= cadmium plate	mfr	= manufacturer	spcl	= special
Comp	= composition	mom	= momentary	spdt	= single-pole, double-throw
conn	= connector	mtg	= mounting	spst	= single-pole, single-throw
compl	= complete	misc	= miscellaneous	semicond	= semiconductor
		met ox	= metal oxide		
dc	= direct current	mintr	= miniature	Ta	= tantalum
dr	= drive			td	= time delay
DTL	= diode-transistor logic	n	= nano (10^{-9})	Ti	= titanium
depc	= deposited carbon	nc	= normally closed or no connection	tgl	= toggle
dpdt	= double-pole, double-throw			thd	= thread
dpst	= double-pole, single-throw	Ne	= neon	tol	= tolerance
		no.	= number or normally open	TTL	= transistor-transistor logic
E	= emitter	np	= nickel plated	term	= terminal
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative positive zero (zero temperature coefficient)	U (μ)	= micro (10^{-6})
elctlt	= electrolytic				
		NSR	= not separately replaceable	V	= volt(s)
F	= farads	NRFR	= not recommended for field replacement	var	= variable
FF	= flip-flop			vio	= violet
flh	= flat head	OD	= outside diameter	VDCW	= direct current working volts
flm	= film	OBD	= order by description		
fxd	= fixed	orn	= orange	W	= watts
filh	= fillister head	ovh	= oval head	ww	= wirewound
		oxd	= oxide	wht	= white
G	= giga (10^9)			WIV	= working inverse voltage
Ge	= germanium	p	= pico (10^{-12})		
gl	= glass	PC	= printed circuit	yel	= yellow

Table 6-19. Total Quantity of Electrical Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192	2
0140-0197	Capacitor, Fxd, Mica, 180 pF, 5%, 300 VDCW	04062	RDM15F181J3C	1
0140-0225	Capacitor, Fxd, Mica, 300 pF, 1%	28480	0140-0225	2
0150-0050	Capacitor, Fxd, Cer, 1000 pF, 600 VDCW	28480	0150-0050	2
0150-0093 ①	Capacitor, Fxd, Cer, 0.001 uF, +80 -20%, 100 VDCW	28480	0150-0093	4
0150-0121	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 50 VDCW	56289	5C50B1S-CML	19
0160-0127	Capacitor, Fxd, Cer, 1.0 uF, 20%, 25 VDCW	56289	5C13CS-CML	41
0160-0154	Capacitor, Fxd, Mica, 0.0022 uF, 10%, 200 VDCW	56289	192P22292-PTS	1
0160-0153 ①	Capacitor, Fxd, My, 0.001 uF, 10%, 200 VDCW	56289	192P10292-PTS	1
0160-0161 ②	Capacitor, Fxd, My, 0.01 uF, 10%, 200 VDCW	56289	192P10392-PTS	1
0160-0163	Capacitor, Fxd, My, 0.033 uF, 10%, 200 VDCW	56289	192P33392-PTS	3
0160-0174	Capacitor, Fxd, Cer, 0.47 uF, +80 -20%, 25 VDCW	56289	SC11B7S-CML	1
0160-0363	Capacitor, Fxd, Mica, 620 pF, 5%	28480	0160-0363	1
0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW	28480	0160-2055	11
0160-2223 ③	Capacitor, Fxd, Mica, 1600 pF, 5%	28480	0160-2223	17
0160-2588	Capacitor, Fxd, Cer, 1000 pF, 5%, 50 VDCW	28480	0160-2588	1
0160-2940	Capacitor, Fxd, Mica, 470 pF, 5%, 300 VDCW	72136	RDM15F471J3C	4
0160-3043	Capacitor, Fxd, Cer, 2x0.005 uF, 20%, 250 VAC	56289	29C147A-CDH	2
0180-0064	Capacitor, Fxd, Elect, 35 uF, +100 -10%, 6 VDCW	56289	30D156G006BB4	3
0180-0094	Capacitor, Fxd, Elect, 100 uF, +75 -10%, 25 VDCW	56289	30D107G 015DD2-DSM	2
0160-3710 ③	Capacitor, Fxd, Mica, 1600 pF, 5%	72136	DM15F16250	17
0180-0097	Capacitor, Fxd, Elect, 47 uF, 10%, 35 VDCW	28480	0180-0097	2
0180-0116	Capacitor, Fxd, Elect, 2.7 uF, 10%, 35 VDCW	28480	0180-0116	2
0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	28480	0180-0155	34
0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X 9020A2	14
0180-1714	Capacitor, Fxd, Elect, 330 uF, 10%, 6 VDCW	28480	0180-1714	1
0180-1866	Capacitor, Fxd, Elect, 500 uF, +75 -10%, 75 VDCW	56289	39D507G 075HL4	2
0180-1867	Capacitor, Fxd, Elect, 1600 uF, +75 -10%, 10 VDCW	28480	0180-1867	1
0180-1868	Capacitor, Fxd, Elect, 4900 uF, +75 -10%, 40 VDCW	28480	0180-1868	1
0180-1869	Capacitor, Fxd, Elect, 8700 uF, +75 -10%, 50 VDCW	28480	0180-1869	1
0180-1870	Capacitor, Fxd, Elect, 10,000 uF, +75 -10%, 20 VDCW	28480	0180-1870	2
0180-1871	Capacitor, Fxd, Elect, 12,000 uF, +75 -10%, 25 VDCW	28480	0180-1871	1
0180-1873	Capacitor, Fxd, Elect, 21,000 uF, +75 -10%, 30 VDCW	28480	0180-1873	2
0180-1874	Capacitor, Fxd, Elect, 15,000 uF, +75 -10%, 7.5 VDCW	28480	0180-1874	2
0180-1875	Capacitor, Fxd, Elect, 100,000 uF, +75 -10%, 20 VDCW	28480	0180-1875	4
0180-1977	Capacitor, Fxd, Elect, 5900 uF, +50 -10%, 50 VDCW	28480	0180-1977	1
0180-1978	Capacitor, Fxd, Elect, 8800 uF, +50 -10%, 75 VDCW	28480	0180-1978	1
0410-0035	Crystal, Quartz, 10 mc/s, 0.005%	28480	0410-0035	1
0490-0372	Relay, 12 VDC, 50-ohm, Coil	04009	WHU012D5-503	1
0490-0892	Relay, 250V	28480	0490-0892	1
0683-1005	Resistor, Fxd, Comp, 10 ohms, 5%, 1/4W	01121	CB1005	1
0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4W	01121	CB1015	5
0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025	51
0683-1215	Resistor, Fxd, Comp, 120 ohms, 5%, 1/4W	01121	CB1215	1
0683-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/4W	01121	CB1515	2
0683-2015	Resistor, Fxd, Comp, 200 ohms, 5%, 1/4W	01121	CB2015	6
0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4W	01121	CB2215	5
0683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4W	01121	CB3305	9
0683-3315	Resistor, Fxd, Comp, 330 ohms, 5%, 1/4W	01121	CB3315	1
0683-3935	Resistor, Fxd, Comp, 39k, 5%, 1/4W	01121	CB3935	1
0683-4705	Resistor, Fxd, Comp, 47 ohms, 5%, 1/4W	01121	CB4705	1

Table 6-19. Total Quantity of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715	38
0683-4725	Resistor, Fxd, Comp, 4700 ohms, 5%, 1/4W	01121	CB4725	1
0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4W	01121	CB5115	4
0683-6805	Resistor, Fxd, Comp, 68 ohms, 5%, 1/4W	01121	CB6805	20
0683-8215	Resistor, Fxd, Comp, 820 ohms, 5%, 1/4W	01121	CB8215	1
0686-1235	Resistor, Fxd, Comp, 12k, 5%, 1/2W	01121	EB1235	2
0686-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/2W	01121	EB1515	1
0686-2205	Resistor, Fxd, Comp, 22 ohms, 5%, 1/2W	01121	EB2205	4
0686-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/2W	01121	EB2215	1
0686-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/2W	01121	EB4715	4
0689-1505	Resistor, Fxd, Comp, 15 ohms, 5%, 1W	01121	GB1505	2
0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082	19
0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8W	28480	0698-3132	2
0698-3134	Resistor. Fxd. Flm. 1.33k, 1%, 1/4W	28480	0698-3134	1
0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154	1
0698-3315	Resistor, Fxd, Flm, 100 ohms, 5%, 1/8W	28480	0698-3315	2
0698-3399	Resistor, Fxd, Flm, 133 ohms, 1%, 1/2W	28480	0698-3399	18
0698-3400	Resistor, Fxd, Flm, 147 ohms, 1%, 1/2W	28480	0698-3400	16
0698-3408	Resistor, Fxd, Flm, 2.15 ohms, 1%, 1/2W	28480	0698-3408	1
0698-3411	Resistor, Fxd, Flm, 3.48k, 1%, 1/2W	28480	0698-3411	2
0698-3430	Resistor, Fxd, Flm, 21.5 ohms, 1%, 1/8W	28480	0698-3430	2
0698-3437	Resistor, Fxd, Flm, 133 ohms, 1%, 1/8W	28480	0698-3437	4
0698-3442	Resistor, Fxd, Flm, 237 ohms, 1%, 1/8W	28480	0698-3442	15
0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	28480	0698-3444	16
0698-3488	Resistor, Fxd, Flm, 442 ohms, 1%, 1/8W	28480	0698-3488	17
0698-4037	Resistor, Fxd, Flm, 46.4 ohms, 1%, 1/8W	28480	0698-4037	34
0698-7310	Resistor, Fxd, Flm, 1650 ohms, 25%, 1/8W	28480	0698-7310	34
0757-0068	Resistor, Fxd, Flm, 74.9 ohms, 1%, 1/4W	28480	0757-0068	1
0757-0071	Resistor, Fxd, Flm, 247.5 ohms, 1%, 1/4W	28480	0757-0071	2
0757-0156	Resistor, Fxd, Flm, 1.5 megohms, 1%, 1/2W	28480	0757-0156	2
0757-0158	Resistor, Fxd, Flm, 619 ohms, 1%, 1/2W	28480	0757-0158	1
0757-0159	Resistor, Fxd, Flm, 1000 ohms, 1%, 1/2W	28480	0757-0159	2
0757-0180	Resistor, Fxd, Flm, 31.6 ohms, 1%, 1/8W	28480	0757-0180	68
0757-0196	Resistor, Fxd, Flm, 6.19k, 1%, 1/2W	28480	0757-0196	1
0757-0197	Resistor, Fxd, Flm, 1500 ohms, 1%, 1/2W	28480	0757-0197	1
0757-0198	Resistor, Fxd, Flm, 100 ohms, 1%, 1/2W	28480	0757-0198	1
0757-0244	Resistor, Fxd, Flm, 499 ohms, 1.0%, 1/4W	28480	0757-0244	3
0757-0274	Resistor, Fxd, Flm, 1.21k, 1%, 1/8W	28480	0757-0274	4
0757-0276	Resistor, Fxd, Flm, 61.9 ohms, 1%, 1/8W	28480	0757-0276	2
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280	76
0757-0284	Resistor, Fxd, Flm, 150 ohms, 1%, 1/8W	28480	0757-0284	2
0757-0338	Resistor, Fxd, Flm, 1.00k, 1%, 1/4W	28480	0757-0338	2
0757-0340	Resistor, Fxd, Flm, 10.0k, 1%, 1/4W	28480	0757-0340	1
0757-0399	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/8W	28480	0757-0399	34
0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401	4
0757-0403	Resistor, Fxd, Flm, 121 ohms, 1%, 1/8W	28480	0757-0403	64
0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W	28480	0757-0417	1
0757-0421	Resistor, Fxd, Flm, 825 ohms, 1%, 1/8W	28480	0757-0421	4
0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442	19
0757-0705	Resistor, Fxd, Flm, 47.5 ohms, 1%, 1/4W	28480	0757-0705	1

Table 6-19. Total Quantity of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0757-0711	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/4W	28480	0757-0711	2
0757-0715	Resistor, Fxd, Flm, 150 ohms, 1%, 1/4W	28480	0757-0715	2
0757-0727	Resistor, Fxd, Flm, 562 ohms, 1%, 1/4W	28480	0757-0727	1
0757-0728	Resistor, Fxd, Flm, 619 ohms, 1%, 1/4W	28480	0757-0728	1
0757-0730	Resistor, Fxd, Flm, 750 ohms, 1%, 1/4W	28480	0757-0730	3
0757-0732	Resistor, Fxd, Flm, 909 ohms, 1%, 1/4W	28480	0757-0732	1
0757-0739	Resistor, Fxd, Flm, 2.00k, 1%, 1/4W	28480	0757-0739	1
0757-0743	Resistor, Fxd, Flm, 3.32k, 1%, 1/4W	28480	0757-0743	3
0757-0744	Resistor, Fxd, Flm, 3920 ohms, 1%, 1/4W	28480	0757-0744	1
0757-0759	Resistor, Fxd, Flm, 18.2k, 1%, 1/4W	28480	0757-0759	1
0757-0805	Resistor, Fxd, Flm, 221 ohms, 1%, 1/2W	28480	0757-0805	1
0757-0808	Resistor, Fxd, Flm, 301 ohms, 1%, 1/4W	28480	0757-0808	2
0757-0814	Resistor, Fxd, Flm, 511 ohms, 1%, 1/2W	28480	0757-0814	1
0757-0821	Resistor, Fxd, Flm, 1.21k, 1%, 1/2W	28480	0757-0821	2
0757-0834	Resistor, Fxd, Flm, 5.62k, 2%, 1/2W	28480	0757-0834	1
0757-0839	Resistor, Fxd, Flm, 10k, 1%, 1/2W	28480	0757-0839	2
0757-0900	Resistor, Fxd, Flm, 100 ohms, 2%, 1/8W	28480	0757-0900	3
0757-0910	Resistor, Fxd, Flm, 270 ohms, 2%, 1/8W	28480	0757-0910	1
0757-0912	Resistor, Fxd, Flm, 330 ohms, 2%, 1/8W	28480	0757-0912	1
0757-0914	Resistor, Fxd, Flm, 390 ohms, 2%, 1/8W	28480	0757-0914	1
0757-0915	Resistor, Fxd, Flm, 430 ohms, 2%, 1/8W	28480	0757-0915	1
0757-0920	Resistor, Fxd, Flm, 680 ohms, 2%, 1/8W	28480	0757-0920	1
0757-0924	Resistor, Fxd, Flm, 1k, 2%, 1/8W	28480	0757-0924	6
0757-0931	Resistor, Fxd, Flm, 2k, 2%, 1/8W	28480	0757-0931	1
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094	1
0761-0011	Resistor, Fxd, Met Ox, 3300 ohms, 5%, 1W	28480	0761-0011	1
0761-0026	Resistor, Fxd, Met Ox, 220 ohms, 5%, 1W	28480	0761-0026	1
0761-0058	Resistor, Fxd, Met Ox, 750 ohms, 5%, 1W	28480	0761-0058	2
0764-0003 (18)	Resistor, Fxd, Met Ox, 3.3k, 5%, 2W	28480	0764-0003	2
0764-0017	Resistor, Fxd, Met Ox, 1.6k, 5%, 2W	28480	0764-0017	1
0764-0063	Resistor, Fxd, Flm, 620 ohms, 5%, 2W	28480	0764-0063	1
0767-0003	Resistor, Fxd, Met Ox, 1.20k, 5%, 3W	28480	0767-0003	1
0770-0002	Resistor, Fxd, Met Ox, 2400 ohms, 5%, 4W	28480	0770-0002	2
0770-0003	Resistor, Fxd, Flm, 3300 ohms, 5%, 4W	28480	0770-0003	1
0811-0003	Resistor, Fxd, Flm, 390 ohms, 1%, 1/4W	28480	0811-0003	1
0811-1339	Resistor, Fxd, WW, 500 ohms, 5%, 5W	28480	0811-1339	1
0811-1857	Resistor, Fxd, WW, 400 ohms, 5%, 5W	28480	0811-1857	4
0811-1858	Resistor, Fxd, WW, 500 ohms, 5%, 5W	28480	0811-1858	2
0811-2031	Resistor, Fxd, WW, 815 ohms, 3%, 1/4W	28480	0811-2031	1
0811-2032	Resistor, Fxd, WW, 880 ohms, 1%, 1/4W	28480	0811-2032	1
0811-2033	Resistor, Fxd, WW, 1100 ohms, 1%, 1/4W	28480	0811-2033	1
0811-2036	Resistor, Fxd, WW, 1800 ohms, 1%, 1/4W	28480	0811-2036	1
0811-2037	Resistor, Fxd, WW, 2400 ohms, 1%, 1/4W	28480	0811-2037	1
0811-2039	Resistor, Fxd, WW, 8000 ohms, 1%, 1/4W	28480	0811-2039	1
0811-2078	Resistor, Fxd, WW, 0.15 ohms, 3%, 12W	28480	0811-2078	8
0811-2079	Resistor, Fxd, WW, 0.25 ohms, 10%, 25W	28480	0811-2079	1
0811-2084	Resistor, Fxd, WW, 43 ohms, 1%, 5W	28480	0811-2084	1
0811-2097	Resistor, Fxd, WW, 0.25 ohms, 3%, 5W	28480	0811-2097	4

Table 6-19. Total Quantity of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0811-2098	Resistor, Fxd, WW, 2.75 ohms, 1%, 1/4W	28480	0811-2098	1
0811-2107	Resistor, Fxd, WW, 75 ohms, 5%, 10W	28480	0811-2107	2
0811-2138	Resistor, Fxd, WW, 120 ohms, 5%, 5W	28480	0811-2138	2
0811-2139	Resistor, Fxd, WW, 2.2k, 5%, 3W	28480	0811-2139	3
0811-2140	Resistor, Fxd, WW, 2 ohms, 5%, 5W	28480	0811-2140	1
0811-2510	Resistor, Fxd, WW, 0.1 ohm, 5%, 25W	28480	0811-2510	2
0811-2614	Resistor, Fxd, WW, 37 ohms, 1%, 5W	28480	0811-2614	4
0811-2648	Resistor, Fxd, WW, 5 ohms, 3%, 12.5W	28480	0811-2648	1
0811-2735 (19)	Resistor, Fxd, WW, 2500 ohms, 3%, 10W	28480	0811-2735	1
0811-2918	Resistor, Fxd, WW, 391 ohms, 1.0%, 5W	28480	0811-2918	17
0812-0046	Resistor, Fxd, WW, 2.0 ohms, 5%, 5W	28480	0812-0046	1
0812-0099	Resistor, Fxd, WW, 1k, 5%, 5W	28480	0812-0099	1
0813-0038	Resistor, Fxd, WW, 0.5 ohm, 10%, 5W	28480	0813-0038	13
0815-0005	Resistor, Fxd, WW, 62 ohms, 5%, 10W	28480	0815-0005	1
1200-0199	Socket, Crystal	91506	8000-AG9	1
1250-0315 ④	Connector, Receptacle	28480	1250-0315	1
1250-0367	Jack, Tip	28480	1251-0367	8
1251-0013 ⑤	Plug, Banana	28480	1251-0013	4
1251-0136	Connector, 32 pin male	02660	26-4100-32P	2
1251-0137	Connector, Receptacle, 32 contacts	02660	26-4200-32S	1
1251-0143	Connector, 32 contacts	28480	1251-0143	1
1251-0233	Connector, PC, 44 contacts	28480	1251-0233	1
1251-0335	Connector, 48 pin	71785	251-24-30-261	1
1251-2660 ⑥	Connector, Receptacle	28480	1251-2660	1
1400-0084	Fuseholder	79515	342014	1
1820-0140	Integrated Circuit	28480	1820-0140	1
1820-0141	Integrated Circuit	28480	1820-0141	9
1820-0186	Integrated Circuit	28480	1820-0186	17
1820-0187	Integrated Circuit	28480	1820-0187	7
1820-0482	Integrated Circuit	28480	1820-0482	9
1820-0952	Integrated Circuit, CTL	07263	SL3455	67
1820-0953	Integrated Circuit, CTL	07263	SL3456	73
1820-0954	Integrated Circuit, CTL	07263	SL3457	34
1820-0955	Integrated Circuit, CTL	07263	SL3458	1
1820-0956	Integrated Circuit, CTL	07263	SL3459	92
1820-0957	Integrated Circuit, CTL	07263	SL3460	2
1820-0965	Integrated Circuit, CTL	07263	SL3462	15
1820-0966	Integrated Circuit, CTL	07263	SL3463	5
1820-0967	Integrated Circuit, CTL	07263	SL3464	40
1820-0968	Integrated Circuit, CTL	07263	SL3466	8
1820-0971	Integrated Circuit, CTL	07263	SL3467	19
1821-0006	Integrated Circuit	28480	1821-0006	25
1850-0062	Transistor, Ge, Alloy Junction	01295	GA287	6
1850-0098	Transistor, Ge, PNP	28480	1850-0098	3
1850-0198	Transistor, Ge, PNP	04713	2N2156	8
1851-0017	Transistor, Ge, NPN	01295	2N130A	3
1853-0001	Transistor, Si, PNP	28480	1853-0001	6
1853-0015	Transistor, Si, PNP	04713	MPS-3640-5	5
1853-0036	Transistor, Si, PNP	04713	SPS-3612	46
1853-0041	Transistor, Si, PNP	02735	38640	2
1853-0063	Transistor, Si, PNP	04713	MJ2268	3
1854-0003	Transistor, Si, NPN	28480	1854-0003	2

Table 6-19. Total Quantity of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
1854-0005	Transistor, Si, NPN	04713	2N708	3
1854-0019	Transistor, Si, NPN	28480	1854-0019	39
1854-0022	Transistor, Si, NPN	07263	S17843	1
1854-0047	Transistor, Si, NPN	28480	1854-0047	1
1854-0094	Transistor, Si, NPN	07263	2N3646	17
1854-0215	Transistor, Si, NPN	04713	SP53611	1
1854-0221	Transistor, Si, NPN	28480	1854-0221	1
1854-0246	Transistor, Si, NPN	07263	2N3643	29
1854-0264	Transistor, Si, NPN	04713	2N3715	5
1854-0265	Transistor, Si, NPN	28480	1854-0265	1
1880-0047	Thyristor, SCR, 25V, 55A	28480	1884-0047	1
1884-0046	Thyristor, SCR, 50V, 25A	28480	1884-0046	4
1901-0025	Diode, Si, 100 mA, 1V	07263	FD2387	13
1901-0040	Diode, Si, 30 mA 30 WV	07263	FDG1088	142
1901-0045	Diode, Si, 0.75A, 100 PIV	04713	SR1358-7	1
1901-0191	Diode, Si, 0.75A, 100 PIV	04713	SR1358-2	13
1901-0343	Diode, Si, 50 PIV, 18A	04713	1N3491R	3
1901-0344	Diode, Si	28480	1901-0344	4
1901-0379	Diode, Breakdown, 20V, 10%, 1.5W	28480	1901-0379	1
1901-0406	Diode, Si, 50 PIV, 18A	04713	1N3491/MR-322	3
1901-0416	Diode, Si, 200 PIV, 3A	28480	1901-0416	10
1901-0476	Diode, Si	28480	1901-0476	4
1902-0017	Diode, Breakdown, 6.81V, 10%, 400 MW	28480	1902-0017	1
1902-0071	Diode, Breakdown, 9.0V, 5%	28480	1902-0071	3
1902-0184	Diode, Breakdown, Si, 16.2V, 5%	28480	1902-0184	1
1902-0379	Diode, Breakdown, 20V, 10%, 1.5W	28480	1902-0379	3
1902-0551	Diode, Breakdown, 6.19V, 5%	28480	1902-0551	1
1902-0556	Diode, Breakdown, 20.0V, 5%, 1W	28480	1902-0556	1
1902-1205	Diode, Breakdown, 15V, +2%	04713	1N2979RB	2
1902-1215	Diode, Breakdown, 20.0V, 2%, 10W	04713	1N2984B	1
1902-1217	Diode, Breakdown, 6.20V, 5%, 405 mA	04713	SZ11746	1
1902-1228	Diode, Breakdown, 27V, 10%, 10W	28480	1902-1228	2
1902-3079	Diode, Breakdown, Si, 4.53V	28480	1902-3079	8
1902-3182	Diode, Breakdown, Si, 12.1V, 5%	28480	1902-3182	1
1902-3224	Diode, Breakdown, 17.8V, 5%, 400 MW	28480	1902-3224	1
1910-0016	Diode, Ge, 100 mA, 0.85V, 60 PIV	93332	D2361	2
1910-0022	Diode, Ge, 5 WIV	28480	1910-0022	8
2100-0755	Resistor, Var, WW, 1k, 5%	28480	2100-0755	1
2100-1429	Resistor, Var, WW, 2000 ohms, 5%, 1W	28480	2100-1429	2
2100-1770	Resistor, Var, WW, 100 ohms, 5%, 1W	28480	2100-1770	3
2100-1772	Resistor, Var, WW, 500 ohms, 5%, 1W	28480	2100-1772	2
2100-1776	Resistor, Var, WW, 10k, 5%, 1W	28480	2100-1776	1
2110-0013	Fuse, 3.2A, 125V, S-B	00000	OBD	1
2110-0014	Fuse, 4A, 125V, S-B	00000	OBD	1
2110-0023	Fuse, 6.25A, 250V, S-B	00000	OBD	2
2110-0025	Fuse, 15A, 32V, S-B	00000	OBD	2
2110-0035	Fuse, 8.0A, 250V, S-B	00000	OBD	2
2110-0044	Fuse, 0.30A, 250V, S-B	00000	OBD	2
2110-0256	Fuse, 32V, 30A, S-B	00000	OBD	4
2140-0035	Lamp, Incandescent, 6V, 0.04A	71744	345	92
3100-2687	Switch	28480	3100-2687	1

Table 6-19. Total Quantity of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
3101-0004	Switch, Pushbutton, spdt	28480	3101-0004	2
3101-0005	Switch, Toggle, dpdt, 125V, 6A	28480	3101-0005	1
3101-0714	Switch, Lighted Pushbutton, dpdt	28480	3101-0714	1
3101-0715	Switch, Pushbutton, spdt	28480	3101-0715	9
3101-0973	Switch, slide, dpdt, 0.5A, 125V, ac/dc	79727	G126-0018	3
3101-1051	Switch, Toggle, spst, 125V, 3A	88140	8908K507	17
3103-0004	Thermal Switch	28480	3103-0004	1
3103-0011	Thermal Switch	28480	3103-0011	2
3160-0072 (16)	Fan, Tubeaxial, 115V, 60 Hz	28480	3160-0072	6
3160-0224 (5)	Fan, Assembly, 115V, 60 Hz	28480	3160-0224	6
5060-8320 (7)	Sense Amplifier Card	28480	5060-8320	2
8120-1214	Cable	28480	8120-1214	1
8120-1478 (5)	Cable Assembly	28480	8120-1478	6
8159-0005	Jumper Wire	28480	8159-0005	5
9100-1834	Line Filter, 20A, ac	28480	9100-1834	1
9100-2903	Transformer, Power	28480	9100-2903	1
9100-3130	Transformer	28480	9100-3130	25
9140-0107	Coil, Fxd, RF, 27 MHz, 10%	99800	1840-38	1
02116-6014	Logic Supply Regulator Card	28480	02116-6014	1
02116-6026	Arithmetic Logic Card	28480	02116-6026	5
02116-6027	Instruction Decoder Card	28480	02116-6027	2
02116-6029	Shift Logic Card	28480	02116-6029	2
02116-6041	I/O Control Card	28480	02116-6041	2
02116-6043	Display Board	28480	02116-6043	1
02116-6175	Power Fail Interrupt Card	28480	02116-6175	2
02116-6194	I/O Address Card	28480	02116-6194	2
02116-6208	Front Panel Coupler Card	28480	02116-6208	2
02116-6290	Cable Assembly	28480	02116-6290	1
02116-6291	Cable Assembly	28480	02116-6291	1
02116-6292	Cable Assembly	28480	02116-6292	1
02116-6293	Cable Assembly	28480	02116-6293	1
02116-6294	Cable Assembly	28480	02116-6294	1
02116-63207 (7)	Sense Amplifier Card	28480	02116-63207	2
02116-63210	Inhibit Driver Card	28480	02116-63210	2
02116-63211	X-Y Driver/Switch Card	28480	02116-63211	2
02116-63212	Memory Address Decoder Card	28480	02116-63212	2
02116-63213	Overvoltage, Component Board Assembly	28480	02116-63213	1
02116-63214 (1)	Memory Regulator Supply Card	28480	02116-63214	1
02116-63217	Power Supply Assembly	28480	02116-63217	1
02116-63219	Door Assembly	28480	02116-63219	1
02116-63220	Timing Generator Card	28480	02116-63220	2
02116-63225	Transformer Assembly	28480	02116-63225	1
02116-63228	AC Input Assembly	28480	02116-63228	1
02116-63229	Component Board Assembly	28480	02116-63229	1
02116-63235	Component Board Assembly	28480	02116-63235	1
02116-63236	Capacitor Board Assembly	28480	02116-63236	1
02116-63237	Heat Sink Assembly, Large	28480	02116-63237	1
02116-63238	Heat Sink Assembly, Small	28480	02116-63238	1
02116-63240	Component Board Assembly	28480	02116-63240	1

Table 6-19. Total Quantity of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
02116-63241	Component Board Assembly	28480	02116-63241	1
02116-63242	Component Board Assembly	28480	02116-63242	1
02116-63244	Connector Assembly, Small	28480	02116-63244	1
02116-63248	Memory Data Buffer Card	28480	02116-63248	2
02116-63267 ②	Memory Supply Regulator Card	28480	02116-63267	1

NOTES:

(1) On computers with serial number prefix 1127A and above, decrease the total quantity by 1.
(2) First used on computers with serial number prefix 1127A.
(3) Part no. 0160-3710 replaces part no. 0160-2223 on Inhibit Driver Cards (02116-63210) with card revision B-1042-22.
(4) Used on computers with serial prefix numbers below 1047A.
(5) First used on computers with serial number prefix 1108A.
(6) First used on computers with serial number prefix 1047A.
(7) Sense Amplifier Cards with part no. 02116-63207 and 5060-8320 are interchangeable.
(16) Used on computers with serial number prefix below 1108A.
(18) First used on computers with serial number prefix 1131A.
(19) On computers with serial number prefix 1131A and above, decrease the total quantity by 1.

Table 6-20. Total Quantity of Mechanical Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0360-0268	Terminal Lug, No. 6	00000	OBD	16
0360-0269	Terminal Lug, No. 8	00000	OBD	4
0360-0270	Terminal Lug, No. 10	00000	OBD	5
0360-0271	Terminal Lug, 1/4 ID	00000	OBD	2
0360-0279	Standoff, No. 4-40, internal threaded base	28480	0360-0279	3
0360-1089	Terminal Lug, 1/2 ID	00000	OBD	2
0360-1130	Terminal Board	28480	0360-1130	1
0360-1254	Terminal Board	28480	0360-1254	1
0360-1255	Terminal Board	00000	OBD	4
0360-1256	Terminal Board	28480	0360-1256	2
0360-1260	Terminal Lug	28480	0360-1260	2
0360-1264	Terminal Lug	28480	0360-1264	7
0360-1279	Shorting Strip	28480	0360-1279	2
0360-1589	Terminal Board	28480	0360-1589	2
0362-0128	Crimp Lug, Termination	00000	OBD	1
0362-0188	Cover, Power Switch	28480	0362-0188	2
0380-0002	Spacer, 1/4 in.	00000	OBD	1
0400-0082	Grommet, Nylon	28480	0400-0082	2
0403-0091	Insert, Foot	28480	0403-0091	4
0404-0247	Trim Strip	28480	0404-0247	2
0404-0248	Trim Strip, Left	28480	0404-0248	1
0404-0371	Trim, Strip, Right	28480	0404-0371	1
0460-0020	Adhesive Cork	28480	0460-0020	1
0510-0735	Latch, Female	28480	0510-0735	6
0510-0736	Latch, Male	28480	0510-0736	6
0520-0065	Screw, Machine, PH, No. 2-56, 1/4 in.	00000	OBD	9
0520-0103	Screw, Machine, PH, No. 2-56, 3/8 in.	00000	OBD	2
0570-0070	Belt, Machine, Hexagon Head, 1/4-20, 3-1/2 in.	00000	OBD	2
0570-1003	Belt, Machine, Hexagon Head, 1/4-20, 3-1/4 in.	00000	OBD	2
0570-1049	Spring Plunger	01226	M-54N	2
0590-0010	Cap Nut, No. 8	00000	OBD	4
0590-0076	Nut, Self-Locking, Hexagon, No. 4	00000	OBD	12
0590-0077	Nut, Self-Locking, Hexagon, No. 6-32	00000	OBD	1
0590-0843	Nut, Self-Locking, Hexagon, No. 8-32	00000	OBD	8
0610-0001	Nut, Plain, Hexagon, No. 2-56	00000	OBD	11
0624-0284 ⑤	Screw, Tapping, Thread Cutting, No. 6	00000	OBD	2
1200-0080	Washer, Flat, Anodized, No. 10	28480	1200-0080	6
1200-0088	Washer, Flat, Anodized	28480	1200-0088	4
1200-0089	Washer, Flat, Anodized	28480	1200-0089	2
1205-0006	Heat Sink	28480	1205-0006	1
1205-0033	Heat Sink	28480	1205-0033	5
1205-0067	Heat Sink	28480	1205-0067	1
1360-0107	Button Latch	13061	B10-B1	1
1390-0179	Lock and Key	74842	DS416J	1
1400-0124	Cable Clamp	00000	OBD	5
1400-0126	Cable Clamp	00000	OBD	1
1400-0127	Cable Clamp	00000	OBD	1
1400-0716	Tag, Identification	28480	1400-0716	1
1400-0741	Cable Clamp, Base	28480	1400-0741	1
1410-0009	Bearing, Ball, Annular	21335	SIKFS58115	10
1460-0742	Spring, Compression, 5/8 in. long, 3/16 in. ID	00000	OBD	1

Table 6-20. Total Quantity of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
1480-0116	Extractor Pin, PC Card	28480	1480-0116	32
2110-0255	Fuse Mounting Bracket	28480	2110-0255	2
2110-0293	Fuseholder Clip	00000	OBD	26
2190-0003	Washer, Lock, split, No. 4	00000	OBD	1
2190-0006	Washer, Lock, split, No. 6	00000	OBD	7
2190-0007	Washer, Lock, int-tooth, No. 6	00000	OBD	4
2190-0010	Washer, Lock, ext-tooth, No. 8	00000	OBD	4
2190-0017	Washer, Lock, split, No. 8	00000	OBD	57
2190-0032	Washer, Lock, split, 1/4 in. ID	00000	OBD	14
2190-0034	Washer, Lock, split, No. 10	00000	OBD	41
2190-0043	Washer, Lock, split, 1/2 in. ID	00000	OBD	19
2190-0045	Connector, Receptacle, Power	74868	32-2907-3	11
2190-0047 (8)	Washer, Recessed, No. 6	00000	OBD	8
2190-0048	Washer, Recessed, No. 8	00000	OBD	18
2190-0070	Washer, Lock, ext-tooth, 1/4 in. ID			2
2190-0076	Washer, Lock, split, No. 8	00000	OBD	31
2190-0108	Washer, Lock, split, No. 4	00000	OBD	20
2190-0851 (9)	Washer, Lock, split, No. 6	00000	OBD	56
2200-0139	Screw, Machine, PH, No. 4-40, 1/4 in.	00000	OBD	2
2200-0141	Screw, Machine, PH, No. 4-40, 5/16 in.	00000	OBD	1
2200-0143	Screw, Machine, PH, No. 4-40, 3/8 in.	00000	OBD	22
2200-0144	Screw, Machine, FH, No. 4-40, 3/8 in.	00000	OBD	3
2200-0147 (6)	Screw, Machine, PH, No. 4-40, 1/2 in.	00000	OBD	4
2200-0149	Screw, Machine, PH, No. 4-40, 5/8 in.	00000	OBD	8
2200-0709	Screw, Machine, Nylon, FH, No. 4-40, 3/8 in.	00000	OBD	4
2260-0009 (6)	Nut, Assembled Washer, No. 4-40	00000	OBD	4
2360-0109	Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	4
2360-0192	Screw, Machine, FH, No. 6-32, 1/4 in.	00000	OBD	13
2360-0193	Screw, Machine, PH, No. 6-32, 1/4 in.	00000	OBD	41
2360-0196	Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	12
2360-0197 (10)	Screw, Machine, PH, No. 6-32, 3/8 in.	00000	OBD	43
2360-0200	Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	42
2360-0201	Screw, Machine, PH, No. 6-32, 1/2 in.	00000	OBD	22
2360-0202	Screw, Machine, FH, No. 6-32, 3/8 in.	00000	OBD	56
2360-0203	Screw, Machine, PH, No. 6-32, 5/8 in.	00000	OBD	12
2360-0204	Screw, Machine, FH, No. 6-32, 3/4 in.	00000	OBD	10
2360-0205 (11)	Screw, Machine, PH, No. 6-32, 3/4 in.	00000	OBD	12
2360-0206 (5)	Screw, Machine, FH, No. 6-32, 7/8 in.	00000	OBD	6
2360-0207	Screw, Machine, PH, No. 6-32, 7/8 in.	00000	OBD	4
2360-0209	Screw, Machine, PH, No. 6-32, 1 in.	00000	OBD	4
2360-0268	Terminal Lug, No. 6	00000	OBD	1
2370-0030	Screw, Machine, FH, No. 6-32, 1-1/2 in.	00000	OBD	2
2390-0014	Screw, Machine, PH, No. 6-32, 2-1/4 in.	00000	OBD	3
2420-0001 (12) (10)	Nut, Assembled Washer, No. 6-32	00000	OBD	107
2420-0002 (9)	Nut, Plain, Hexagon, No. 6-32	00000	OBD	56
2480-0004	Nut, Plain, Hexagon, No. 8-32	00000	OBD	8
2510-0003	Nut, Assembled Washer, No. 8-32	00000	OBD	4
2510-0063	Screw, Machine, FH, No. 8-32, 1-1/2 in.	00000	OBD	2
2510-0102	Screw, Machine, FH, No. 8-32, 3/8 in.	00000	OBD	18
2510-0103	Screw, Machine, PH, No. 8-32, 3/8 in.	00000	OBD	60
2510-0106	Screw, Machine, FH, No. 8-32, 1/2 in.	00000	OBD	16
2510-0107 (13)	Screw, Machine, PH, No. 8-32, 1/2 in.	00000	OBD	46
2510-0109 (14)	Screw, Machine, PH, No. 8-32, 5/8 in.	00000	OBD	27
2510-0111	Screw, Machine, PH, No. 8-32, 3/4 in.	00000	OBD	2

Table 6-20. Total Quantity of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
2515-0016	Screw, Machine, PH, No. 8-32, 2-1/2 in.	00000	OBD	3
2530-0017	Washer, Recessed, No. 8	00000	OBD	2
2580-0003 (14)	Nut, Assembled Washer, No. 8-32	00000	OBD	12
2580-0004	Nut, Plain, Hexagon, No. 8-32	00000	OBD	14
2680-0103	Screw, Machine, PH, No. 10-32, 1/2 in.	00000	OBD	20
2680-0104	Screw, Machine, FH, No. 10-32, 1/2 in.	00000	OBD	4
2680-0108	Screw, Machine, FH, No. 10-32, 3/4 in.	00000	OBD	5
2740-0002	Nut, Plain, Hexagon, 1/4 in. ID	00000	OBD	43
2950-0004	Nut, Plain, Hexagon, 1/4-20	00000	OBD	2
2950-0024	Nut, Plain, Hexagon, 1/2-20	00000	OBD	2
2950-0035	Nut, Plain, Hexagon, 15/32-32	00000	OBD	17
3030-0248	Setscrew, No. 10-32, 3/4 in.	00000	OBD	16
3050-0002	Washer, Flat, No. 4	00000	OBD	4
3050-0088	Washer, Concave, No. 8	00000	OBD	3
3050-0098	Washer, Flat, No. 2	00000	OBD	2
3050-0139 (13)	Washer, Flat, No. 8	00000	OBD	44
3050-0225	Washer, Flat, 1/4 ID	00000	OBD	2
3050-0228 (12)	Washer, Flat, No. 6	00000	OBD	61
3050-0234	Washer, Flat, 1/4 ID	00000	OBD	8
3050-0239	Washer, Nonmetallic, No. 8	00000	OBD	17
3050-0247	Washer, Nonmetallic, No. 6	00000	OBD	13
3050-0270	Terminal Lug, No. 10	00000	OBD	3
3101-0716	Lens (RUN)	28480	3101-0716	1
3101-0717	Lens (LOAD ADDRESS)	28480	3101-0717	1
3101-0718	Lens (PRESET)	28480	3101-0718	1
3101-0719	Lens (POWER)	28480	3101-0719	1
3101-0720	Lens (SINGLE CYCLE)	28480	3101-0720	1
3101-0721	Lens (HALT)	28480	3101-0721	1
3101-0722	Lens (LOAD B)	28480	3101-0722	1
3101-0723	Lens (LOAD MEMORY)	28480	3101-0723	1
3101-0724	Lens (LOAD A)	28480	3101-0724	1
3101-0725	Lens (DISPLAY MEMORY)	28480	3101-0725	1
3130-0130	Nut, Face, 1/2 in. ID	28480	3030-0103	17
3160-0099	Fan Grille	23936	5504	4
4040-0431	Air Deflector	28480	4040-0431	1
4320-0002	Gasket, rubber	28480	4320-0002	1
4320-0043	Channel, rubber	28480	4320-0043	1
4320-0096	Extrusion, rubber	28480	4320-0096	1
5000-0131	Trim, Aluminum	28480	5000-0131	4
5000-0207	Shorting Bar	28480	5000-0207	8
5000-5722	Bracket, Mounting, Filter	28480	5000-5722	1
5000-8015 (5)	Fan Guard	28480	5000-8015	3
5020-0244	Bracket	28480	5020-0244	4
5020-1922	Spacer, Nylon	28480	5020-1922	1
5040-1464	Extractor, PC Card	28480	5040-1464	32
5060-0735	Retaining Plate, Handle	28480	5060-0735	2
5060-0763	Handle	28480	5060-0763	2
5060-6236	Rack Mounting Kit	28480	5060-6236	1
5060-8323 (15)	Cable, Power	28480	5060-8323	1
5080-1543	Component Board	28480	5080-1543	2
5080-6595	Fortran Code Pad	28480	5080-6595	1
5080-6596	Assembler Code Pad	28480	5080-6596	1

Table 6-20. Total Quantity of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
5080-6599	Absolute Block Loader	28480	5080-6599	1
7120-0134	Tag, Serial No.	28480	7120-0134	1
7120-2416	Label	28480	7120-2416	1
7120-2433	Label	28480	7120-2433	1
02115-6047	Cable, Extender	28480	02115-6047	1
02116-0002	Bracket, Transformer	28480	02116-0002	4
02116-0005	Front Panel	28480	02116-0005	1
02116-0007	Panel Brace	28480	02116-0007	2
02116-0010	Fan Panel	28480	02116-0010	1
02116-0012	Center Brace	28480	02116-0012	2
02116-0013	Side Cover	28480	02116-0013	2
02116-0014	Cover, Lower-Rear	28480	02116-0014	1
02116-0016	Cover, Top and Bottom	28480	02116-0016	2
02116-0020	Center Brace	28480	02116-0020	1
02116-0021	Right Brace	28480	02116-0021	1
02116-0022	Left Brace	28480	02116-0022	1
02116-0023	Bracket, Mounting, Bus Bar	28480	02116-0023	1
02116-0024	Housing, AC Input	28480	02116-0024	1
02116-0025	Deck, Blank, Power Supply	28480	02116-0025	1
02116-0028	Support Plate	28480	02116-0028	1
02116-0032	Bottom Panel	28480	02116-0032	1
02116-0033	Bracket, Thermal Switch	28480	02116-0033	3
02116-0047	Capacitor Board Bracket	28480	02116-0047	1
02116-0053	Connector Bracket	28480	02116-0053	2
02116-0054	Bracket, Connector	28480	02116-0054	2
02116-0056	Bracket, Diode	28480	02116-0056	2
02116-0057 (16)	Filter, Air	28480	02116-0057	2
02116-0059	Bracket, Terminal Mounting, Left	28480	02116-0059	1
02116-0060	Bracket, Terminal Mounting, Right	28480	02116-0060	1
02116-0063	Bracket, Terminal Board	28480	02116-0063	4
02116-0064	Terminal Board	28480	02116-0064	1
02116-0066	Shorting Bar	28480	02116-0066	2
02116-0067	Bus Bar	28480	02116-0067	1
02116-0068	Bus Bar	28480	02116-0068	1
02116-0069	Bus Bar	28480	02116-0069	1
02116-0073	Bus Bar, 4.5V	28480	02116-0073	1
02116-0074	Bus Bar Brace	28480	02116-0074	1
02116-0075	Bus Bar Brace	28480	02116-0075	1
02116-0077	Side Bracket	28480	02116-0077	2
02116-0078	Shield, Filter	28480	02116-0078	1
02116-0080	Subpanel	28480	02116-0080	1
02116-0085	Card Retainer	28480	02116-0085	1
02116-0087	Cable Spacer	28480	02116-0087	1
02116-0088	Filler Plate	28480	02116-0088	2
02116-0089	Top Panel	28480	02116-0089	1
02116-0090	Top Door Panel	28480	02116-0090	1
02116-0091	Bracket, Resistor	28480	02116-0091	1
02116-0092	Bus Bar, 2V	28480	02116-0092	1
02116-0093	Bus Bar (End Output)	28480	02116-0093	1
02116-0101	Subpanel	28480	02116-0101	1

Table 6-20. Total Quantity of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
02116-0102	Cable Clamp Bracket	28480	02116-0102	1
02116-0105	Fan Cover	28480	02116-0105	1
02116-01104	Top Door Panel	28480	02116-01104	1
02116-01107	Bracket	28480	02116-01107	1
02116-01108	Cover, Overvoltage Protection Assembly	28480	02116-01108	1
02116-01109	Housing, AC Input	28480	02116-01109	1
02116-01110	Side Panel, Left	28480	02116-01110	1
02116-01111	Side Panel, Right	28480	02116-01111	1
02116-01112	Plate, Top	28480	02116-01112	1
02116-01113	Back Panel, Power Supply	28480	02116-01113	1
02116-01115	Front Panel	28480	02116-01115	1
02116-01116	Transformer Cover	28480	02116-01116	1
02116-01117	Cover, AC Housing	28480	02116-01117	1
02116-01118	Cover, Upper-Rear	28480	02116-01118	1
02116-01124	Terminal Board	28480	02116-01124	1
02116-01125	Filler Plate, large	28480	02116-01125	1
02116-01126	Filler Plate, small	28480	02116-01126	1
02116-01127	Subpanel	28480	02116-01127	1
02116-01128 (5)	Filter, Air	28480	02116-01128	2
02116-2002	Slide Pin	28480	02116-2002	2
02116-2003	Eccentric Screw, No. 8	28480	02116-2003	4
02116-2005	Bezel, Upper	28480	02116-2005	1
02116-2009	Bezel, Upper	28480	02116-2009	3
02116-2010	Upper Side	28480	02116-2010	1
02116-2011	Lower Slide	28480	02116-2011	1
02116-2012	Hinged Slide	28480	02116-2012	2
02116-2013	Support Bar	28480	02116-2013	1
02116-2014	Hinged Bar	28480	02116-2014	2
02116-2015	Bearing Shaft	28480	02116-2015	8
02116-2016	Hinged Pin	28480	02116-2016	2
02116-2017	Main Frame	28480	02116-2017	2
02116-2021	Horizontal Brace	28480	02116-2021	1
02116-2022	Vertical Brace	28480	02116-2022	1
02116-2023	Insert, Catch Rod	28480	02116-2023	4
02116-2026	Horizontal Bracket	28480	02116-2026	2
02116-2027	Vertical Bracket	28480	02116-2027	2
02116-2032	Latch Retainer	28480	02116-2032	1
02116-2033	Catch Rod	28480	02116-2033	2
02116-2034	Tab Catch, Upper	28480	02116-2034	1
02116-2035	Bracket, Capacitor Board, Large	28480	02116-2035	1
02116-2040	Bezel	28480	02116-2040	1
02116-2041 (17)	Brace, Front, Lower	28480	02116-2041	1
02116-2052	Bezel, Lower	28480	02116-2052	1
02116-2055	Bus Bar, +4.5V	28480	02116-2055	1
02116-2056	Bus Bar, -20V	28480	02116-2056	1
02116-2057	Foot, Cabinet	28480	02116-2057	4
02116-2058	Bracket, Capacitor Board, Small	28480	02116-2058	1
02116-2059	Mounting Bar, Upper	28480	02116-2059	1
02116-2060	Mounting Bar, Front	28480	02116-2060	1
02116-2061	Mounting Bar, Rear	28480	02116-2061	1
02116-2063	Tab Catch, Lower	28480	02116-2063	1

Table 6-20. Total Quantity of Mechanical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
02116-2064	Mounting Bar, Lower	28480	02116-2064	1
02116-2065	Guide, Rod, Lower	28480	02116-2065	1
02116-2067	Guide, Rod, Upper	28480	02116-2067	1
02116-2068	Mount, Bus Bar	28480	02116-2068	1
02116-2069	Bakelite Spacer	28480	02116-2069	2
02116-2072	Support Bar	28480	02116-2072	1
02116-2075	PC Guide Support	28480	02116-2075	6
02116-2077 (17)	Brace, Top-Front	28480	02116-2077	1
02116-2078	Vertical Brace	28480	02116-2078	1
02116-2079	Spacer	28480	02116-2079	1
02116-2080	Door Catch	28480	02116-2080	2
02116-20831	Latch	28480	02116-20831	1
02116-4002	Light Mask	28480	02116-4002	1
02116-4007	PC Guide	28480	02116-4007	22
02116-6282	Back Panel Assembly, Card Cage	28480	02116-6282	1
02116-6295	Door Frame	28480	02116-6295	1
02116-63216	Extender Board, Single Connector	28480	02116-63216	1
02116-63223	Card Cage Assembly	28480	02116-63223	1
02116-63251	Cable, Extender	28480	02116-63251	1
02116-63266	Accessory Kit	28480	02116-63266	1
02116-8177	Decal	28480	02116-8177	1
02116-8199	Indicator, Strip, Top	28480	02116-8199	1
02116-8200	Indicator, Strip, Middle	28480	02116-8200	1
02116-8201	Indicator, Strip, Bottom	28480	02116-8201	1
02116-83231	Window, Display	28480	02116-83231	1
02116-83232	Sheet, Light Diffusion	28480	02116-83232	1
02116-91755	Manual, Volume I	28480	02116-91755	1
02116-91756	Manual, Volume II	28480	02116-91756	1
02116-91757	Manual, Volume III	28480	02116-91757	1

NOTES:

(5) First used on computers with serial number prefix 1108A.

(6) First used on computers with serial number prefix 1047A.

(8) For computers with serial number prefix 1108A and above increase the total quantity by 2.

(9) For computers with serial number prefix 1108A and above, increase the total quantity by 4.

(10) For computers with serial number prefix 1047A, decrease the total quantity by 2.

(11) For computers with serial number prefix 1108A and above, increase the total quantity by 20.

(12) For computers with serial number prefix 1108A and above, increase the total quantity by 12.

(13) For computers with serial number prefix 1108A and above, decrease the total quantity by 12.

(14) For computers with serial number prefix 1108A and above, decrease the total quantity by 4.

(15) For computers with serial number prefix below 1047A, use power cable with part number 5060-2267.

(16) Used on computers with serial number prefix below 1108A.

(17) For computers with serial numbers 1108A00276 and above, part number 02116-2041 is used for both the top and lower front brace and part number 02116-2077 is not used.

Table 6-21. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 (Name to Code) and H4-2 (Code to Name) and their latest supplements. The date of revision and the date of the supplements used appear at the bottom of each page. Alphabetical codes have been arbitrarily assigned to suppliers not appearing in the H4 Handbooks.

Code No.	Manufacturer	Address
00000	U.S.A Common	Any supplier of U.S.
00136	McCoy Electronics	Mount Holly Springs, Pa.
00213	Sage Electronics Corp.	Rochester, N.Y.
00287	Cemco, Inc.	Danielson, Conn.
00334	Humidial	Colton, Calif.
00348	Mictron, Co., Inc.	Valley Stream, N.Y.
00373	Garlock Inc.	Cherry Hill, N.J.
00656	Aerovox Corp.	New Bedford, Mass.
00779	Amp. Inc.	Harrisburg, Pa.
00781	Aircraft Radio Corp.	Boonton, N.J.
00809	Croven, Ltd.	Whitby, Ontario, Canada
00815	Northern Engineering Laboratories, Inc.	Burlington, Wis.
00853	Sangamo Electric Co., Pickens Div.	Pickens, S.C.
00866	Goe Engineering Co.	City of Industry, Cal.
00891	Carl E. Holmes Corp.	Los Angeles, Cal.
00929	Microlab Inc.	Livingston, N.J.
01002	General Electric Co., Capacitor Dept.	Hudson Falls, N.Y.
01009	Alden Products Co.	Brockton, Mass.
01121	Allen Bradley Co.	Milwaukee, Wis.
01255	Litton Industries, Inc.	Beverly Hills, Cal.
01281	TRW Semiconductors, Inc.	Lawndale, Cal.
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas
01349	The Alliance Mfg. Co	Alliance, Ohio
01538	Small Parts Inc.	Los Angeles, Cal.
01589	Pacific Relays, Inc.	Van Nuys, Cal.
01670	Gudebrod Bros. Silk Co.	New York, N.Y.
01930	Amerock Corp.	Rockford, Ill.
01960	Pulse Engineering Co	Santa Clara, Cal.
02114	Ferroxcube Corp. of America	Saugerties, N.Y.
02116	Wheelock Signals, Inc.	Long Branch, N.J.
02286	Cole Rubber and Plastics Inc	Sunnyvale, Cal.
02660	Amphenol-Borg Electronics Corp.	Broadview, Ill.
02735	Radio Corp. of America, Semiconductor and Materials Division	Somerville, N.J.
02771	Vocaline Co. of America, Inc.	Old Saybrook, Conn.
02777	Hopkins EngineeringCo.	San Fernando, Cal.
02875	Hudson Tool & Die	Newark, N.J.
03296	Nylon Molding Corp.	Springfield, N.J.
03508	G.E. Semiconductor Prod. Dept.	Syracuse, N.Y.
03705	Apex Machine & Tool Co.	Dayton, Ohio
03797	Eldema Corp.	Compton, Calif.
03818	Parker Seal Co.	Los Angeles, Cal.
03877	Transitron Electric Corp.	Wakefield, Mass.
03888	Pyrofilm Resistor Co., Inc.	Cedar Knolls, N.J.
03954	Singer Co., Diehl Div., Finderne Plant	Sumerville, N.J.
04009	Arrow, Hart and Hegeman Elect. Co.	Hartford, Conn.
04013	Taruus Corp.	Lambertville, N.J.
04062	Arco Electronic Inc.	Great Neck, N.Y.
04217	Essex Wire	Los Angeles, Cal.
04222	Hi-Q Division of Aerovox.	Myrtle Beach, S.C.
04354	Precision Paper Tube Co.	Wheeling, Ill.
04404	Palo Alto Division of Hewlett-Packard Co.	Palo Alto, Cal.
04651	Sylvania Electric Products, Microwave Device Div.	Mountain View, Cal.
04673	Dakota Engr. Inc.	Culver City, Cal.
04713	Motorola Inc. Semiconductor Prod. Div.	Phoenix, Arizona
04732	Filtron Co., Inc. Western Div.	Culver City, Cal.
04773	Automatic Electric Co.	Northlake, Ill.
04796	Sequoia Wire Co.	Redwood City, Cal.
04811	Precision Coil Spring Co.	El Monte, Cal.
04870	P.M. Motor Company	Westchester, Ill.
04919	Component Mfg. Service Co.	W. Bridgewater, Mass.
05006	Twentieth Century Plastics, Inc.	Los Angeles, Cal.
05277	Westinghouse Electric Corp. Semiconductor Dept.	Youngwood, Pa.
05347	Ultronix, Inc.	San Mateo, Cal.
05397	Union Carbine Corp., Elect. Div.	New York, N.Y.
05574	Viking Ind. Inc.	Canoga Park, Cal.
05593	Icore Electro-Plastics Inc.	Sunnyvale, Cal.
05616	Cosmo Plastic (c/o Electrical Spec. Co.)	Cleveland, Ohio
05624	Barber Colman Co.	Rockford, Ill.
05728	Tiffen Optical Co.	Roslyn Heights, Long Island, N.Y.
05729	Metro-Tel Corp.	Westbury, N.Y.
05783	Stewart Engineering Co.	Santa Cruz, Cal.
05820	Wakefield Engineering Inc.	Wakefield, Mass.
06004	Bassick Co., Div. of Stewart Warner Corp.	Bridgeport, Conn.
06090	Raychem Corp.	Redwood City, Cal.
06175	Bausch and Lomb Optical Co.	Rochester, N.Y.
06402	E.T.A. Products Co. of America	Chicago, Ill.
06540	Amatom Electronic Hardware Co., Inc.	New Rochelle, N.Y.
06555	Beede Electrical Instrument Co., Inc.	Penacook, N.H.
06666	General Devices Co., Inc.	Indianapolis, Ind.
06751	Components Inc., Ariz. Div.	Phoenix, Arizona
06812	Torrington Mfg. Co., West Div.	Van Nuys, Cal.
06980	Varian Assoc. Etmac Div.	San Carlos, Cal.
07088	Kelvin Electric Co.	Van Nuys, Cal.
07126	Digitran Co.	Pasadena, Cal.
07137	Transistor Electronics Corp.	Minneapolis, Minn.
07138	Westinghouse Electric Corp., Electronic Tube Div.	Elmira, N.Y.
07149	Filmohm Corp.	New York, N.Y.
07233	Cinch-Graphik Co.	City of Industry, Cal.
07256	Silicon Transistor Corp.	Carle Place, N.Y.
07261	Avnet Corp.	Culver City, Cal.
07263	Fairchild Camera & Inst. Corp., Semiconductor Div.	Mountain View, Cal.
07322	Minnesota Rubber Co.	Minneapolis, Minn.
07387	Birtcher Corp, The	Monterey Park, Cal.
07397	Sylvania Elect. Prod. Inc., Mt. View Operations	Mountain View, Cal.
07700	Technical Wire Products Inc.	Cranford, N.J.
07829	Bodine Elect. Co.	Chicago, Ill.
07910	Continental Device Corp.	Hawthorne, Cal.
07933	Raytheon Mfg. Co., Semiconductor Div.	Mountain View, Cal.
07980	Hewlett-Packard Co., New Jersey Division	Rockaway, N.J.
08145	U.S. Engineering Co.	Los Angeles, Cal.
08289	Blinn, Delbert Co.	Pomona, Cal.
08358	Burgess Battery Co.	Niagara Falls, Ontario, Canada
08524	Deutsch Fastener Corp.	Los Angeles, Cal.
08664	Bristol Co., The	Waterbury, Conn
08717	Sloan Company	Sun Valley, Cal.
08718	ITT Cannon Electric Inc., Phoenix Div.	Phoenix, Arizona
08727	National Radio Lab. Inc.	Paramus, N.J.
08792	CBS Electronics Semiconductor Operations, Div. of CBS Inc	Lowell, Mass.
08806	General Electric Co., Miniature Lamp Dept.	Cleveland, Ohio
08984	Mel-Rain	Indianapolis, Ind.
09026	Babcock Relays Div.	Costa Mesa, Cal.
09097	Electronic Enclosures Inc.	Los Angeles, Calif.
09134	Texas Capacitor Co.	Houston, Texas
09145	Tech. Ind. Inc. Atohm Elect.	Burbank, Cal.
09250	Electro Assemblies, Inc.	Chicago, Ill.
09353	C & K Components Inc.	Newton, Mass.
09569	Mallory Battery Co. of Canada, Ltd.	Toronto, Ontario, Canada
09795	Pennsylvania Florocarbon.	Clifton Heights, Penn.
09922	Burndy Corp	Norwalk, Conn.
10214	General Transistor Western Corp.	Los Angeles, Cal.
10411	Ti-Tal, Inc.	Berkeley, Cal.
10646	Carborundum Co.	Niagara Falls, N.Y.
11236	CTS of Berne, Inc.	Berne, Ind.
11237	Chicago Telephone of California, Inc.	So. Pasadena, Cal.
11242	Bay State Electronics Corp.	Waltham, Mass.
11312	Teledyne Inc., Microwave Div.	Palo Alto, Cal.
11314	National Seal	Downey, Cal.
11453	Precision Connector Corp.	Jamaica, N.Y.
11534	Duncan Electronics Inc.	Costa Mesa, Cal.
11711	General Instrument Corp., Semiconductor Division Products Group	Newark, N.J.
11717	Imperial Electronic, Inc.	Buena Park, Cal.
11870	Melabs, Inc.	Palo Alto, Cal.
12136	Philadelphia Handle Co.	Camden, N.J.
12361	Grove Mfg. Co., Inc.	Shady Grove, Pa.
12574	Gulton Ind. Inc., Data System Div.	Albuquerque, N.M.
12697	Clarostat Mfg. Co.	Dover, N.H.
12728	Elmar Filter Corp	W. Haven, Conn.
12859	Nippon Electric Co., Ltd.	Tokyo, Japan
12881	Metex Electronics Corp.	Clark, N.J.
12930	Delta Semiconductor Inc.	Newport Beach, Cal.
12954	Dickson Electronics Corp.	Scottsdale, Arizona
13019	Airco Supply Co., Inc.	Witchita, Kansas
13061	Wilco Products	Detroit, Mich.
13103	Thermolloy	Dallas, Texas
13327	Solitron Devices Inc.	Tappan, N.Y.
13396	Telefunken (GmbH)	Hanover, Germany
13835	Midland-Wright Div. of Pacific Industries, Inc.	Kansas City, Kansas
14099	Sem-Tech	Newbury Park, Cal.
14193	Calif. Resistor Corp	Santa Monica, Cal.
14298	American Components, Inc.	Conshohocken, Pa.
14433	ITT Semiconductor, a Div. of Int. Telephone and Telegraph Corporation	West Palm Beach, Fla.
14493	Hewlett-Packard Company.	Loveland, Colo.
14655	Cornell Dublier Electric Corp	Newark, N.J.
14674	Corning Glass Works	Corning, N.Y.
14752	Electro Cube Inc.	San Gabriel, Cal.
14960	Williams Mfg. Co.	San Jose, Cal.
15106	The Sphere Co., Inc.	Little Falls, N.J.
15203	Webster Electronics Co.	New York, N.Y.
15287	Scionics Corp.	Northridge, Cal.
15291	Adjustable Bushing Co.	N. Hollywood, Cal.
15558	Micron Electronics.	Garden City, Long Island, N.Y.
15566	Amprobe Inst. Corp.	Lynbrook, N.Y.
15631	Cabletronics	Costa Mesa, Cal.
15772	Twentieth Century Coil Spring Co.	Santa Clara, Cal.
15801	Fenwal Elect. Inc.	Framingham, Mass.
15818	Amelco Inc.	Mountain View, Cal.
16037	Spruce Pine Mica Co.	Spruce Pine, N.C.
16179	Omni-Spectra Inc.	Detroit, Ill.
16352	Computer Diode Corp.	Lodi, N.J.
16554	Electroid Co.	Union, N.J.
16585	Boots Aircraft Nut Corp.	Pasadena, Cal.
16688	Ideal Prec. Meter Co., Inc., De Jur Meter Div.	Brooklyn, N.Y.
16758	Delco Radio Div. of G.M. Corp.	Kokomo, Ind.
17109	Thermonetics Inc.	Canoga Park, Cal.
17474	Tranex Company	Mountain View, Cal.
17675	Hamlin Metal Products Corp.	Akron, Ohio
17745	Angstrohm Prec. Inc.	No. Hollywood, Cal.
17856	Siliconix Inc.	Sunnyvale, Cal.
17870	McGraw-Edison Co.	Manchester, N.H.
18042	Power Design Pacific Inc.	Palo Alto, Cal.
18083	Clevite Corp. Semiconductor Div.	Palo Alto, Cal.
18324	Signetics Corp.	Sunnyvale, Cal.
18476	Ty-Car Mfg. Co., Inc.	Holliston, Mass.
18486	TRW Elect. Comp. Div.	Des Plaines, Ill.
18565	Chomerics	Plainville, Mass.
18583	Curtis Instrument, Inc.	Mt. Kisco, N.Y.
18612	Vishay Instruments Inc.	Malvern, Pa.
18873	E.I. DuPont and Co., Inc.	Wilmington, Del.
18911	Durant Mfg. Co.	Milwaukee, Wis.
19315	The Bendix Corp., Navigation & Control Div.	Teterboro, N.J.
19500	Thomas A. Edison Industries, Div. of McGraw-Edison	West Orange, N.J.
19589	Concoa	Baldwin Park, Cal.

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From: Handbook Supplements
H4-1 Dated January 1970

Table 6-21. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address
19644	LRC Electronics	Horseheads, N.Y.
19701	Electra Mfg. Co.	Independence, Kansas
20183	General Atronics Corp.	Philadelphia, Pa.
21226	Executone, Inc.	Long Island City, N.Y.
21355	Fafnir Bearing Co., The	New Britian, Conn.
21520	Fansteel Metallurgical Corp.	N. Chicago, Ill.
23020	General Reed Co.	Metuchen, N.J.
23042	Texscan Corp.	Indianapolis, Ind.
23783	British Radio Electronics Ltd.	Washington, D.C.
24455	G.E. Lamp Division, Nela Park	Cleveland, Ohio
24655	General Radio Co.	West Concord, Mass.
24681	Memcor Inc., Comp. Div.	Huntington, Ind.
26365	Gries Reproducer Corp.	New Rochelle, N.Y.
26462	Grobert File Co. of America, Inc.	Carlstadt, N.J.
26851	Compac Hollister Co.	Hollister, Cal.
26992	Hamilton Watch Co.	Lancaster, Pa.
28480	Hewlett-Packard Co.	Palo Alto, Cal.
28520	Heyman Mfg. Co.	Kenilworth, N.J.
30817	Instrument Specialties Co., Inc.	Little Falls, N.J.
33173	G.E. Receiving Tube Dept.	Owensboro, Ky.
35434	Lectrohm Inc.	Chicago, Ill.
36196	Stanwyck Coil Products, ltd.	Hawkesbury, Ontario, Canada
36287	Cunningham, W.H. & Hill, Ltd.	Toronto, Ontario, Canada
37942	P.R. Mallory & Co., Inc.	Indianapolis, Ind.
39543	Mechanical Industries Prod. Co.	Akron, Ohio
40920	Miniature Precision Bearings, Inc.	Keene, N.H.
40931	Honeywell Inc.	Minneapolis, Minn.
42190	Muter Co.	Chicago, Ill.
43990	C.A. Norgren Co.	Englewood, Colo.
44655	Ohmite Mfg. Co.	Skokie, Ill.
46384	Penn Eng. & Mfg. Corp.	Doylestown, Pa.
47904	Polaroid Corp.	Cambridge, Mass.
48620	Precision Thermometer & Inst. Co.	Southampton, Pa.
49956	Microwave & Power Tube Div.	Waltham, Mass.
52090	Rowan Controller Co.	Westminster, Md.
52983	HP Co., Med. Elec. Div.	Waltham, Mass.
54294	Shallcross Mfg. Co.	Selma, N.C.
55026	Simpson Electric Co.	Chicago, Ill.
55933	Sonotone Corp.	Elmsford, N.Y.
55938	Raytheon Co. Commercial Apparatus & System Div.	So. Norwalk, Conn.
56137	Spaulding Fibre Co., Inc.	Tonawanda, N.Y.
56289	Sprague Electric Co.	North Adams, Mass.
58474	Superior Elect. Co.	Bristol, Conn.
59446	Telex Corp.	Tulsa, Okla.
59730	Thomas & Betts Co.	Elizabeth, N.J.
60741	Triplett Electrical Inst. Co.	Bluffton, Ohio
61775	Union Switch and Signal Div. of Westinghouse Air Brake Co.	Pittsburgh, Pa.
62119	Universal Electric Co.	Owosso, Mich.
63743	Ward-Leonard Electric Co.	Mt. Vernon, N.Y.
64959	Western Electric Co., Inc.	New York, N.Y.
65092	Weston Inst. Inc. Weston-Newark	Newark, N.J.
66295	Wittek Mfg. Co.	Chicago, Ill.
66346	Minnesota Mining & Mfg. Co. Revere Mincom Div.	St. Paul, Minn.
70276	Allen Mfg. Co.	Hartford, Conn.
70309	Allied Control	New York, N.Y.
70318	Allmetal Screw Product Co., Inc.	Garden City, N.Y.
70417	Amplex, Div. of Chrysler Corp.	Detroit, Mich.
70485	Atlantic India Rubber Works, Inc.	Chicago, Ill.
70563	Amperite Co., Inc.	Union City, N.J.
70674	ADC Products Inc.	Minneapolis, Minn.
70903	Belden Mfg. Co.	Chicago, Ill.
70998	Bird Electric Corp.	Cleveland, Ohio
71002	Birnbach Radio Co.	New York, N.Y.
71034	Bliley Electric Co., Inc.	Erie, Pa.
71041	Boston Gear Works Div. of Murray Co. of Texas	Quincey, Mass.
71218	Bud Radio, Inc.	Willoughby, Ohio
71279	Cambridge Thermionics Corp.	Cambridge, Mass.
71286	Camloc Fastener Corp.	Paramus, N.J.
71313	Cardwell Condenser Corp.	Lindenhurst, L.I., N.Y.
71400	Bussmann Mfg. Div. of McGraw-Edison Co.	St. Louis, Mo.
71436	Chicago Condenser Corp.	Chicago, Ill.
71447	Calif. Spring Co., Inc.	Pico-Rivera, Cal.
71450	CTS Corp.	Elkhart, Ind.
71468	ITT Cannon Electric Inc.	Los Angeles, Cal.
71471	Cinema, Div. Aerovox Corp.	Burbank, Cal.
71482	C.P. Clare & Co.	Chicago, Ill.
71590	Centralab Div. of Globe Union Inc.	Milwaukee, Wis.
71616	Commercial Plastics Co.	Chicago, Ill.
71700	Cornish Wire Co., The	New York, N.Y.
71707	Coto Coil Co., Inc.	Providence, R.I.
71744	Chicago Miniature Lamp Works	Chicago, Ill.
71785	Cinch Mfg. Co., Howard B. Jones Div.	Chicago, Ill.
71984	Dow Corning Corp.	Midland, Mich.
72136	Electro Motive Mfg. Co., Inc.	Willimantic, Conn.
72619	Dialight Corp.	Brooklyn, N.Y.
72656	Indiana General Corp., Electronics Div.	Keasby, N.J.
72699	General Instrument Corp., Cap Division	Newark, N.J.
72765	Drake Mfg. Co.	Harwood Heights, Ill.
72825	Hugh H. Eby Inc.	Philadelphia, Pa.
72928	Gudeman Co.	Chicago, Ill.
72962	Elastic Stop Nut Corp.	Union, N.J.
72964	Robert M. Hadley Co.	Los Angeles, Cal.
72982	Erie Technological Products, Inc.	Erie, Pa.
73061	Hansen Mfg. Co., Inc.	Princeton, Ind.
73076	H.M. Harper Co.	Chicago, Ill.
73138	Helipot Div. of Beckman Inst., Inc.	Fullerton, Cal.
73293	Hughes Products Division of Hughes Aircraft Co.	Newport Beach, Cal.
73445	Amperex Elect. Co.	Hicksville, L.I., N.Y.
73506	Bradley Semiconductor Corp.	New Haven, Conn.
73559	Carling Electric, Inc.	Hartford, Conn.
73586	Circle F Mfg. Co.	Trenton, N.J.
73682	George K. Garrett Co., Div. MSL Industries, Inc.	Philadelphia, Pa.
73734	Federal Screw Products, Inc.	Chicago, Ill.
73743	Fischer Special Mfg. Co.	Cincinnati, Ohio
73793	General Industries Co., The	Elyria, Ohio
73846	Goshen Stamping & Tool Co.	Goshen, Ind.
73899	JFD Electronics Corp.	Brooklyn, N.Y.
73905	Jennings Radio Mfg. Corp.	San Jose, Cal.
73957	Groove-Pin Corp.	Ridgefield, N.J.
74276	Signalite Inc.	Neptune, N.J.
74455	J.H. Winns, and Sons	Winchester, Mass.
74861	Industrial Condenser Corp.	Chicago, Ill.
74868	R.F. Products Division of Amphenol-Borg Electronic Corp.	Danbury, Conn.
74970	E.F. Johnson Co.	Waseca, Minn.
75042	International Resistance Co.	Philadelphia, Pa.
75263	Keystone Carbon Co., Inc.	St. Marys, Pa.
75378	CTS Knights, Inc.	Sandwich, Ill.
75382	Kulka Electric Corp.	Mt. Vernon, N.Y.
75818	Lenz Electric Mfg. Co.	Chicago, Ill.
75915	Littlefuse, Inc.	Des Plaines, Ill.
76005	Lord Mfg. Co.	Erie, Pa.
76210	C.W. Marwedel	San Francisco, Cal.
76433	General Instrument Corp., Micamold Division	Newark, N.J.
76487	James Millen Mfg. Co., Inc.	Malden, Mass.
76493	J.W. Miller Co.	Los Angeles, Cal.
76530	Cinch-Monadnock, Div. of United Carr Fastener Corp.	San Leandro, Cal.
76545	Mueller Electric Co.	Cleveland, Ohio
76703	National Union	Newark, N.J.
76854	Oak Manufacturing Co.	Crystal Lake, Ill.
77068	The Bendix Corp., Electrodynamics Div.	N. Hollywood, Cal.
77075	Pacific Metals Co.	San Francisco, Cal.
77221	Phaostron Instrument and Electronic Co.	So. Pasadena, Cal.
77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.
77342	American Machine & Foundry Co. Potter & Brumfield Div.	Princeton, Ind.
77630	TRW Electronic Components Div.	Camden, N.J.
77638	General Instrument Corp., Rectifier Division	Brooklyn, N.Y.
77764	Resistance Products Co.	Harrisburg, Pa.
77969	Rubbercraft Corp. of Calif.	Torrance, Cal.
78189	Shakeproof Division of Illinois Tool Works	Elgin, Ill.
78277	Sigma	So. Braintree, Mass.
78283	Signal Indicator Corp.	New York, N.Y.
78290	Struthers-Dunn Inc.	Pitman, N.J.
78452	Thompson-Bremer & Co.	Chicago, Ill.
78471	Tilley Mfg. Co.	San Francisco, Cal.
78488	Stackpole Carbon Co.	St. Marys, Pa.
78493	Standard Thomson Corp.	Waltham, Mass.
78553	Tinnerman Products, Inc.	Cleveland, Ohio
78790	Transformer Engineers	San Gabriel, Cal.
78947	Ucinite Co.	Newtonville, Mass.
79136	Waldes Kohinoor Inc.	Long Island City, N.Y.
79142	Veeder Root, Inc.	Hartford, Conn.
79251	Wenco Mfg. Co.	Chicago, Ill.
79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.
79963	Zierick Mfg. Corp.	New Rochelle, N.Y.
80031	Mepco Division of Sessions Clock Co.	Morristown, N.J.
80033	Prestole Corp.	Toledo, Ohio
80120	Schnitzer Alloy Products Co.	Elizabeth, N.J.
80131	Electronic Industries Association. Standard tube or semi-conductor device, any manufacturer.	
80207	Unimax Switch, Div. Maxon Electronics Corp.	Wallingford, Conn.
80223	United Transformer Corp.	New York, N.Y.
80248	Oxford Electric Corp.	Chicago, Ill.
80294	Bourns Inc.	Riverside, Cal.
80411	Arco Div. of Robertshaw Controls Co.	Columbus, Ohio
80486	All Star Products Inc.	Defiance, Ohio
80509	Avery Label Co.	Monrovia, Cal.
80583	Hammarlund Co., Inc.	Mars Hill, N.C.
80640	Stevens, Arnold, Co., Inc.	Boston, Mass.
80813	Dimco Gray Co.	Dayton, Ohio
81030	International Inst. Inc.	Orange, Conn.
81073	Grayhill Co.	LaGrange, Ill.
81095	Triad Transformer Corp.	Venice, Cal.
81312	Winchester Elec. Div. Litton Ind., Inc.	Oakville, Conn.
81349	Military Specification	
81483	International Rectifier Corp.	El Segundo, Cal.
81541	Airpax Electronics, Inc.	Cambridge, Maryland
81860	Barry Controls, Div. Barry Wright Corp.	Watertown, Mass.
82042	Carter Precision Electric Co.	Skokie, Ill.
82047	Sperti Faraday Inc., Copper Hewitt Electric Div.	Hoboken, N.J.
82116	Electric Regulator Corp.	Norwalk, Conn.
82142	Jeffers Electronics Division of Speer Carbon Co.	Du Bois, Pa.
82170	Fairchild Camera & Inst. Corp., Space & Defense Systems Div.	Paramus, N.J.
82209	Magnetic Industries, Inc.	Greenwich, Conn.
82219	Sylvania Electric Prod., Inc. Electronic Tube Division	Emporium, Pa.
82376	Astron Corp.	East Newark, Harrison, N.J.
82389	Switchcraft, Inc.	Chicago, Ill.
82647	Metals & Controls Inc., Spencer Products	Attleboro, Mass.
82768	Phillips-Advance Control Co.	Joliet, Ill.
82866	Research Products Corp.	Madison, Wis.
82877	Rolton Mfg. Co., Inc.	Woodstock, N.Y.
82893	Vector Electronic Co.	Glendale, Cal.
83058	Carr Fastener Co.	Cambridge, Mass.
83086	New Hampshire Ball Bearing, Inc.	Peterborough, N.H.
83125	General Instrument Corp., Capacitor Div.	Darlington, S.C.
83148	ITT Wire and Cable Div.	Los Angeles, Cal.
83186	Victory Eng. Corp.	Springfield, N.J.
83298	Bendix Corp., Red Bank Div.	Red Bank, N.J.
83315	Hubbell Corp.	Mundelein, Ill.
83324	Rosan Inc.	Newport Beach, Cal.
83330	Smith, Herman H., Inc.	Brooklyn, N.Y.
83332	Tech Labs	Palisades Park, N.J.
83385	Central Screw Co.	Chicago, Ill.
83501	Gavitt Wire and Cable Co., Div. of Amerace Corp.	Brookfield, Mass.
83594	Burroughs Corp., Electronic Tube Div.	Plainfield, N.J.
83740	Union Carbide Corp., Consumer Prod. Div.	New York, N.Y.
83777	Model Eng. and Mfg., Inc.	Huntington, Ind.
83821	Loyd Scruggs Co.	Festus, Mo.
83942	Aeronautical Inst. & Radio Co.	Lodi, N.J.
84171	Arco Electronics Inc.	Great Neck, N.Y.
84396	A.J. Glesener Co., Inc.	San Francisco, Cal.
84411	TRW Capacitor Div.	Ogallala, Neb.

Table 6-21. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address
94870	Sarkes Tarzian, Inc.	Bloomington, Ind.
85454	Boonton Molding Company	Boonton, N.J.
85471	A.B. Boyd Co.	San Francisco, Cal.
85474	R.M. Bracamonte & Co.	San Francisco, Cal.
85660	Koiled Kords, Inc.	Hamden, Conn.
85911	Seamless Rubber Co.	Chicago, Ill.
86174	Fafnir Bearing Co.	Los Angeles, Calif.
86197	Clifton Precision Products Co., Inc.	Clifton Heights, Pa.
86579	Precision Rubber Products Corp.	Dayton, Ohio
86684	Radio Corp. of America, Electronic Comp. & Devices Division	Harrison, N.J.
86928	Seastrom Mfg. Co.	Glendale, Cal.
87034	Marco Industries	Anaheim, Cal.
87216	Philco Corporation (Lansdale Division)	Lansdale, Pa.
87473	Western Fibrous Glass Products Co.	San Francisco, Cal.
87664	Van Waters & Rogers Inc.	San Francisco, Cal.
87930	Tower Mfg. Corp.	Providence, R.I.
88140	Cutler-Hammer, Inc.	Lincoln, Ill.
88220	Gould-National Batteries, Inc.	St. Paul, Minn.
88698	General Mills, Inc.	Buffalo, N.Y.
89221	Graybar Electric Co.	Oakland, Cal.
89473	G.E. Distributing Corp.	Schenectady, N.Y.
89479	Security Co.	Detroit, Mich.
89665	United Transformer Co.	Chicago, Ill.
90030	United Shoe Machinery Corp.	Beverly, Mass.
90179	U.S. Rubber Co., Consumer Ind. & Plastics Prod. Div.	Passaic, N.J.
90365	Belleville Speciality Tool Mfg., Inc.	Belleville, Ill.
90763	United Carr Fastener Corp.	Chicago, Ill.
90970	Bearing Engineering Co.	San Francisco, Cal.
91146	ITT Cannon Elect. Inc., Salem Div.	Salem, Mass.
91260	Connor Spring Mfg. Co.	San Francisco, Cal.
91345	Miller Dial & Nameplate Co.	El Monte, Cal.
91418	Radio Materials Co.	Chicago, Ill.
91506	Augat Inc.	Attleboro, Mass.
91637	Dale Electronics, Inc.	Columbus, Nebr.
91662	Elco Corp.	Willow Grove, Pa.
91673	Epiphone Inc.	New York, N.Y.
91737	Gremar Mfg. Co., Inc.	Wakefield, Mass.
91827	K F Development Co.	Redwood City, Cal.
91886	Malco Mfg., Inc.	Chicago, Ill.
91929	Honeywell Inc., Micro Switch Division	Freeport, Ill.
91961	Nahm-Bros. Spring Co.	Oakland, Cal.
92180	Tru-Connector Corp.	Peabody, Mass.
92367	Elgeet Optical Co., Inc.	Rochester, N.Y.
92607	Tensolite Insulated Wire Co., Inc.	Tarrytown, N.Y.
92702	IMC Magnetics Corp.	Westbury, L.I., N.Y.
92966	Hudson Lamp Co.	Kearney, N.J.
93332	Sylvania Electric Prod. Inc., Semiconductor Div.	Woburn, Mass.
93369	Robbins & Myers Inc.	Pallisades Park, N.J.
93410	Stemco Controls, Div. of Essex Wire Corp.	Mansfield, Ohio
93632	Waters Mfg. Co.	Culver City, Cal.
93929	G.V. Controls	Livingston, N.J.
94137	General Cable Corp.	Bayonne, N.J.
94144	Raytheon Co., Comp. Div., Ind. Comp. Operations	Quincy, Mass.
94148	Scientific Electronics Products, Inc.	Loveland, Colo.
94154	Wagner Elect. Corp., Tung-Sol Div.	Newark, N.J.
94197	Curtiss-Wright Corp., Electronics Div.	East Patterson, N.J.
94222	South Chester Corp.	Chester, Pa.
94330	Wire Cloth Products, Inc.	Bellwood, Ill.
94375	Automatic Metal Products Co.	Brooklyn, N.Y.
94682	Worcester Pressed Aluminum Corp.	Worcester, Mass.
94696	Magnecraft Electric Co.	Chicago, Ill.
95023	George A. Philbrick Researchers, Inc.	Boston, Mass.
95146	Alco Elect. Mfg. Co.	Lawrence, Mass.
95236	Allies Products Corp.	Diania, Fla.
95238	Continental Connector Corp.	Woodside, N.Y.
95263	Leecraft Mfg. Co., Inc.	Long Island, N.Y.
95265	National Coil Co.	Sheridan, Wyo.
95275	Vitramon, Inc.	Bridgeport, Conn.
95348	Gordos Corp.	Bloomfield, N.J.
95354	Methode Mfg. Co.	Rolling Meadows, Ill.
95566	Arnold Engineering Co.	Marengo, Ill.
95712	Dage Electric Co., Inc.	Franklin, Ind.
95984	Siemon Mfg. Co.	Wayne, Ill.
95987	Weckesser Co.	Chicago, Ill.
96067	Microwave Assoc., West, Inc.	Sunnyvale, Cal.
96095	Hi-Q Div. of Aerovox Corp.	Olean, N.Y.
96256	Thordarson-Meissner Inc.	Mt. Carmel, Ill.
96296	Solar Mfg. Co.	Los Angeles, Cal.
96396	Microswitch, Div. of Minn.-Honeywell	Freeport, Ill.
96330	Carlton Screw Co.	Chicago, Ill.
96341	Microwave Associates, Inc.	Burlington, Mass.
96501	Excel Transformer Co.	Oakland, Cal.
96508	Xcelite, Inc.	Orchard Park, N.Y.
96733	San Fernando Elec. Mfg. Co.	San Fernando, Cal.
96881	Thomson Ind. Inc.	Long Island, N.Y.
97464	Industrial Retaining Ring Co.	Irvington, N.J.
97539	Automatic & Precision Mfg.	Englewood, N.J.
97979	Reon Resistor Corp.	Yonkers, N.Y.
97983	Litton System Inc., Adler-Westrex Commun. Div.	New Rochelle, N.Y.
98141	R-Tronics, Inc.	Jamaica, N.Y.
98159	Rubber Teck, Inc.	Gardena, Cal.
98220	Hewlett-Packard Co., Medical Elec. Div.	Pasadena, Cal.
98278	Microdot, Inc.	So. Pasadena, Cal.
98291	Sealectro Corp.	Mamaronech, N.Y.
98376	Zero Mfg. Co.	Burbank, Cal.
98410	Etc Inc.	Cleveland, Ohio
98731	General Mills Inc., Electronics Div.	Minneapolis, Minn.
98734	Paeco Division of Hewlett-Packard Co.	Palo Alto, Cal.
98821	North Hills Electronics, Inc.	Glen Cove, N.Y.
98978	International Electronic Research Corp.	Burbank, Cal.
99109	Columbia Technical Corp.	New York, N.Y.
99313	Varian Associates	Palo Alto, Cal.
99378	Atlee Corp.	Winchester, Mass.
99515	Marshall Ind., Capacitor Div.	Monrovia, Cal.
99707	Control Switch Division, Controls Co. of America	El Segundo, Cal.
99800	Delevan Electronics Corp.	East Aurora, N.Y.
99848	Wilco Corporation	Indianapolis, Ind.
99928	Branson Corp.	Whippany, N.J.
99934	Rembrandt, Inc.	Boston, Mass.
99942	Hoffman Electronics Corp., Semiconductor Division	El Monte, Cal.
99957	Technology-Instrument Corp. of California	Newbury Park, Cal.

The following HP Vendors have no number assigned in the latest supplement to the Federal Supply Code for Manufacturers Handbook.

0000F	Malco Tool and Die	Los Angeles, Calif.
0000Z	Willow Leather Products Corp.	Newark, N.J.
000AB	ETA	England
000BB	Precision Instrument Comp. Co.	Van Nuys, Cal.
000CS	Hewlett-Packard Co., Colorado Springs Div.	Colorado Springs, Colorado
000MM	Rubber Eng. & Development	Hayward, Cal.
000NN	A "N" D Mfg. Co.	San Jose, Cal.
000QQ	Cooltron	Oakland, Cal.
000WW	California Eastern Lab	Burlington, Cal.
000YY	S.K. Smith Co.	Los Angeles, Cal.

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SECTION VII

DIAGRAMS

7-1. INTRODUCTION.

7-2. This section contains diagrams to assist in trouble-shooting or adjusting the computer. Included are various tables, which augment the information in the illustrations.

7-3. The diagrams are of three types: microcircuit and integrated circuit pack diagrams, schematic diagrams, and parts location diagrams. There are five types of tables: an integrated-circuit characteristics table, signal index, backplane wire list, signal lists, and reference designation indexes.

7-4. MICROCIRCUIT AND INTEGRATED CIRCUIT DIAGRAMS.

7-5. Microcircuit and integrated circuit diagrams are contained in figure 7-1. This figure illustrates the internal circuits and pin connections for each type of encapsulated circuit used in the computer. In the reference designation indexes and in the circuit diagrams that follow, the reference designations "MC" and "U" are used interchangeably to indicate either microcircuits or integrated circuits. Each diagram in figure 7-1 is identified by a part number placed over the top of the diagram. These part numbers can be associated to particular reference designations by referring to the reference designation indexes and circuit diagrams. Integrated logic circuits are further identified by a characteristic number placed under the diagram. This number is used in table 7-1 to identify the input and output levels, open circuit logic level, and propagation delay for each integrated circuit.

7-6. SCHEMATIC DIAGRAMS.

7-7. This section contains schematic diagrams for each type of plug-in, printed-circuit card used in the computer, for the power supply, and for the door assembly. These diagrams are presented in the numerical sequence of the assembly reference designation numbers except where an assembly is used in more than one location. Multiple use assemblies are presented in sequence by their lowest reference designation number with all applicable reference designation numbers being listed in the figure title. The schematic diagrams use conventional schematic symbols to depict analog circuit components. Logic symbols used on diagrams are described in appendix A.

7-8. PARTS LOCATION DIAGRAMS.

7-9. The parts location diagrams show the appearance of each electronic assembly in the computer, and the location of each electronic component on the assembly. For the locations of the assemblies themselves, refer to figures 1-3, 1-4, and 1-5, or (for circuit cards) refer to figure 7-2 and 7-3.

7-10. The location of each backplane electrical connector (card slot) is shown in figures 7-2 and 7-3.

7-11. With the exception of card cage circuit cards and backplane connectors, each parts location diagram shows connections to other assemblies. Only connection to the next assembly is shown; from the next assembly further connection may be made to other units. For full wiring information, refer to tables 7-2 and 7-3 and to figures 7-34, 7-37, and 7-38.

7-12. Connections to card cage circuit cards are furnished in the backplane wiring list and signal lists, which are described in later paragraphs.

7-13. INTEGRATED CIRCUIT CHARACTERISTICS.

7-14. Table 7-1 provides characteristics for integrated logic circuits shown in figure 7-1. In figure 7-1, a characteristic number is provided below each integrated circuit diagram. This characteristic number is matched with a number in the characteristic column of table 7-1. The integrated circuit characteristics appear on a horizontal line with the characteristic number. As a rule, logic levels less than 1 volt are considered logic "0" and logic levels greater than 1.25 volts are considered logic "1". However, this is approximate and actual logic levels should be checked against the values given in table 7-1.

7-15. SIGNAL INDEX.

7-16. The signal index is a listing of all signals within the computer with references to the backplane wiring list and to circuit diagrams showing the signal source. This table is arranged in three columns. The first column lists the signal mnemonic for each signal in numeric-alphabetic sequence. In the second column, each signal is assigned a unique reference number that is used to locate and identify the signal on the backplane wiring list (table 7-3). Diagram references are provided in the third column. Number references such as 7-38 refer to schematic diagrams contained in this manual. Other diagram references such as EAU, DMA, Memory Protect, Parity Error, and I/O Interface Card refer to signals that are originated by optional equipment and interface cards. For circuit diagrams showing how optional and interface signals are originated, refer to the operation and maintenance manual covering the particular option or interface kit.

7-17. BACKPLANE WIRING LIST.

7-18. The backplane wiring list is a maintenance and troubleshooting aid that lists the source and all destinations for every signal in the computer. This table is arranged in numeric sequence by the signal reference numbers assigned in the signal index (table 7-2). Signal mnemonics are listed next to the signal reference number for each signal. The rest of the table is divided into three groups labeled memory, logic, and input/output. These three groups correspond to the three sections of the computer card cage (see figure 7-2). Each of these groups is further divided into columns with each column representing a printed circuit card electrical receptacle (card slot). Columns in the table are numbered at top and bottom to correspond with the card slot numbers in the computer. The connections for each signal are indicated by connector pin numbers placed in the applicable columns. Signal source connections are indicated by shaded squares.

7-19. Each signal can be traced to all connections on the backplane by starting with the signal mnemonic, signal reference number, or any backplane connector pin number. If the signal mnemonic is known, find the applicable signal reference number next to the signal mnemonic that is listed in numeric-alphabetic sequence in the signal index (table 7-2). Once the signal reference number is known, go directly to the backplane wiring list (table 7-3) and find the reference number listed in numeric sequence in either the extreme left or extreme right column. All connections for the signal are found on the same line as the reference number by tracing the line horizontally across the page. Connections are identified by pin numbers placed in the applicable squares and the connector is identified by the slot number at the top and bottom of each column. The signal source connection is identified by a shaded box.

7-20. If only a backplane connector and pin number is known, first find the slot number (connector) column on the backplane wire list. Trace vertically down the column on each page of the backplane wire list until the pin number is found. All pin connections for the signal are located on the same horizontal line along with the signal mnemonic and signal reference number. To locate a diagram that shows how the signal is originated, refer to the signal index (table 7-2).

7-21. SIGNAL LISTS.

7-22. Signal lists accompany the schematic diagram for each circuit card. The signal lists show all connections to and from each circuit card in the card cage. Also furnished in the signal lists are logic equations, and definitions of the abbreviations (mnemonics) used for signal names. The various columns in these tables contain the following information:

a. The "SIGNAL OR FLIP-FLOP" column lists, in numeric-alphabetic sequence, all signals entering or leaving the card and all flip-flops situated on the card. Power voltages and ground connections are included. Additionally, this column defines the abbreviation used for each signal or flip-flop. If a circuit card is optional, flip-flops are not included in the signal list.

b. The "SIGNAL SOURCE" column identifies the point of origin of each signal, power voltage, or ground connection. First the reference designation of the origin is given; this is followed by the origin pin number, if any. An asterisk indicates a pin in the 48-pin connector. In many instances there are two or more points of origin for a signal, functioning at different times. When this is the case, all origins are listed. If the signal originates on the card to which the entire signal list pertains, the reference designation of the card itself, together with the appropriate pin number, are listed. For a flip-flop, no entry is made in the "SIGNAL SOURCE" column.

c. The "SIGNAL DESTINATION" column gives the destination of each signal entering or leaving the circuit card to which the signal list pertains. If the signal enters the card, the reference designation of the card is given, followed by the appropriate pin number. If the signal is also furnished to other cards, these are not included. (The signal list for the source card lists all destinations of the signal.) In some cases the "SIGNAL SOURCE" and "SIGNAL DESTINATION" columns specify the same card and pin. This indicates that the signal is produced by the card under certain conditions, and is received by the card under other conditions. For a flip-flop, no entry is made in the "SIGNAL DESTINATION" column.

d. The "LOGIC EQUATION" column gives the Boolean equation for signals that originate on the card. If the signal is furnished by another card, this column specifies "See source" or "See option". If the statement is "See source", the signal list for the source card will furnish the Boolean equation. "See option" indicates that the source is an optional circuit card, which may not be installed in the computer. If the card is installed, reference should be made to the operating and service manual for the optional card. There, either the Boolean equation will be found or the equation can be determined from the logic diagram for the card. Also included in the "LOGIC EQUATION" column are the Boolean equations for signals that set or clear flip-flops situated on the card. (Flip-flops are not listed for optional cards.) No logic equations are given for power voltages or ground connections.

7-23. REFERENCE DESIGNATION INDEXES.

7-24. The third group of tables in this section are the reference designation indexes. One of these is furnished for each electronic assembly, including each circuit card. In each table the electronic components in the applicable assembly are listed alpha-numerically, using the reference designations employed in the schematic diagram for the assembly. With the exception of semiconductor devices, the principal electrical characteristics of each component also are given. In addition, the manufacturer of each component is specified by means of a code number, and the manufacturer's part number is listed. Table 6-21 gives the names and

addresses of the companies designated by the manufacturer code numbers.

7-25. A reference designation index is not supplied for sense amplifier card (part number 02116-63207). Because this card must not be repaired in the field, a list of parts is not required.

7-26. Mechanical parts and assemblies are not listed in the reference designation indexes. For information on these, refer to section VI.

7-27. ARRANGEMENT OF FIGURES AND TABLES.

7-28. CARD CAGE.

7-29. Signals, backplane wiring, components and assemblies used in the card cage are covered by figures 7-1 through 7-21 and tables 7-1 through 7-56.

7-30. The figures and tables for circuit cards are arranged in sequence by card reference designation. In the case of duplicate cards, the figures and tables for the cards are located under the lowest reference designation. To find a schematic for a given circuit card, scan the list of illustrations in the front of this volume to find the desired reference designation number and then turn to the listed page number.

7-31. A signal list is presented for each circuit card, including optional cards. In the case of duplicate cards, a signal list is provided for each card.

7-32. The signal list or lists for each card are followed by the reference designation index for the card. Then the parts location and schematic diagram for the card is provided. Reference designation indexes and schematic diagrams are not furnished for optional cards; only signal lists are provided. (The operating and service manual for each optional device provides the reference designation indexes and schematic diagrams for the optional cards.)

7-33. POWER SUPPLY.

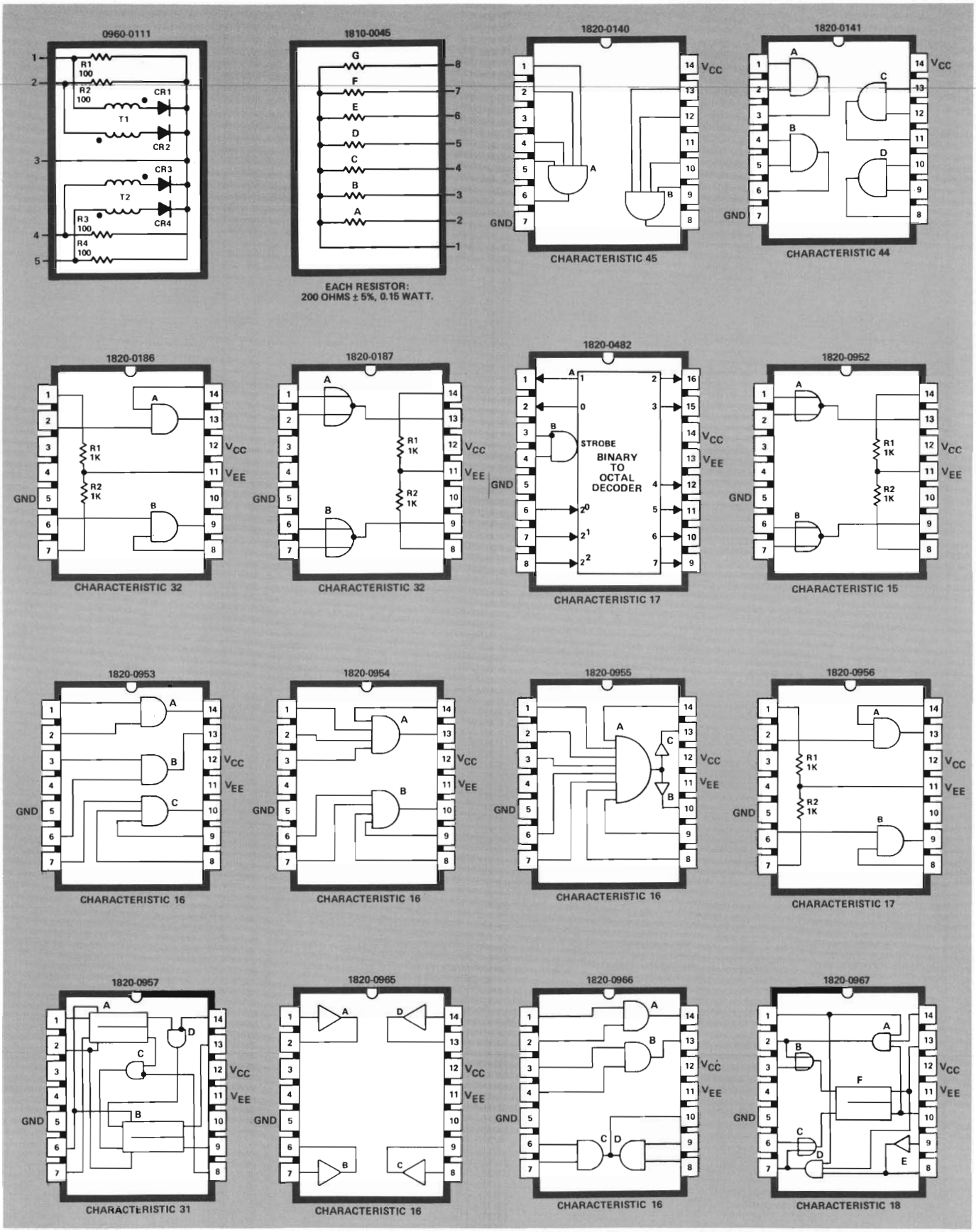
7-34. The power supply is covered in figures 7-22 through 7-34 and tables 7-57 through 7-69, following the card cage material. First, a reference designation index is provided, listing the electronic assemblies which comprise the power supply. Then, for each assembly, a parts location and connection diagram is presented, together with a reference designation index for the assembly. The assembly figures and tables are arranged in sequence by reference designation. Finally, the power supply schematic diagram is presented.

7-35. DOOR ASSEMBLY.

7-36. The door assembly is covered by tables 7-70 and 7-71, and by figures 7-35 through 7-37. The two tables and the first two figures are reference designation indexes and parts location diagrams for the two electronic assemblies installed on the door. Figure 7-37 is the schematic diagram for these two assemblies.

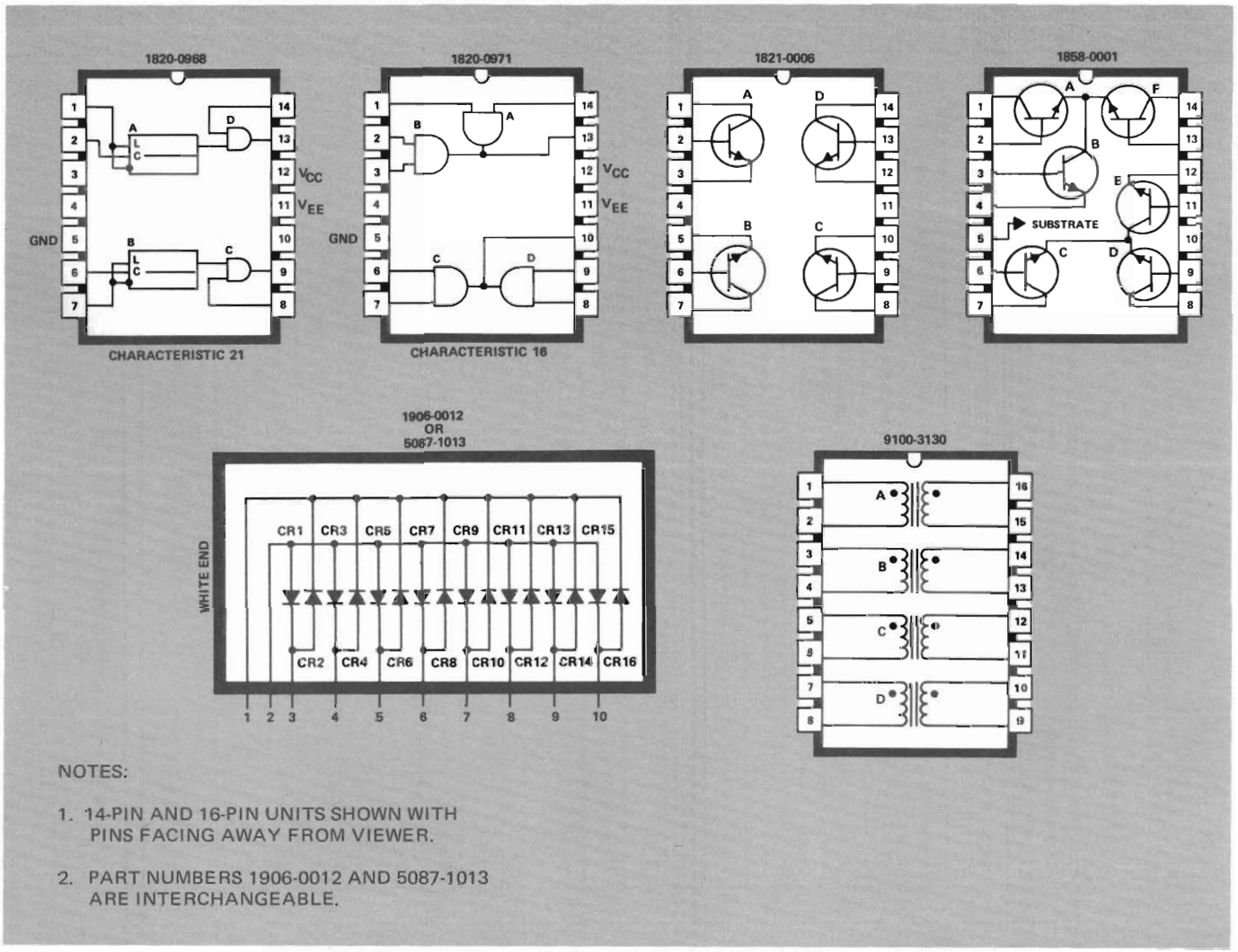
7-39. OVERALL INTERCONNECTION DIAGRAM.

7-40. An overall interconnection diagram is provided on a foldout page at the back of this section so that it may be extended and referenced while reviewing any other part of this section. The diagram shows connections between the power supply, card cage, and door assembly. For connections within these major units, refer respectively to figure 7-34, the signal lists, and figure 7-37.



2107-72A (1 of 2)

Figure 7-1. Microcircuit and Integrated Circuit Diagrams (Sheet 1 of 2)



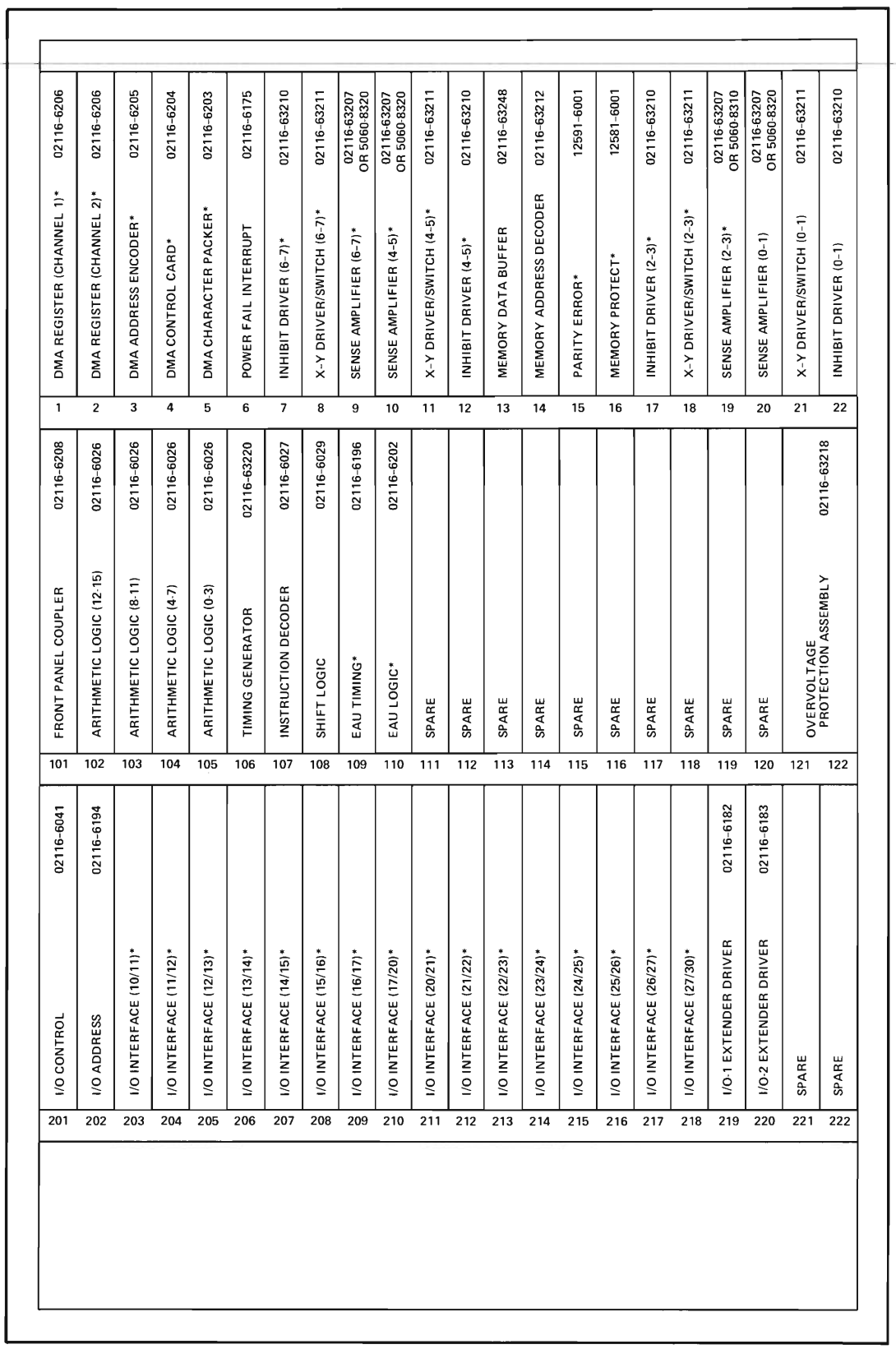
2107-72B (2 OF 2)

Figure 7-1. Microcircuit and Integrated Circuit Diagram (Sheet 2 of 2)

Table 7-1. Integrated Circuit Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	PROPAGATION DELAY (MAX)	
	LOGIC 1 (Volts, Min)	LOGIC 0 (Volts, Max)	LOGIC 1 (Volts, Min)	LOGIC 0 (Volts, Max)		TO LOGIC 1 (Nanosecond)	TO LOGIC 2 (Nanosecond)
15	1.25	0.5	2.35	-0.36	Logic 0	14	12
16	1.8	0.0	1.5	0.22	Logic 0	4.5	4
17	1.25	0.5	2.25	-0.36	Logic 0	18	18
18	1.33*	0.5	2.35	-0.36	Logic 0	15*	25*
	1.25**	0.5	2.35	-0.36	Logic 0	25**	38**
	1.25†	0.8†	— —	— —	Logic 0	— —	— —
21	1.8	0.0	2.0	-0.16	Logic 0	25	4
31	1.25	0.5	2.5	-0.36	Logic 0	15	30
32	1.25	0.5	2.35	-0.36	Logic 0	8	8
44	1.8	1.1	2.5	0.4	Logic 1	15	15
45	2.0	1.1	††	0.5	Logic 1	50	35

Notes:
*J and K inputs
**Set and clear inputs
†Clock input
††Depends on load

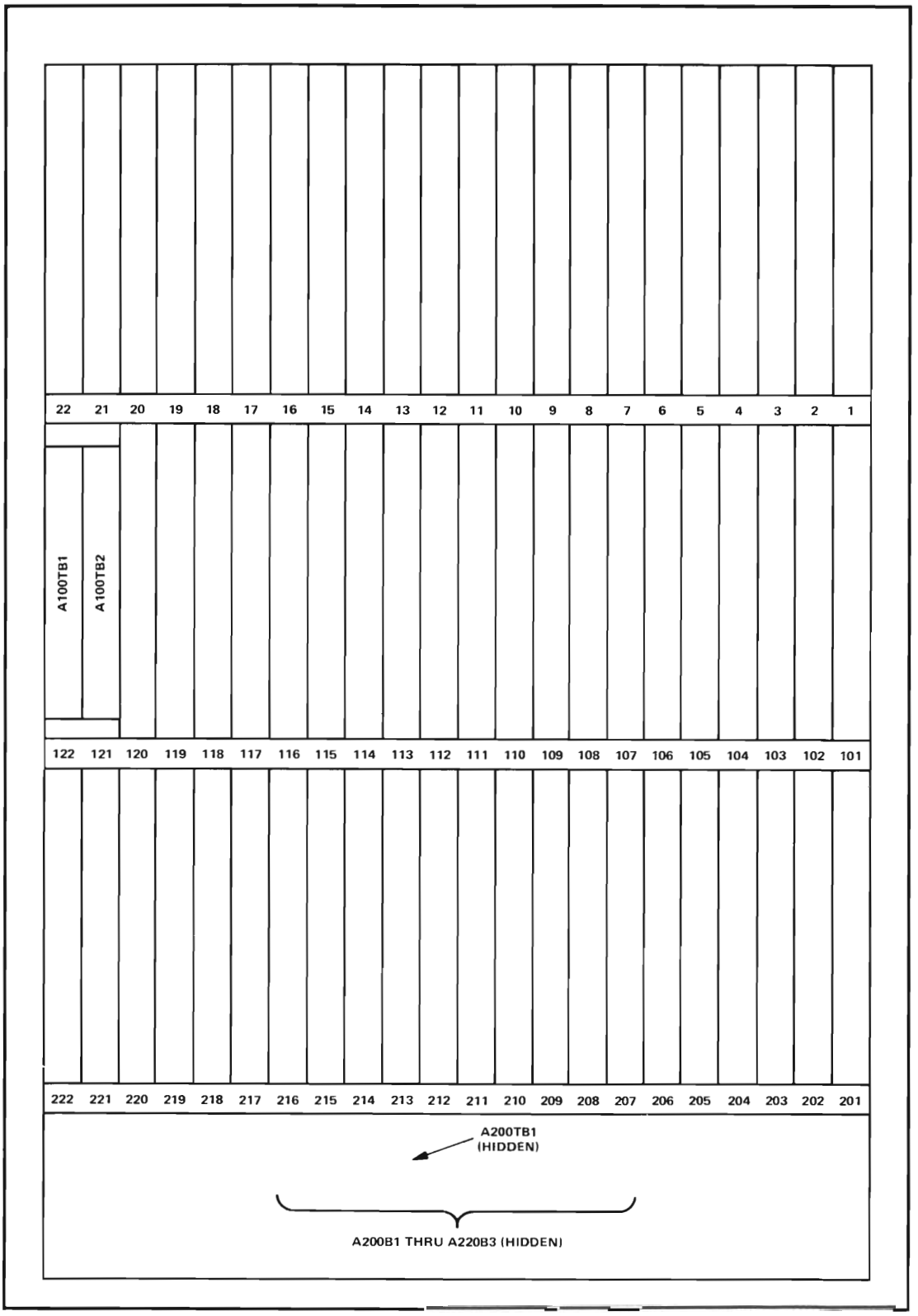


NOTES:

* OPTIONAL CARDS. MAY BE ADDED AT ANY TIME IF CURRENT REQUIREMENTS DO NOT EXCEED POWER SUPPLY RATINGS.

2107-19B

Figure 7-2. Card Cage Assembly, Front View



NOTE:

BACKPLANE CONNECTORS 11 THRU 20 AND 221 AND 222 ARE REPLACED BY FILLER-PLATES ON SOME MODELS.

2107-20A

Figure 7-3. Card Cage Assembly, Rear View

Table 7-2. Signal Index

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
-2V	1	7-38
+4.5V	2	7-38
-5.6V	395	7-38
+7V	3	7-38
+12V	4	7-38
-12V	5	7-38
18.3 VAC	12	7-38
18.3 VAC	13	7-38
+20V	6	7-38
-20V	7	7-38
+30V	40	7-38
+32V	8	7-38
AAF	51	7-15
ADD	66	7-14
ADF	78	7-14
ANF	91	7-14
AS	425	EAU
ASG	82	7-14
BAF	63	7-14
C0	50	7-15
C4	151	7-12
C8	173	7-12
C12	194	7-12
C16	213	7-12
CIN	457	DMA
CLC	49	7-15
CLF	45	7-15
CM1	447	DMA
$\overline{\text{CM2}}$	456	DMA
$\overline{\text{CMF}}$	39	7-10
$\overline{\text{CMFB}}$	436	EAU
$\overline{\text{CMFE}}$	76	7-14
COUT	445	DMA
CPA	87	7-14
CR1	461	DMA
CR2	449	DMA
CRS	277	7-19
D1	414	
thru	thru	EAU
D6	419	
D5L8	400	EAU
DE1	488	DMA
DE2	489	DMA
DIN1	450	DMA
DIN2	459	DMA

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
DL3	430	EAU
DL4	431	EAU
DMS	391	7-11
DS3	397	EAU
DS4	398	EAU
DS34	399	EAU
EDT	374	DMA
EIR	125	7-13
ENF	283	7-19
$\overline{\text{EOF}}$	38	7-10
$\overline{\text{EOFB}}$	435	EAU
EOFE	77	7-14
EPF	16	7-5
EPH	33	7-10
EPO	15	7-5
ESR	287	7-19
EXIT	428	EAU
EXTEND IND.	47	7-15
FLG0	278	
thru	thru	7-20
FLG3	281	
GATE	429	EAU
GND	9	7-38
GND	10	7-38
GND	665	7-7A or 7-8
HIN	55	7-15
HIS	373	DMA
HLS	386	7-11
$\overline{\text{HLS}}$	385	7-11
IAK	273	7-19
ID0M0	507	
thru	thru	7-6
ID16M7	642	
IDW1	484	DMA
IDW2	485	DMA
IEN6	275	7-19
IEN10	276	7-19
IEN20	274	7-19
IHC1	486	DMA
IHC2	487	DMA
IIR	437	EAU
ILS	378	7-11
IN	453	DMA

Table 7-2. Signal Index (Continued)

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
INT	284	7-20
IOBI 0	339	
thru	thru	7-12
IOBI 16	355	
IOBO 0	156	7-12
IOBO 1	152	7-12
IOBO 2	144	7-12
IOBO 3	141	7-12
IOBO 4	177	7-12
IOBO 5	174	7-12
IOBO 6	166	7-12
IOBO 7	163	7-12
IOBO 8	199	7-12
IOBO 9	195	7-12
IOBO 10	187	7-12
IOBO 11	184	7-12
IOBO 12	218	7-12
IOBO 13	214	7-12
IOBO 14	207	7-12
IOBO 15	204	7-12
IOBO 16	372	7-21
IOCO	58	7-15
IODO	444	DMA
IOF	99	7-14
IOGE(B)	270	7-19
IOGE	375	7-5
IOI	46	7-15
IOO	43	7-15
IOS	285	7-19
IR15	89	7-14
IRQ1	304	
thru	thru	7-20
IRQ17	318	
ISG	403	EAU
ISR	64	7-15
ISZ	97	7-14
JMP	79	7-14
JSB	94	7-14
LAMP GND	11	7-38
LAS	388	7-11
LADS	390	7-11
LBS	389	7-11
LMS	387	7-11
LPS	393	7-11
M0	19	
thru	thru	7-10
M13	32	

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
M14	506	7-10
MAC	67	7-14
MD2	402	EAU
MIT	663	7-13
MITX	643	7-9
MMD13	439	7-7
MMD14	440	7-7
MNS	377	7-11
MOD0	246	7-10
MOD1	247	7-10
MOD2	248	7-10
MOD3	249	7-10
MOD4	490	7-10
MOD5	493	7-10
MOD6	494	7-10
MOD7	495	7-10
MOD0/1	250	7-10
MOD2/3	251	7-10
MOD4/5	502	7-10
MOD6/7	505	7-10
MP1	409	EAU
MP2	410	EAU
MP3	411	EAU
MP4	412	EAU
MP5	413	EAU
MPC	438	7-5
MPT	252	7-10
MPT1	496	7-7
MPT2	497	7-7
MPT3	498	7-7
MPT4	499	7-7
MR0	158	7-12
MR0	145	7-12
MR1	149	7-12
MR1	139	7-12
MR2	146	7-12
MR2	157	7-12
MR3	140	7-12
MR3	150	7-12
MR4	179	7-12
MR4	167	7-12
MR5	171	7-12
MR5	161	7-12
MR6	168	7-12
MR6	178	7-12

Table 7-2. Signal Index (Continued)

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
MR7	162	7-12
$\overline{\text{MR7}}$	172	7-12
MR8	201	7-12
$\overline{\text{MR8}}$	188	7-12
MR9	192	7-12
$\overline{\text{MR9}}$	182	7-12
MR10	189	7-12
$\overline{\text{MR10}}$	200	7-12
MR11	183	7-12
$\overline{\text{MR11}}$	193	7-12
MR12	219	7-12
$\overline{\text{MR12}}$	208	7-12
MR13	212	7-12
MR14	209	7-12
MRT1	242	7-13
MRT2	107	7-13
MSG	662	7-13
MST	124	7-13
MWL	136	7-13
MWT1	105	7-13
MWT2	664	7-13
OASL	406	EAU
OHC1	480	DMA
OHC2	481	DMA
OLC1	482	DMA
OLC2	483	DMA
$\overline{\text{OPO}}$	84	7-14
OUT	446	DMA
OVD	404	EAU
OVERFLOW IND.	42	7-15
OVR	422	EAU
$\overline{\text{OVR}}$	423	EAU
P123	104	7-13
P123G	34	7-10
PEH	239	7-13
PEI	241	7-13
PH1	111	7-13
PH2	110	7-13
PH3	128	7-13
PH4	101	7-13
PH5	443	DMA
$\overline{\text{PH5}}$	442	DMA
$\overline{\text{PH5}}$	286	7-19
PIND	394	7-5
PNS	376	7-11

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
POFP	380	7-5
PON	379	7-11
POPIO	115	7-13
POPIO(B)	338	7-19
PRESET LAMP	14	7-5
PRH5/PRL4	336	7-19
PRH6/PRL5	337	7-19
PRH10/PRL7 thru PRH30/PRL27	319 thru 335	I/O Interface Card
PRL6	503	7-19
PRS	381	7-11
$\overline{\text{PRSW}}$	382	7-11
PSO	17	7-5
RARB	70	7-14
RB0	74	7-14
RB14	222	7-12
RB15	221	7-12
RBRB	85	7-14
$\overline{\text{RF2}}$	127	7-13
$\overline{\text{RL4}}$	56	7-15
$\overline{\text{RLL}}$	60	7-15
RMSB	95	7-14
RNSW	384	7-11
$\overline{\text{RNSW}}$	383	7-11
RO	424	EAU
ROT5	405	EAU
RPB	106	7-13
RPRB	96	7-14
$\overline{\text{RRS}}$	48	7-15
RSDS	407	MEMORY PROTECT
RSET	396	EAU
RSM6-9	83	7-14
RSM10-15	69	7-14
RST	92	7-14
RT	426	EAU
$\overline{\text{RT}}$	427	EAU
RTSB	98	7-14
RUN	500	7-20
SA0 thru SA15	254 thru 269	7-7A or 7-8
SA16	492	7-7A or 7-8
SB0	80	7-14

Table 7-2. Signal Index (Continued)

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
SB15	220	7-12
SCL0	288	
thru	thru	7-20
SCL7	295	
SCM0	296	
thru	thru	7-20
SCM7	303	
SCS	392	7-11
SEO	131	7-13
SFC	54	7-15
SFS	61	7-15
SIR	272	7-19
SKF	282	7-19
SL14	36	7-10
SL14B	434	EAU
SL14E	59	7-15
SLM	35	7-10
SLMB	432	EAU
SLME	53	7-15
SMAR1	458	DMA
SMAR2	448	DMA
SPARE	501	I/O Interface Card
SRCS	401	EAU
SRE	240	PARITY ERROR
SRG	88	7-14
SRM	37	7-10
SRMB	433	EAU
SRME	57	7-15
SRQ10	356	I/O
thru	thru	Interface
SRQ27	371	Card
ST0	644	
thru	thru	7-9
ST16	660	
STBA	90	7-14
STBB	73	7-14
STBT	75	7-14
STC	62	7-15
STF	41	7-15
STM0-5	86	7-14
STM6-9	71	7-14
STM10-11	72	7-14
STM12-15	109	7-14
STP0-9	68	7-14
STP10-11	65	7-14
STP12-15	81	7-14
STR	93	7-14
STRX	661	7-9
SWCR1	462	DMA
SWCR2	452	DMA
SWSA	133	7-13
SWSB	118	7-13
SWSM	119	7-13
SWSP	130	7-13
SWST	129	7-13
SWT1 (NC)*	245	7-10
SWT2 (NC)*	441	7-10
T0	122	7-13
T0T1	134	7-13
T1	113	7-13
T1T2	103	7-13
T2	132	7-13
T2T3 (B)	408	EAU
T3	116	7-13
T3(B)	271	7-19
T3T4	102	7-13
T4	126	7-13
T4T5	120	7-13
T5	117	7-13
T6	135	7-13
T6T7	123	7-13
T7	121	7-13
T7S	112	7-13
TAN1	142	7-12
TAN2	164	7-12
TAN3	185	7-12
TAN4	205	7-12
TB0	223	
thru	thru	7-12
TB15	238	
TE1	454	DMA
TE2	463	DMA
TEV	421	EAU
THERM SWITCH	18	7-34
TOD	420	EAU
TR0	155	7-12
TR0(B)	52	7-15
TR0(B)	464	
thru	thru	DMA
TR15(B)	479	

*These signals are not connected through the backplane.

Table 7-2. Signal Index (Continued)

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
$\overline{\text{TR0}}$	153	7-12
TR1	137	7-12
$\overline{\text{TR1}}$	147	7-12
TR2	154	7-12
TR2(B)	44	7-15
$\overline{\text{TR2}}$	143	7-12
TR3	148	7-12
$\overline{\text{TR3}}$	138	7-12
TR4	176	7-12
$\overline{\text{TR4}}$	175	7-12
TR5	159	7-12
$\overline{\text{TR5}}$	169	7-12
TR6	108	7-12
$\overline{\text{TR6}}$	165	7-12
TR7	170	7-12
$\overline{\text{TR7}}$	160	7-12
TR8	198	7-12
$\overline{\text{TR8}}$	196	7-12
TR9	180	7-12
$\overline{\text{TR9}}$	190	7-12

SIGNAL MNEMONIC	SIGNAL REF NO.	DIAGRAM REFERENCE
TR10	197	7-12
$\overline{\text{TR10}}$	186	7-12
TR11	191	7-12
$\overline{\text{TR11}}$	181	7-12
TR12	217	7-12
$\overline{\text{TR12}}$	215	7-12
TR13	202	7-12
$\overline{\text{TR13}}$	210	7-12
TR14	216	7-12
$\overline{\text{TR14}}$	206	7-12
TR15	211	7-12
$\overline{\text{TR15}}$	203	7-12
$\overline{\text{TR16}}$	491	PARITY ERROR
TS	114	7-13
TSA	504	7-13
WCR1	451	DMA
WCR2	460	DMA
XT1	243	7-10
XT2	244	7-10

Table 7-3. Backplane Wiring List

MEMORY

REF.	SIGNAL	22 INHIBIT DRIVER 0-1	21 X-Y DRIVER/ SWITCH 0-1	20 SENSE AMPLIFIER 0-1	19 SENSE AMPLIFIER 2-3	18 X-Y DRIVER/ SWITCH 2-3	17 INHIBIT DRIVER 2-3	16 MEMORY PROTECT	15 PARITY ERROR	14 MEMORY ADDRESS DECODER	13 MEMORY DATA BUFFER	12 INHIBIT DRIVER 4-5	11 X-Y DRIVER/ SWITCH 4-5	10 SENSE AMPLIFIER 4-5	9 SENSE AMPLIFIER 6-7	8 X-Y DRIVER/ SWITCH 6-7	7 INHIBIT DRIVER 6-7	6 POWER FAIL	5 DMA PACKER	4 DMA CONTROL	3 DMA ENCODER	2 DMA REGISTER 1	1 DMA REGISTER 2
1	-2V	47, 48	←									BUS										→	47, 48
2	+4.5V	39, 40	←									BUS										→	39, 40
3	+7V																						
4	+12V			13, 14	13, 14									13, 14	13, 14			43, 44					
5	-12V			73, 74	73, 74									73, 74	73, 74			69, 70					
6	+20V	15, 16 / 71, 72	9, 10			9, 10	15, 16 / 71, 72					15, 16 / 71, 72	9, 10			9, 10	15, 16 / 71, 72	31					
7	-20V		75, 76			75, 76							75, 76			75, 76		33					
8	+32V																	29					
9	GND	1, 2	←									BUS										→	1, 2
10	GND	85, 86	←									BUS										→	85, 86
11	LAMP GND																						
12	18.3 VAC																	79					
13	18.3 VAC																	80					
14	PRESET LAMP																	**35**					
15	EPO																	37					
16	EPF																	42					
17	PSO																	**51**					
18	THERM SW																	52					
19	M0		35			35				**6**			35			35						41	41
20	M1		36			36				**10**			36			36						46	48
21	M2		37			37				**14**			37			37						45	45
22	M3		33			33				**18**			33			33						55	55
23	M4		32			32				**22**			32			32						65	65
24	M5		31			31				**26**	75		31			31						63	63
25	M6		49			49				**30**	79		49			49						71	71
26	M7		52			52				**34**			52			52						72	72
27	M8		51			51				**38**			51			51						83	83
28	M9		53			53				**44**			53			53						82	82
29	M10		56			56				**50**			56			56						6	6
30	M11		55			55				**54**			55			55						10	10
31	M12									**58**												12	12
32	M13					23				**62**												16	16
33	EPH									**72**													
34	P123G									**65**													
35	SLM									**77**													
36	SL14 (overbar)									**74**													
37	SRM (overbar)									**78**													
38	EOF (overbar)									**75**													
39	CMF (overbar)									**79**													
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
1	-2V													47, 48	←				BUS			→	47, 48
2	+4.5V													39, 40	←				BUS			→	39, 40
3	+7V																						
4	+12V																						
5	-12V																						
6	+20V																						
7	-20V																						
8	+32V																						
9	GND													1, 2	←				BUS			→	1, 2
10	GND													85, 86	←				BUS			→	85, 86
11	LAMP GND																						
12	18.3 VAC																						
13	18.3 VAC																						
14	PRESET LAMP																						
15	EPO																						
16	EPF																						
17	PSO																						
18	THERM SW																						
19	M0																						
20	M1																						
21	M2																						
22	M3																						
23	M4																						
24	M5																						
25	M6																						
26	M7																						
27	M8																						
28	M9																						
29	M10																						
30	M11																						
31	M12																						
32	M13																						
33	EPH																	14					
34	P123G															69							
35	SLM (overbar)																		41, 82 / 80	41, 82 / 80	41, 82 / 80	80	
36	SL14 (overbar)																					82	
37	SRM (overbar)																		74	83 / 74	83 / 74	83 / 74	
38	EOF (overbar)																		76	←	→	76	
39	CMF (overbar)																		64	←	→	64	
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

REF.	SIGNAL	222	221	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 (27)	217 (26)	216 (25)	215 (24)	214 (23)	213 (22)	212 (21)	211 (20)	210 (17)	209 (16)	208 (15)	207 (14)	206 (13)	205 (12)	204 (11)	203 (10)	202 I/O ADDRESS ENCODER	201 I/O CONTROL	REF.
1	-2V			47, 48	←								BUS									→	47, 48	1
2	+4.5V			39, 40	←								BUS									→	39, 40	2
3	+7V																							3
4	+12V			43, 44	←								BUS									→	43, 44	4
5	-12V			69, 70	←								BUS									→	69, 70	5
6	+20V																							6
7	-20V																							7
8	+32V																							8
9	GND			1, 2	←								BUS									→	1, 2	9
10	GND			85, 86	←								BUS									→	85, 86	10
11	LAMP GND																							11
12	18.3 VAC																							12
13	18.3 VAC																							13
14	PRESET LAMP																							14
15	EPO																							15
16	EPF																							16
17	PSO																							17
18	THERM SW																							18
19	M0																							19
20	M1																							20
21	M2																							21
22	M3																							22
23	M4																							23
24	M5																							24
25	M6																							25
26	M7																							26
27	M8																							27
28	M9																							28
29	M10																							29
30	M11																							30
31	M12																							31
32	M13																							32
33	EPH																							33
34	P123G																							34
35	SLM (overbar)																							35
36	SL14 (overbar)																							36
37	SRM (overbar)																							37
38	EOF (overbar)																							38
39	CMF (overbar)																							39
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL (shaded pin numbers shown in bold above)

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	22 INHIBIT DRIVER 0-1	21 X-Y DRIVER/ SWITCH 0-1	20 SENSE AMPLIFIER 0-1	19 SENSE AMPLIFIER 2-3	18 X-Y DRIVER/ SWITCH 2-3	17 INHIBIT DRIVER 2-3	16 MEMORY PROTECT	15 PARITY ERROR	14 MEMORY ADDRESS DECODER	13 MEMORY DATA BUFFER	12 INHIBIT DRIVER 4-5	11 X-Y DRIVER/ SWITCH 4-5	10 SENSE AMPLIFIER 4-5	9 SENSE AMPLIFIER 6-7	8 X-Y DRIVER/ SWITCH 6-7	7 INHIBIT DRIVER 6-7	6 POWER FAIL	5 DMA PACKER	4 DMA CONTROL	3 DMA ENCODER	2 DMA REGISTER 1	1 DMA REGISTER 2
40	+30V																						
41	STF								18											16			
42	OVERFLOW IND																						
43	IOO							57												56	30	8	8
44	TR2B																						
45	CLF								51									7		14			51
46	IOI							59	15											$^{84}_{81}$	$^{43}_{11}$	22	22
47	EXTEND IND																						
48	$\overline{\text{RRS}}$																						
49	CLC																	21		60		18	18
50	CO																						43
51	AAF							17	49														
52	TR0B																						
53	$\overline{\text{SLME}}$									70													
54	SFC																	5		24			
55	HIN							55	69														
56	$\overline{\text{RL4}}$																						
57	$\overline{\text{SRME}}$									76													
58	IOCO																						
59	$\overline{\text{SL14E}}$									67													
60	$\overline{\text{RLL}}$																						
61	SFS																			20			31
62	STC							41										22		58	17	20	20
63	BAF							13	50														
64	ISR																						
65	STP10-11																						
66	ADD																						
67	MAC																						
68	STP0-9																						
69	RSM10-15																						
70	RARB																						
71	STM6-9																						
72	STM10-11																						
73	STBB																						
74	RB0																						
75	STBT																						
76	$\overline{\text{CMFE}}$									81													
77	$\overline{\text{EOFE}}$									83													
78	ADF																			82			
79	JMP							11															

LOGIC

REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
40	+30V																						
41	STF														15	5							
42	OVERFLOW IND															9							4
43	IOO															13							
44	TR2B															15							
45	CLF														24	19							
46	IOI															44			31	←	→	31	
47	EXTEND IND															37							83
48	$\overline{\text{RRS}}$															41			83				
49	CLC															53							
50	CO															71			67				
51	AAF															77	49	75					
52	TR0B															4							
53	$\overline{\text{SLME}}$															8							
54	SFC															14							
55	HIN															26		66					
56	$\overline{\text{RL4}}$															28			78	←	→	78	
57	$\overline{\text{SRME}}$															32							
58	IOCO															34			70	←	→	70	
59	$\overline{\text{SL14E}}$															38							
60	$\overline{\text{RLL}}$															42						41	
61	SFS															54							
62	STC															56							
63	BAF															80	13	83					
64	ISR															84							6
65	STP10-11																74				44		
66	ADD															29	3						
67	MAC														62		5						
68	STP0-9																7		$^{23}_{44}$	$^{23}_{44}$	23		
69	RSM10-15																11				21	$^{14}_{21}$	
70	RARB													65			19		34	←	→	34	
71	STM6-9																21			22	29		
72	STM10-11																27				22		
73	STBB																51		26	←	→	26	
74	RB0													43		52	61		37				
75	STBT																63		51	←	→	51	
76	$\overline{\text{CMFE}}$																65						
77	$\overline{\text{EOFE}}$																67						
78	ADF													12			75		5	←	→	5	
79	JMP																79	34					

INPUT/OUTPUT

REF.	SIGNAL	222	221	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 27	217 26	216 25	215 24	214 23	213 22	212 21	211 20	210 17	209 16	208 15	207 14	206 13	205 12	204 11	203 10	202 I/O ADDRESS ENCODER	201 I/O CONTROL	REF.
40	+30V			36	←							BUS								→	36			40
41	STF			9	←							BUS								→	9		41	41
42	OVERFLOW IND																							42
43	IOO			20	←							BUS								→	20			43
44	TR2B																					53		44
45	CLF			7	←							BUS								→	7		51	45
46	IOI			24	←							BUS									→	24		46
47	EXTEND IND																							47
48	$\overline{\text{RRS}}$																							48
49	CLC			21	←							BUS								→	21		75	49
50	CO																							50
51	AAF																							51
52	TR0B																					83		52
53	$\overline{\text{SLME}}$																							53
54	SFC			5	←							BUS								→	5		71	54
55	HIN																							55
56	$\overline{\text{RL4}}$																							56
57	$\overline{\text{SRME}}$																							57
58	IOCO																							58
59	$\overline{\text{SL14E}}$																							59
60	$\overline{\text{RLL}}$																							60
61	SFS			25	←							BUS								→	25		68	61
62	STC				22	←						BUS								→	22		61	62
63	BAF																							63
64	ISR																							64
65	STP10-11																							65
66	ADD																							66
67	MAC																							67
68	STP0-9																							68
69	RSM10-15																							69
70	RARB																							70
71	STM6-9																							71
72	STM10-11																							72
73	STBB																							73
74	RB0																							74
75	STBT																							75
76	$\overline{\text{CMFE}}$																							76
77	$\overline{\text{EOFE}}$																							77
78	ADF																							78
79	JMP																							79

NOTES:
SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1 22	X-Y DRIVER/ SWITCH 0-1 21	SENSE AMPLIFIER 0-1 20	SENSE AMPLIFIER 2-3 19	X-Y DRIVER/ SWITCH 2-3 18	INHIBIT DRIVER 2-3 17	MEMORY PROTECT 16	PARITY ERROR 15	MEMORY ADDRESS DECODER 14	MEMORY DATA BUFFER 13	INHIBIT DRIVER 4-5 12	X-Y DRIVER/ SWITCH 4-5 11	SENSE AMPLIFIER 4-5 10	SENSE AMPLIFIER 6-7 9	X-Y DRIVER/ SWITCH 6-7 8	INHIBIT DRIVER 6-7 7	POWER FAIL 6	DMA PACKER 5	DMA CONTROL 4	DMA ENCODER 3	DMA REGISTER 1 2	DMA REGISTER 2 1
80	SB0																						
81	STP12-15																						
82	ASG																						
83	RSM6-9																						
84	$\overline{OPO}$																						
85	RBRB																						
86	STM0-5																						
87	CPA																						
88	SRG																						
89	$\overline{IR15}$							33										4					
90	STBA																						
91	ANF																						
92	RST																						
93	STR										46												
94	JSB																						
95	RMSB																						
96	RPRB																						
97	ISZ								44														69
98	RTSB																						60
99	$\overline{IOF}$																						
100	IOGS							16	59									38					
101	PH4										82												
102	T3T4																			30			
103	T1T2																						
104	P123							63	52	68													
105	MWT1		$^{50}_{58}$			$^{50}_{58}$							$^{50}_{58}$			$^{50}_{58}$							
106	RPB								46														
107	MRT2									33													
108	TR6								58										15				
109	STM12-15																						
110	PH2							49			78												
111	PH1							21			76												
112	T7S																			10			
113	T1							24															
114	TS																						
115	POPIO								45														37
116	T3							23	23														
117	T5																						
118	SWSB																						
119	SWSM																						
120	T4T5																			6	31		
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	EAU LOGIC 110	EAU TIMING 109	SHIFT LOGIC 108	INSTRUCTION DECODER 107	TIMING GENERATOR 106	ARITHMETIC LOGIC 0-3 105	ARITHMETIC LOGIC 4-7 104	ARITHMETIC LOGIC 8-11 103	ARITHMETIC LOGIC 12-15 102	FRONT PANEL COUPLER 101
80	SB0													44			**81**		42				
81	STP12-15																**8**					$^{23}_{44}$	
82	ASG															82	**10**						
83	RSM6-9																**12**			21	14		
84	$\overline{OPO}$																**16**	42					
85	RBRB													58			**18**		28	←	→	28	
86	STM0-5																**20**		$^{22}_{29}$	29			
87	CPA															63	**22**						
88	SRG															49	**38**						
89	$\overline{IR15}$																**42**	49					
90	STBA																**50**		38	←	→	38	
91	ANF																**56**		72	←	→	72	
92	RST																**58**		7	←	→	7	
93	STR																**64**						
94	JSB																**66**	82					
95	RMSB													34			**68**		8	←	→	8	
96	RPRB													4			**72**		12	←	→	12	
97	ISZ															61	**76**	24					
98	RTSB													19			**82**		20	←	→	20	
99	$\overline{IOF}$																**84**		73	←	→	73	
100	IOGS																**6**						
101	PH4																83	**13**					
102	T3T4													74		7	70	**15**					
103	T1T2													51			52	**21**					
104	P123														13		78	**23**					
105	MWT1																	**35**					
106	RPB																	**27**					
107	MRT2																	**26**					
108	TR6														66	3				**56**			
109	STM12-15																**28**					$^{22}_{29}$	
110	PH2																53	**37**					
111	PH1														81		44	**41**					
112	T7S														23			**51**					
113	T1													13	71		62	**53**					
114	TS															74	45	**55**					
115	POPIO																	**61**					
116	T3													32	75	45	43	**63**					
117	T5													54	67	46	36	**69**					
118	SWSB													10			24	**71**					
119	SWSM													33			26	**73**					
120	T4T5													23		21	54	**16**					
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

REF.	SIGNAL	222	221	I/O EXTENDER X2 220	I/O EXTENDER X1 219	27 218	26 217	25 216	24 215	23 214	22 213	21 212	20 211	17 210	16 209	15 208	14 207	13 206	12 205	11 204	10 203	I/O ADDRESS ENCODER 202	I/O CONTROL 201	REF.
80	SB0																							80
81	STP12-15																							81
82	ASG																							82
83	RSM6-9																					11		83
84	$\overline{OPO}$																							84
85	RBRB																							85
86	STM0-5																							86
87	CPA																							87
88	SRG																							88
89	$\overline{IR15}$																							89
90	STBA																							90
91	ANF																							91
92	RST																							92
93	STR																							93
94	JSB																							94
95	RMSB																							95
96	RPRB																							96
97	ISZ																							97
98	RTSB																							98
99	$\overline{IOF}$																							99
100	IOGS																							100
101	PH4																						53	101
102	T3T4																							102
103	T1T2																							103
104	P123																							104
105	MWT1																							105
106	RPB																							106
107	MRT2																							107
108	TR6																							108
109	STM12-15																						79	109
110	PH2																							110
111	PH1																						29	111
112	T7S																							112
113	T1																						23	113
114	TS																						27	114
115	POPIO																						63	115
116	T3																						3	116
117	T5																						45	117
118	SWSB																							118
119	SWSM																							119
120	T4T5																							120
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:
SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL (shaded pin numbers shown in bold)

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1	X-Y DRIVER/ SWITCH 0-1	SENSE AMPLIFIER 0-1	SENSE AMPLIFIER 2-3	X-Y DRIVER/ SWITCH 2-3	INHIBIT DRIVER 2-3	MEMORY PROTECT	PARITY ERROR	MEMORY ADDRESS DECODER	MEMORY DATA BUFFER	INHIBIT DRIVER 4-5	X-Y DRIVER/ SWITCH 4-5	SENSE AMPLIFIER 4-5	SENSE AMPLIFIER 6-7	X-Y DRIVER/ SWITCH 6-7	INHIBIT DRIVER 6-7	POWER FAIL	DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
121	T7							61	26											64			57
122	T0																						54
123	T6T7																				73		
124	MST										36 83												
125	$\overline{\text{EIR}}$																						
126	T4																						
127	$\overline{\text{RF2}}$																	62					
128	PH3								43		80												67
129	SWST																			83			
130	SWSP																						
131	SEO																						
132	T2																						
133	SWSA																						
134	T0T1																						
135	T6																						
136	MWL							34	54														
137	TR1								83										5				
138	$\overline{\text{TR3}}$	83					83		73			83					83						
139	$\overline{\text{MR1}}$																						
140	MR3							18		16													
141	IOBO3							3											45		35	34	34
142	TAN1																						
143	$\overline{\text{TR2}}$	13					13		74			13					13						
144	IOBO2							4											41		65	32	32
145	$\overline{\text{MR0}}$																						
146	MR2							8		12													
147	$\overline{\text{TR1}}$	11					11		81			11					11						
148	TR3								75										9				
149	MR1							10		8													
150	$\overline{\text{MR3}}$																						
151	C4																						
152	IOBO1							5											38		42	26	26
153	$\overline{\text{TR0}}$	5					5		82			5					5						
154	TR2								76										7				
155	TR0								84										3				
156	IOBO0							6											35		21	24	24
157	$\overline{\text{MR2}}$																						
158	MR0							14		4													
159	TR5								67										13				
160	$\overline{\text{TR7}}$	73					73		55			73					73						

LOGIC

REF.	SIGNAL													EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
121	T7													28	73	83	32	18					
122	T0													15	51	68	46	28					
123	T6T7													11	14	72	69	30					
124	MST																	32					
125	$\overline{\text{EIR}}$																4	52					
126	T4													24	55	65	31	54					
127	$\overline{\text{RF2}}$														54			58					14
128	PH3															62	60	60					
129	SWST													20			34	62					
130	SWSP													3			37	64					
131	SEO															22	77	72					
132	T2													22	43	35	59	76					
133	SWSA													66			35	84					
134	T0T1													36			80	17					
135	T6													30	60			11					
136	MWL																	33					
137	TR1														30				9				
138	$\overline{\text{TR3}}$															10			15				
139	$\overline{\text{MR1}}$																		19				
140	MR3																		25				
141	IOBO3																		35				
142	TAN1															58			43				
143	$\overline{\text{TR2}}$															33			53				
144	IOBO2																		57				
145	$\overline{\text{MR0}}$																		63				
146	MR2																		65				
147	$\overline{\text{TR1}}$															27			10				
148	TR3														32				16				
149	MR1																		18				
150	$\overline{\text{MR3}}$																		24				
151	C4																		36	67			
152	IOBO1																		50				
153	$\overline{\text{TR0}}$															24			54				
154	TR2														38		71		56				
155	TR0														37	12			58				
156	IOBO0																		60				
157	$\overline{\text{MR2}}$																		66				
158	MR0																		68				
159	TR5														69					9			
160	$\overline{\text{TR7}}$															30	23			15			

INPUT/OUTPUT

REF.	SIGNAL			I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL	REF.
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	
121	T7																							121
122	T0																						31	122
123	T6T7																							123
124	MST																							124
125	$\overline{\text{EIR}}$																							125
126	T4																							126
127	$\overline{\text{RF2}}$																					36		127
128	PH3																							128
129	SWST																							129
130	SWSP																							130
131	SEO																							131
132	T2																						83	132
133	SWSA																							133
134	T0T1																							134
135	T6																							135
136	MWL																							136
137	TR1																					84		137
138	$\overline{\text{TR3}}$																					59		138
139	$\overline{\text{MR1}}$																							139
140	MR3																							140
141	IOBO3				55	45	←							BUS						→	45			141
142	TAN1																							142
143	$\overline{\text{TR2}}$																					66		143
144	IOBO2				53	41	←							BUS						→	41			144
145	$\overline{\text{MR0}}$																							145
146	MR2																							146
147	$\overline{\text{TR1}}$																					80		147
148	TR3																					60		148
149	MR1																							149
150	$\overline{\text{MR3}}$																							150
151	C4																							151
152	IOBO1				51	38	←							BUS						→	38			152
153	$\overline{\text{TR0}}$																					82		153
154	TR2																							154
155	TR0																							155
156	IOBO0				49	35	←							BUS						→	35			156
157	$\overline{\text{MR2}}$																							157
158	MR0																							158
159	TR5																					58		159
160	$\overline{\text{TR7}}$																							160

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1 (22)	X-Y DRIVER/SWITCH 0-1 (21)	SENSE AMPLIFIER 0-1 (20)	SENSE AMPLIFIER 2-3 (19)	X-Y DRIVER/SWITCH 2-3 (18)	INHIBIT DRIVER 2-3 (17)	MEMORY PROTECT (16)	PARITY ERROR (15)	MEMORY ADDRESS DECODER (14)	MEMORY DATA BUFFER (13)	INHIBIT DRIVER 4-5 (12)	X-Y DRIVER/SWITCH 4-5 (11)	SENSE AMPLIFIER 4-5 (10)	SENSE AMPLIFIER 6-7 (9)	X-Y DRIVER/SWITCH 6-7 (8)	INHIBIT DRIVER 6-7 (7)	POWER FAIL (6)	DMA PACKER (5)	DMA CONTROL (4)	DMA ENCODER (3)	DMA REGISTER 1 (2)	DMA REGISTER 2 (1)
161	$\overline{MR5}$																						
162	MR7							32		32													
163	IOBO7							20											52			50	50
164	TAN2																						
165	$\overline{TR6}$	79					79		56			79					79						
166	IOBO6							22											53			52	52
167	$\overline{MR4}$																						
168	MR6							37		28													
169	$\overline{TR5}$	77					77		65			77					77						
170	TR7								57										17				
171	MR5							42		24													
172	$\overline{MR7}$																						
173	C8																						
174	IOBO5							28											51		61	42	42
175	$\overline{TR4}$	81					81		66			81					81						
176	TR4								68										11				
177	IOBO4							26											42		63	36	36
178	$\overline{MR6}$																						
179	MR4							30		20													
180	TR9								31										43				
181	$\overline{TR11}$	80					80		19			80					80						
182	$\overline{MR9}$																						
183	MR11							60		52													
184	IOBO11							52											55			64	64
185	TAN3																						
186	$\overline{TR10}$	74					74		20			74					74						
187	IOBO10							50											58			66	66
188	$\overline{MR8}$																						
189	MR10							58		46													
190	$\overline{TR9}$	76					76		29			76					76						
191	TR11								21										50				
192	MR9							68		42													
193	$\overline{MR11}$																						
194	C12																						
195	IOBO9							54											56			62	62
196	$\overline{TR8}$	75					75		30			75					75						
197	TR10								22										46				
198	TR8								32										34				
199	IOBO8							45											54			56	56
200	$\overline{MR10}$																						
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	EAU LOGIC (110)	EAU TIMING (109)	SHIFT LOGIC (108)	INSTRUCTION DECODER (107)	TIMING GENERATOR (106)	ARITHMETIC LOGIC 0-3 (105)	ARITHMETIC LOGIC 4-7 (104)	ARITHMETIC LOGIC 8-11 (103)	ARITHMETIC LOGIC 12-15 (102)	FRONT PANEL COUPLER (101)
161	$\overline{MR5}$																			19			
162	MR7																			25			
163	IOBO7																			35			
164	TAN2															57				43			
165	$\overline{TR6}$															23	55			53			
166	IOBO6																			57			
167	$\overline{MR4}$																			63			
168	MR6																			65			
169	$\overline{TR5}$															6				10			
170	TR7														83	11				16			
171	MR5																			18			
172	$\overline{MR7}$																			24			
173	C8																			36	67		
174	IOBO5																			50			
175	$\overline{TR4}$															79				54			
176	TR4														72		25			58			
177	IOBO4																			60			
178	$\overline{MR6}$																			66			
179	MR4																			68			
180	TR9														61	17					9		
181	$\overline{TR11}$														70	55					15		
182	$\overline{MR9}$																				19		
183	MR11																				25		
184	IOBO11																				35		
185	TAN3															60					43		
186	$\overline{TR10}$																				53		
187	IOBO10																				57		
188	$\overline{MR8}$																				63		
189	MR10																				65		
190	$\overline{TR9}$																57				10		
191	TR11														84	43	14				16		
192	MR9																				18		
193	$\overline{MR11}$																				24		
194	C12																				36	67	
195	IOBO9																				50		
196	$\overline{TR8}$															36					54		
197	TR10																9				56		
198	TR8														78	18	29				58		
199	IOBO8																				60		
200	$\overline{MR10}$																				66		
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

SIGNAL	222	221	I/O EXTENDER X2 (220)	I/O EXTENDER X1 (219)	27 (218)	26 (217)	25 (216)	24 (215)	23 (214)	22 (213)	21 (212)	20 (211)	17 (210)	16 (209)	15 (208)	14 (207)	13 (206)	12 (205)	11 (204)	10 (203)	I/O ADDRESS ENCODER (202)	I/O CONTROL (201)	REF.
$\overline{MR5}$																							161
MR7																							162
IOBO7				63	52								← BUS →							52			163
TAN2																							164
$\overline{TR6}$																							165
IOBO6				61	53								← BUS →							53			166
$\overline{MR4}$																							167
MR6																							168
$\overline{TR5}$																					79		169
TR7																							170
MR5																							171
$\overline{MR7}$																							172
C8																							173
IOBO5				59	51								← BUS →							51			174
$\overline{TR4}$																					78		175
TR4																					81		176
IOBO4				57	42								← BUS →							42			177
$\overline{MR6}$																							178
MR4																							179
TR9																							180
$\overline{TR11}$																							181
$\overline{MR9}$																							182
MR11																							183
IOBO11				73	55								← BUS →							55			184
TAN3																							185
$\overline{TR10}$																							186
IOBO10				71	58								← BUS →							58			187
$\overline{MR8}$																							188
MR10																							189
$\overline{TR9}$																							190
TR11																							191
MR9																							192
$\overline{MR11}$																							193
C12																							194
IOBO9				67	56								← BUS →							56			195
$\overline{TR8}$																							196
TR10																							197
TR8																							198
IOBO8				65	54								← BUS →							54			199
$\overline{MR10}$																							200
	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

		INHIBIT DRIVER 0-1	X-Y DRIVER/ SWITCH 0-1	SENSE AMPLIFIER 0-1	SENSE AMPLIFIER 2-3	X-Y DRIVER/ SWITCH 2-3	INHIBIT DRIVER 2-3	MEMORY PROTECT	PARITY ERROR	MEMORY ADDRESS DECODER	MEMORY DATA BUFFER	INHIBIT DRIVER 4-5	X-Y DRIVER/ SWITCH 4-5	SENSE AMPLIFIER 4-5	SENSE AMPLIFIER 6-7	X-Y DRIVER/ SWITCH 6-7	INHIBIT DRIVER 6-7	POWER FAIL	DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2
REF.	SIGNAL	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
201	MR8							66		36													
202	TR13								13										66				
203	$\overline{TR15}$	9					9		3			9					9						
204	IOBO15																		74	51		78	78
205	TAN4																						
206	$\overline{TR14}$	82					82		4			82					82						
207	IOBO14							43											65		15	76	76
208	$\overline{MR12}$																						
209	MR14							72		64													
210	$\overline{TR13}$	84					84		11			84					84						
211	TR15								5										70				
212	MR13							77		60													
213	C16																						
214	IOBO13							46											61	54		74	74
215	$\overline{TR12}$	78					78		12			78					78						
216	TR14								6										68				
217	TR12								14										62				
218	IOBO12							44											57			68	68
219	MR12							74		56													
220	SB15																						
221	RB15																						
222	RB14																						
223	TB0																						
224	TB1																						
225	TB2																						
226	TB3																						
227	TB4																						
228	TB5																						
229	TB6																						
230	TB7																						
231	TB8																						
232	TB9																						
233	TB10																						
234	TB11																						
235	TB12																						
236	TB13																						
237	TB14																						
238	TB15																						
239	PEH								**62**														
240	SRE								**35**														
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

														EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
201	MR8																				**68**		
202	TR13																30					**9**	
203	$\overline{TR15}$																	36				**15**	
204	IOBO15																					**35**	
205	TAN4															59						**43**	
206	$\overline{TR14}$																					**53**	
207	IOBO14																					**57**	
208	$\overline{MR12}$																					**63**	
209	MR14																					**65**	
210	$\overline{TR13}$																					**10**	
211	TR15																41	38				**16**	
212	MR13																					**18**	
213	C16													50		64						**36**	
214	IOBO13																					**50**	
215	$\overline{TR12}$																					**54**	
216	TR14																33					**56**	
217	TR12																17					**58**	
218	IOBO12																					**60**	
219	MR12																					**68**	
220	SB15															50						**6**	
221	RB15													77		66						**30**	
222	RB14													25								**71**	
223	TB0													79		51			**69**			81	
224	TB1															75			**13**			75	
225	TB2															67			**55**			84	
226	TB3															78			**17**	77		45	
227	TB4																		81	**69**			
228	TB5																		75	**13**			
229	TB6																		74	**55**			
230	TB7																		45	**17**	77		
231	TB8																			81	**69**		
232	TB9																			75	**13**		
233	TB10																			84	**55**		
234	TB11																			45	**17**	77	
235	TB12															76					81	**69**	
236	TB13															73					75	**13**	
237	TB14															70					84	**55**	
238	TB15													80	64	20			77		45	**17**	
239	PEH																	57					
240	SRE																						
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

				I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL	
REF.	SIGNAL	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	REF.
201	MR8																							201
202	TR13																							202
203	$\overline{TR15}$																							203
204	IOBO15				81	74	←						BUS							→	74			204
205	TAN4																							205
206	$\overline{TR14}$																							206
207	IOBO14				79	65	←						BUS							→	65			207
208	$\overline{MR12}$																							208
209	MR14																							209
210	$\overline{TR13}$																							210
211	TR15																							211
212	MR13																							212
213	C16																							213
214	IOBO13				77	61	←						BUS							→	61			214
215	$\overline{TR12}$																							215
216	TR14																							216
217	TR12																							217
218	IOBO12				75	57	←						BUS							→	57			218
219	MR12																							219
220	SB15																							220
221	RB15																							221
222	RB14																							222
223	TB0																					10		223
224	TB1																					9		224
225	TB2																					8		225
226	TB3																					7		226
227	TB4																					6		227
228	TB5																					5		228
229	TB6																							229
230	TB7																							230
231	TB8																							231
232	TB9																							232
233	TB10																							233
234	TB11																							234
235	TB12																							235
236	TB13																							236
237	TB14																							237
238	TB15																							238
239	PEH																							239
240	SRE																							240
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	22 INHIBIT DRIVER 0-1	21 X-Y DRIVER/ SWITCH 0-1	20 SENSE AMPLIFIER 0-1	19 SENSE AMPLIFIER 2-3	18 X-Y DRIVER/ SWITCH 2-3	17 INHIBIT DRIVER 2-3	16 MEMORY PROTECT	15 PARITY ERROR	14 MEMORY ADDRESS DECODER	13 MEMORY DATA BUFFER	12 INHIBIT DRIVER 4-5	11 X-Y DRIVER/ SWITCH 4-5	10 SENSE AMPLIFIER 4-5	9 SENSE AMPLIFIER 6-7	8 X-Y DRIVER/ SWITCH 6-7	7 INHIBIT DRIVER 6-7	6 POWER FAIL	5 DMA PACKER	4 DMA CONTROL	3 DMA ENCODER	2 DMA REGISTER 1	1 DMA REGISTER 2
241	PEI								**61**														
242	MRT1		$^{54}_{57}$			$^{54}_{57}$							$^{54}_{57}$			$^{54}_{57}$							
243	XRT1		$^{30}_{38}$			$^{30}_{38}$				**29**			$^{30}_{38}$			$^{30}_{38}$							
244	XRT2		$^{29}_{34}$			$^{29}_{34}$				**37**			$^{29}_{34}$			$^{29}_{34}$							
245	SWT1									**49**													
246	MOD0	6		3						**35**													
247	MOD1	12		4						**41**													
248	MOD2				3		6			**45**													
249	MOD3				4		12			**51**													
250	$\overline{MOD0/1}$		46							**9**													
251	$\overline{MOD2/3}$					46				**13**													
252	MPT								34	**25**													
253																							
254	SA 0			**15**	**15**						3			**15**	**15**								
255	SA1			**18**	**18**						7			**18**	**18**								
256	SA2			**17**	**17**						11			**17**	**17**								
257	SA3			**20**	**20**						15			**20**	**20**								
258	SA4			**19**	**19**						19			**19**	**19**								
259	SA5			**22**	**22**						23			**22**	**22**								
260	SA6			**21**	**21**						27			**21**	**21**								
261	SA7			**63**	**63**						31			**63**	**63**								
262	SA8			**64**	**64**						35			**64**	**64**								
263	SA9			**65**	**65**						41			**65**	**65**								
264	SA10			**66**	**66**						45			**66**	**66**								
265	SA11			**67**	**67**						51			**67**	**67**								
266	SA12			**68**	**68**						55			**68**	**68**								
267	SA13			**69**	**69**						59			**69**	**69**								
268	SA14			**70**	**70**						63			**70**	**70**								
269	SA15			**71**	**71**						67			**71**	**71**								
270	IOGE(B)																	15		22	84	11	11
271	T3(B)																					5	5
272	SIR							36	37									32		34	70	53	53
273	IAK							56	38									10		27			44
274	IEN20																						
275	IEN6							53												7			35
276	IEN10																						
277	CRS																			32	74	9	9
278	FLG0																			25			30
279	FLG1																						
280	FLG2																						
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
241	PEI																	7					
242	MRT1																	**29**					
243	XRT1																						
244	XRT2																						
245	SWT1																						
246	MOD0																						
247	MOD1																						
248	MOD2																						
249	MOD3																						
250	$\overline{MOD0/1}$																						
251	$\overline{MOD2/3}$																						
252	MPT																						
253																							
254	SA 0																						
255	SA1																						
256	SA2																						
257	SA3																						
258	SA4																						
259	SA5																						
260	SA6																						
261	SA7																						
262	SA8																						
263	SA9																						
264	SA10																						
265	SA11																						
266	SA12																						
267	SA13																						
268	SA14																						
269	SA15																						
270	IOGE(B)																						
271	T3(B)																						
272	SIR																						
273	IAK																						
274	IEN20																						
275	IEN6																						
276	IEN10																						
277	CRS														68								
278	FLG0																						
279	FLG1																						
280	FLG2																						
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

REF.	SIGNAL	222	221	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 27	217 26	216 25	215 24	214 23	213 22	212 21	211 20	210 17	209 16	208 15	207 14	206 13	205 12	204 11	203 10	202 I/O ADDRESS ENCODER	201 I/O CONTROL	REF.
241	PEI																							241
242	MRT1																							242
243	XRT1																							243
244	XRT2																							244
245	SWT1																							245
246	MOD0																							246
247	MOD1																							247
248	MOD2																							248
249	MOD3																							249
250	$\overline{MOD0/1}$																							250
251	$\overline{MOD2/3}$																							251
252	MPT																							252
253																								253
254	SA 0																							254
255	SA1																							255
256	SA2																							256
257	SA3																							257
258	SA4																							258
259	SA5																							259
260	SA6																							260
261	SA7																							261
262	SA8																							262
263	SA9																							263
264	SA10																							264
265	SA11																							265
266	SA12																							266
267	SA13																							267
268	SA14																							268
269	SA15																							269
270	IOGE(B)			15	←								BUS							→	15	34	**37**	270
271	T3(B)			11	←								BUS							→	11		**21**	271
272	SIR			32	←								BUS							→	32		**35**	272
273	IAK			10	←								BUS							→	10		**77**	273
274	IEN20			4		8	←					8	$^{8}_{23}$										**7**	274
275	IEN6																						**$^{5}_{10}$**	275
276	IEN10													8	←					→	8		[illegible]	276
277	CRS			13	←								BUS							→	13		**65**	277
278	FLG0													**4**	**$^{4}_{49}$**					→	**$^{4}_{49}$**	14		278
279	FLG1				**26**	**$^{4}_{49}$**	←					→	**$^{4}_{49}$**	**49**								16		279
280	FLG2				**28**																	13		280
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

(shaded box) SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1 22	X-Y DRIVER/ SWITCH 0-1 21	SENSE AMPLIFIER 0-1 20	SENSE AMPLIFIER 2-3 19	X-Y DRIVER/ SWITCH 2-3 18	INHIBIT DRIVER 2-3 17	MEMORY PROTECT 16	PARITY ERROR 15	MEMORY ADDRESS DECODER 14	MEMORY DATA BUFFER 13	INHIBIT DRIVER 4-5 12	X-Y DRIVER/ SWITCH 4-5 11	SENSE AMPLIFIER 4-5 10	SENSE AMPLIFIER 6-7 9	X-Y DRIVER/ SWITCH 6-7 8	INHIBIT DRIVER 6-7 7	POWER FAIL 6	DMA PACKER 5	DMA CONTROL 4	DMA ENCODER 3	DMA REGISTER 1 2	DMA REGISTER 2 1
281	FLG3																						
282	SKF																	12		29			15
283	ENF								71									46		37	49		
284	INT							31	79									28					
285	IOS																						
286	$\overline{PH5}$																						
287	ESR																						
288	SCL0																				32		
289	SCL1							71													80		
290	SCL2																				18		13
291	SCL3																				82	13	
292	SCL4																	16			38		
293	SCL5							12	9												79		
294	SCL6																			36	46		
295	SCL7																			38	50		
296	SCM0							9	7									14		18	51	14	14
297	SCM1																				67		
298	SCM2																				69		
299	SCM3																						
300	SCM4																						
301	SCM5																						
302	SCM6																						
303	SCM7																						
304	IRQ1																						
305	IRQ2																						
306	IRQ3																						
307	IRQ4																	6					
308	IRQ5							35	77														
309	IRQ6																			28			29
310	IRQ7																			26			
311	IRQ10																						
312	IRQ11																						
313	IRQ12																						
314	IRQ13																						
315	IRQ14																						
316	IRQ15																						
317	IRQ16																						
318	IRQ17																						

LOGIC

REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	EAU LOGIC 110	EAU TIMING 109	SHIFT LOGIC 108	INSTRUCTION DECODER 107	TIMING GENERATOR 106	ARITHMETIC LOGIC 0-3 105	ARITHMETIC LOGIC 4-7 104	ARITHMETIC LOGIC 8-11 103	ARITHMETIC LOGIC 12-15 102	FRONT PANEL COUPLER 101
281	FLG3																						
282	SKF															31							
283	ENF																						
284	INT																	44					
285	IOS														29	81							
286	$\overline{PH5}$																						
287	ESR																						
288	SCL0																						
289	SCL1																						
290	SCL2																						
291	SCL3																						
292	SCL4																						
293	SCL5																						
294	SCL6																						
295	SCL7																						
296	SCM0																						
297	SCM1																						
298	SCM2																						
299	SCM3																						
300	SCM4																						
301	SCM5																						
302	SCM6																						
303	SCM7																						
304	IRQ1																						
305	IRQ2																						
306	IRQ3																						
307	IRQ4																						
308	IRQ5																						
309	IRQ6																						
310	IRQ7																						
311	IRQ10																						
312	IRQ11																						
313	IRQ12																						
314	IRQ13																						
315	IRQ14																						
316	IRQ15																						
317	IRQ16																						
318	IRQ17																						

INPUT/OUTPUT

REF.	SIGNAL	222	221	I/O EXTENDER X2 220	I/O EXTENDER X1 219	27 218	26 217	25 216	24 215	23 214	22 213	21 212	20 211	17 210	16 209	15 208	14 207	13 206	12 205	11 204	10 203	I/O ADDRESS ENCODER 202	I/O CONTROL 201	REF.
281	FLG3				30																	15		281
282	SKF			12	◄—								BUS								—► 12		73	282
283	ENF			46	◄—								BUS								—► 46		67	283
284	INT																					3		284
285	IOS																						6	285
286	$\overline{PH5}$																					4	9	286
287	ESR																					12	21	287
288	SCL0			67		34							16	34							16	65	38	288
289	SCL1			71								16	34							16	34	67	42	289
290	SCL2			73							16	34							16	34		61		290
291	SCL3			75						16	34							16	34			63		291
292	SCL4			77					16	34							16	34				51		292
293	SCL5			79				16	34							16	34					52		293
294	SCL6			81			16	34							16	34						49		294
295	SCL7			83		16	34							16	34							50		295
296	SCM0			55																		75	36	296
297	SCM1													14	14 37 ◄—						—► 14 37	77		297
298	SCM2					14	14 37 ◄—						—► 14 37	37								71		298
299	SCM3			57		37																73		299
300	SCM4			59																		56		300
301	SCM5			61																		57		301
302	SCM6			63																		54		302
303	SCM7			65																		55		303
304	IRQ1				50							6	33									17		304
305	IRQ2				52						6	33										21		305
306	IRQ3				54					6	33											23		306
307	IRQ4				56				6	33												27		307
308	IRQ5				58			6	33													29		308
309	IRQ6				60		6	33														25		309
310	IRQ7				62	6	33															19		310
311	IRQ10				64	33															6	33		311
312	IRQ11				66															6	33	35		312
313	IRQ12				68														6	33		37		313
314	IRQ13				72													6	33			18		314
315	IRQ14				74												6	33				31		315
316	IRQ15				76											6	33					20		316
317	IRQ16				78										6	33						38		317
318	IRQ17				80									6	33							22		318

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

		INHIBIT DRIVER 0-1	X-Y DRIVER/ SWITCH 0-1	SENSE AMPLIFIER 0-1	SENSE AMPLIFIER 2-3	X-Y DRIVER/ SWITCH 2-3	INHIBIT DRIVER 2-3	MEMORY PROTECT	PARITY ERROR	MEMORY ADDRESS DECODER	MEMORY DATA BUFFER	INHIBIT DRIVER 4-5	X-Y DRIVER/ SWITCH 4-5	SENSE AMPLIFIER 4-5	SENSE AMPLIFIER 6-7	X-Y DRIVER/ SWITCH 6-7	INHIBIT DRIVER 6-7	POWER FAIL	DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2
REF.	SIGNAL	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
319	PRH10/PRL7																			9			
320	PRH11/PRL10																						
321	PRH12/PRL11																						
322	PRH13/PRL12																						
323	PRH14/PRL13																						
324	PRH15/PRL14																						
325	PRH16/PRL15																						
326	PRH17/PRL16																						
327	PRH20/PRL17																						
328	PRH21/PRL20																						
329	PRH22/PRL21																						
330	PRH23/PRL22																						
331	PRH24/PRL23																						
332	PRH25/PRL24																						
333	PRH26/PRL25																						
334	PRH27/PRL26																						
335	PRH30/PRL27																						
336	PRH5/PRL4							38	25									3			57		
337	PRH6/PRL5							51	27														33
338	POPIO(B)							29												35			
339	IOBI0							79											26			17	17
340	IOBI1							80											29			25	25
341	IOBI2							78											30			28	28
342	IOBI3							75											64			58	58
343	IOBI4							81											77			77	77
344	IOBI5							82											80			80	80
345	IOBI6							84											81			79	79
346	IOBI7							83											84			81	81
347	IOBI8							64											27			21	21
348	IOBI9							65											28			19	19
349	IOBI10							67											31			27	27
350	IOBI11							62											60			49	49
351	IOBI12							70											78			61	61
352	IOBI13							73											79			75	75
353	IOBI14							76											82				73
354	IOBI15								28										83				
355	IOBI16																						
356	SRQ10																				22		
357	SRQ11																				28		
358	SRQ12																				20		
359	SRQ13																				26		
360	SRQ14																				33		
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

														EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
319	PRH10/PRL7																						
320	PRH11/PRL10																						
321	PRH12/PRL11																						
322	PRH13/PRL12																						
323	PRH14/PRL13																						
324	PRH15/PRL14																						
325	PRH16/PRL15																						
326	PRH17/PRL16																						
327	PRH20/PRL17																						
328	PRH21/PRL20																						
329	PRH22/PRL21																						
330	PRH23/PRL22																						
331	PRH24/PRL23																						
332	PRH25/PRL24																						
333	PRH26/PRL25																						
334	PRH27/PRL26																						
335	PRH30/PRL27																						
336	PRH5/PRL4																						
337	PRH6/PRL5																						
338	POPIO(B)																						
339	IOBI0																		79				3
340	IOBI1																		32				7
341	IOBI2																		33				11
342	IOBI3																		27				15
343	IOBI4																			79			19
344	IOBI5																			32			23
345	IOBI6																			33			27
346	IOBI7																			27			31
347	IOBI8																				79		35
348	IOBI9																				32		41
349	IOBI10																				33		45
350	IOBI11																				27		51
351	IOBI12																					79	55
352	IOBI13																					32	59
353	IOBI14																					33	63
354	IOBI15																					27	67
355	IOBI16																						
356	SRQ10																						
357	SRQ11																						
358	SRQ12																						
359	SRQ13																						
360	SRQ14																						
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

				I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL	
REF.	SIGNAL	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	REF.
319	PRH10/PRL7																				23		12 80 14	319
320	PRH11/PRL10																			23	3			320
321	PRH12/PRL11																		23	3				321
322	PRH13/PRL12																	23	3					322
323	PRH14/PRL13																23	3						323
324	PRH15/PRL14															23	3							324
325	PRH16/PRL15														23	3								325
326	PRH17/PRL16													23	3									326
327	PRH20/PRL17												23	3									16	327
328	PRH21/PRL20											23	3											328
329	PRH22/PRL21										23	3												329
330	PRH23/PRL22									23	3													330
331	PRH24/PRL23								23	3														331
332	PRH25/PRL24							23	3															332
333	PRH26/PRL25						23	3																333
334	PRH27/PRL26					23	3																	334
335	PRH30/PRL27			3		3																		335
336	PRH5/PRL4																						84	336
337	PRH6/PRL5																						76 82	337
338	POPIO(B)			17									← BUS →								17		72	338
339	IOBI0			50		26							← BUS →								26	26		339
340	IOBI1			52		29							← BUS →								29	28		340
341	IOBI2			54		30							← BUS →								30	41		341
342	IOBI3			56		64							← BUS →								64	45		342
343	IOBI4			58		77							← BUS →								77	42		343
344	IOBI5			60		80							← BUS →								80	30		344
345	IOBI6			62		81							← BUS →								81			345
346	IOBI7			64		84							← BUS →								84			346
347	IOBI8			66		27							← BUS →								27			347
348	IOBI9			68		28							← BUS →								28			348
349	IOBI10			72		31							← BUS →								31			349
350	IOBI11			74		60							← BUS →								60			350
351	IOBI12			76		78							← BUS →								78			351
352	IOBI13			78		79							← BUS →								79			352
353	IOBI14			80		82							← BUS →								82			353
354	IOBI15			82		83							← BUS →								83			354
355	IOBI16			30		18							← BUS →								18			355
356	SRQ10																				19			356
357	SRQ11																			19				357
358	SRQ12																		19					358
359	SRQ13																	19						359
360	SRQ14																19							360
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1	X-Y DRIVER/ SWITCH 0-1	SENSE AMPLIFIER 0-1	SENSE AMPLIFIER 2-3	X-Y DRIVER/ SWITCH 2-3	INHIBIT DRIVER 2-3	MEMORY PROTECT	PARITY ERROR	MEMORY ADDRESS DECODER	MEMORY DATA BUFFER	INHIBIT DRIVER 4-5	X-Y DRIVER/ SWITCH 4-5	SENSE AMPLIFIER 4-5	SENSE AMPLIFIER 6-7	X-Y DRIVER/ SWITCH 6-7	INHIBIT DRIVER 6-7	POWER FAIL	DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
361	SRQ15																				44		
362	SRQ16																				29		
363	SRQ17																				37		
364	SRQ20																				71		
365	SRQ21																				66		
366	SRQ22																				68		
367	SRQ23																				64		
368	SRQ24																				58		
369	SRQ25																				54		
370	SRQ26																				56		
371	SRQ27																				52		
372	IOBO16																						
373	HIS																				**83**		
374	EDT																			**42**			
375	IOGE							19										**59**					
376	PNS																						
377	MNS																						
378	ILS																						
389	PON		42			42							42			42		58					
380	POFP																	56					
381	PRS																	78					
382	$\overline{PRSW}$																						
383	$\overline{RNSW}$																						
384	RNSW																	60					
385	$\overline{HLS}$																						
386	HLS																	72					
387	LMS																						
388	LAS																						
389	LBS																						
390	LADS																						
391	DMS																						
392	SCS																						
393	LPS									31													
394	PIND																	49					
395	-5.6V																	75					
396	R SET																						
397	DS3																						
398	DS4																						
399	DS34																						
400	D5L8																						

LOGIC

REF.	SIGNAL													EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
361	SRQ15																						
362	SRQ16																						
363	SRQ17																						
364	SRQ20																						
365	SRQ21																						
366	SRQ22																						
367	SRQ23																						
368	SRQ24																						
369	SRQ25																						
370	SRQ26																						
371	SRQ27																						
372	IOBO16																						
373	HIS																						
374	EDT																						
375	IOGE															16							
376	PNS																	43					**18**
377	MNS																	12					**22**
378	ILS																73						**26**
389	PON																						**71**
380	POFP																	77					**10**
381	PRS																	78					**30**
382	$\overline{PRSW}$																	79					**34**
383	$\overline{RNSW}$																						
384	RNSW																	70					**44**
385	$\overline{HLS}$																	45					**50**
386	HLS																	50					**54**
387	LMS																	46					**58**
388	LAS																	80					**62**
389	LBS																	65					**66**
390	LADS																	68					**70**
391	DMS																	59					**74**
392	SCS																	56					**78**
393	LPS																						**82**
394	PIND																						**75**
395	-5.6V																						79
396	R SET													63	**42**								
397	DS3													67	**28**								
398	DS4													52	**9**								
399	DS34													14	**6**								
400	D5L8													71	**27**								

INPUT/OUTPUT

REF.	SIGNAL			I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL	REF.
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	
361	SRQ15															**19**								361
362	SRQ16														**19**									362
363	SRQ17													**19**										363
364	SRQ20												**19**											364
365	SRQ21											**19**												365
366	SRQ22										**19**													366
367	SRQ23									**19**														367
368	SRQ24								**19**															368
369	SRQ25							**19**																369
370	SRQ26						**19**																	370
371	SRQ27					**19**																		371
372	IOBO16				83	73	←						BUS							→	73			372
373	HIS																						4	373
374	EDT				3	62	←						BUS							→	62			374
375	IOGE																						33	375
376	PNS																							376
377	MNS																							377
378	ILS																							378
389	PON				41	66	←						BUS							→	66			379
380	POFP																							380
381	PRS																							381
382	$\overline{PRSW}$																							382
383	$\overline{RNSW}$																							383
384	RNSW																							384
385	$\overline{HLS}$																							385
386	HLS																							386
387	LMS					59	←						BUS							→	59			387
388	LAS																							388
389	LBS																							389
390	LADS																							390
391	DMS																							391
392	SCS																							392
393	LPS																							393
394	PIND																							394
395	-5.6V																							395
396	R SET																							396
397	DS3																							397
398	DS4																							398
399	DS34																							399
400	D5L8																							400

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL (shaded pin numbers shown in bold)

Table 7-3. Backplane Wiring List (Continued)

		MEMORY																					
		INHIBIT DRIVER 0-1	X-Y DRIVER/ SWITCH 0-1	SENSE AMPLIFIER 0-1	SENSE AMPLIFIER 2-3	X-Y DRIVER/ SWITCH 2-3	INHIBIT DRIVER 2-3	MEMORY PROTECT	PARITY ERROR	MEMORY ADDRESS DECODER	MEMORY DATA BUFFER	INHIBIT DRIVER 4-5	X-Y DRIVER/ SWITCH 4-5	SENSE AMPLIFIER 4-5	SENSE AMPLIFIER 6-7	X-Y DRIVER/ SWITCH 6-7	INHIBIT DRIVER 6-7	POWER FAIL	DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2
REF.	SIGNAL	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
401	SRCS																						
402	MD2																						
403	ISG																			3			
404	OVD																						
405	ROT5																						
406	OASL																						
407	RSDS							**15**	72														
408	T2T3(B)																						
409	MP1																						
410	MP2																						
411	MP3																						
412	MP4																						
413	MP5																						
414	D1																						
415	D2																						
416	D3																						
417	D4																						
418	D5																						
419	D6																						
420	TOD																						
421	TEV																						
422	OVR																						
423	$\overline{OVR}$																						
424	RO																						
425	AS																						
426	RT																						
427	$\overline{RT}$																						
428	EXIT																						
429	GATE																						
430	DL3																						
431	DL4																						
432	SLMB									73													
433	SRMB									61													
434	SL14B									84													
435	EOFB									82													
436	CMFB									80													
437	IIR							69		71													
438	MPC							**25**	63									36					
439	MMD13					25				**19**													
440	MMD14									**23**			25										
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

		LOGIC																					
														EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
401	SRCS													83	**31**								
402	MD2													16	**79**								
403	ISG														**63**			4					
404	OVD													**56**	80								
405	ROT5													68	**82**								
406	OASL													**31**	5								
407	RSDS														65								
408	T2T3(B)													**21**	35								
409	MP1													59	**12**								
410	MP2													5	**11**								
411	MP3													69	**4**								
412	MP4													46	**3**								
413	MP5													9	**8**								
414	D1													62	**34**								
415	D2													60	**33**								
416	D3													27	**26**								
417	D4													6	**25**								
418	D5													73	**17**								
419	D6													8	**18**								
420	TOD													82	**45**								
421	TEV													81	**56**								
422	OVR													35	**22**								
423	$\overline{OVR}$													64	**16**								
424	RO													75	**46**								
425	AS													84	**50**								
426	RT													57	**52**								
427	$\overline{RT}$													78	**58**								
428	EXIT													17	**74**								
429	GATE													76	**59**								
430	DL3													70	**57**								
431	DL4													18	**36**								
432	SLMB														**44**								
433	SRMB														**41**								
434	SL14B														**49**								
435	EOFB													**26**									
436	CMFB													**72**									
437	IIR														**77**			6					
438	MPC																						
439	MMD13																						
440	MMD14																						
		122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

		INPUT/OUTPUT																						
				I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL	
REF.	SIGNAL	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	REF.
401	SRCS																							401
402	MD2																							402
403	ISG																							403
404	OVD																							404
405	ROT5																							405
406	OASL																							406
407	RSDS																							407
408	T2T3(B)																							408
409	MP1																							409
410	MP2																							410
411	MP3																							411
412	MP4																							412
413	MP5																							413
414	D1																							414
415	D2																							415
416	D3																							416
417	D4																							417
418	D5																							418
419	D6																							419
420	TOD																							420
421	TEV																							421
422	OVR																							422
423	$\overline{OVR}$																							423
424	RO																							424
425	AS																							425
426	RT																							426
427	$\overline{RT}$																							427
428	EXIT																							428
429	GATE																							429
430	DL3																							430
431	DL4																							431
432	SLMB																							432
433	SRMB																							433
434	SL14B																							434
435	EOFB																							435
436	CMFB																							436
437	IIR																							437
438	MPC																							438
439	MMD13																							439
440	MMD14																							440
		222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL (shaded pin numbers shown in bold)

Table 7-3. Backplane Wiring List (Continued)

REF.	SIGNAL	MEMORY: INHIBIT DRIVER 0-1 (22)	X-Y DRIVER/SWITCH 0-1 (21)	SENSE AMPLIFIER 0-1 (20)	SENSE AMPLIFIER 2-3 (19)	X-Y DRIVER/SWITCH 2-3 (18)	INHIBIT DRIVER 2-3 (17)	MEMORY PROTECT (16)	PARITY ERROR (15)	MEMORY ADDRESS DECODER (14)	MEMORY DATA BUFFER (13)	INHIBIT DRIVER 4-5 (12)	X-Y DRIVER/SWITCH 4-5 (11)	SENSE AMPLIFIER 4-5 (10)	SENSE AMPLIFIER 6-7 (9)	X-Y DRIVER/SWITCH 6-7 (8)	INHIBIT DRIVER 6-7 (7)	POWER FAIL (6)	DMA PACKER (5)	DMA CONTROL (4)	DMA ENCODER (3)	DMA REGISTER 1 (2)	DMA REGISTER 2 (1)	LOGIC: EAU LOGIC (110)	EAU TIMING (109)	SHIFT LOGIC (108)	INSTRUCTION DECODER (107)	TIMING GENERATOR (106)	ARITHMETIC LOGIC 0-3 (105)	ARITHMETIC LOGIC 4-7 (104)	ARITHMETIC LOGIC 8-11 (103)	ARITHMETIC LOGIC 12-15 (102)	FRONT PANEL COUPLER (101)	INPUT/OUTPUT: I/O EXTENDER X2 (220)	I/O EXTENDER X1 (219)	27 (218)	26 (217)	25 (216)	24 (215)	23 (214)	22 (213)	21 (212)	20 (211)	17 (210)	16 (209)	15 (208)	14 (207)	13 (206)	12 (205)	11 (204)	10 (203)	I/O ADDRESS ENCODER (202)	I/O CONTROL (201)	REF.
441	SWT2									57																																						441
442	PH5																			5																												442
443	PH5							7	8	69	84									8	78		70		53																						17	443
444	IODO																		19	4																												444
445	COUT																			63	36																											445
446	OUT																			65	6																											446
447	CM1																			67	7																											447
448	SMAR2																			69		38																											448
449	CR2																			71	27																											449
450	DIN1																			75			4																									450
451	WCR1																			77			84																									451
452	SWCR2																			79		3																											452
453	IN																			52																											453
454	TE1																			66	60																											454
455																																																455
456	CM2																			68	81																											456
457	CIN																			70	41																											457
458	SMAR1																			72			38																											458
459	DIN2																			74		4																											459
460	WCR2																			76		84																											460
461	CR1																			78	34																											461
462	SWCR1																			80			3																											462
463	TE2																			62	62																											463
464	TR0(B)																		4																													464
465	TR1(B)																		6																													465
466	TR2(B)																		8																													466
467	TR3(B)																		10																													467
468	TR4(B)																		12																													468
469	TR5(B)																		14																													469
470	TR6(B)																		16																													470
471	TR7(B)																		18																													471
472	TR8(B)																		33																													472
473	TR9(B)																		37																													473
474	TR10(B)																		44																													474
475	TR11(B)																		49																													475
476	TR12(B)																		59																													476
477	TR13(B)																		63																													477
478	TR14(B)																		67																													478
479	TR15(B)																		69																													479
480	OHC1																		20		10																											480
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	110	109	108	107	106	105	104	103	102	101	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	22 INHIBIT DRIVER 0-1	21 X-Y DRIVER/ SWITCH 0-1	20 SENSE AMPLIFIER 0-1	19 SENSE AMPLIFIER 2-3	18 X-Y DRIVER/ SWITCH 2-3	17 INHIBIT DRIVER 2-3	16 MEMORY PROTECT	15 PARITY ERROR	14 MEMORY ADDRESS DECODER	13 MEMORY DATA BUFFER	12 INHIBIT DRIVER 4-5	11 X-Y DRIVER/ SWITCH 4-5	10 SENSE AMPLIFIER 4-5	9 SENSE AMPLIFIER 6-7	8 X-Y DRIVER/ SWITCH 6-7	7 INHIBIT DRIVER 6-7	6 POWER FAIL	5 DMA PACKER	4 DMA CONTROL	3 DMA ENCODER	2 DMA REGISTER 1	1 DMA REGISTER 2
481	OHC2																		21		12		
482	OLC1																		22		19		
483	OLC2																		23		13		
484	IDW1																		24		16		
485	IDW2																		25		14		
486	IHC1																		32		9		
487	IHC2																		36		8		
488	DE1																				53		
489	DE2																				55		
490	MOD4									55		6		3									
491	$\overline{TR16}$	7					7		53			7					7						
492	SA16			72	72						71			72	72								
493	MOD5									59		12		4									
494	MOD6									63					3		6						
495	MOD7									5					4		12						
496	MPT1		27			28				3													
497	MPT2					27				7			28										
498	MPT3									11			27			28							
499	MPT4									15						27							
500	RUN																						
501	SPARE																						
502	$\overline{MOD4/5}$									17			46										
503	PRL6																			31			23
504	TSA							27	17												45	59	59
505	$\overline{MOD6/7}$									21						46							
506	M14									66			23									7	7
507	ID0M0	25		25																			
508	ID0M1	26		26																			
509	ID1M0	27		27																			
510	ID1M1	28		28																			
511	ID2M0	29		29																			
512	ID2M1	30		30																			
513	ID3M0	31		31																			
514	ID3M1	32		32																			
515	ID4M0	33		33																			
516	ID4M1	34		34																			
517	ID5M0	35		35																			
518	ID5M1	36		36																			
519	ID6M0	37		37																			
520	ID6M1	38		38																			

LOGIC

REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110 EAU LOGIC	109 EAU TIMING	108 SHIFT LOGIC	107 INSTRUCTION DECODER	106 TIMING GENERATOR	105 ARITHMETIC LOGIC 0-3	104 ARITHMETIC LOGIC 4-7	103 ARITHMETIC LOGIC 8-11	102 ARITHMETIC LOGIC 12-15	101 FRONT PANEL COUPLER
481	OHC2																						
482	OLC1																						
483	OLC2																						
484	IDW1																						
485	IDW2																						
486	IHC1																						
487	IHC2																						
488	DE1																						
489	DE2																						
490	MOD4																						
491	$\overline{TR16}$																						
492	SA16																						
493	MOD5																						
494	MOD6																						
495	MOD7																						
496	MPT1																						
497	MPT2																						
498	MPT3																						
499	MPT4																						
500	RUN																						
501	SPARE																						
502	$\overline{MOD4/5}$																						
503	PRL6																						
504	TSA													29	76			67					
505	$\overline{MOD6/7}$																						
506	M14																						
507	ID0M0																						
508	ID0M1																						
509	ID1M0																						
510	ID1M1																						
511	ID2M0																						
512	ID2M1																						
513	ID3M0																						
514	ID3M1																						
515	ID4M0																						
516	ID4M1																						
517	ID5M0																						
518	ID5M1																						
519	ID6M0																						
520	ID6M1																						

INPUT/OUTPUT

REF.	SIGNAL	222	221	220 I/O EXTENDER X2	219 I/O EXTENDER X1	218 (27)	217 (26)	216 (25)	215 (24)	214 (23)	213 (22)	212 (21)	211 (20)	210 (17)	209 (16)	208 (15)	207 (14)	206 (13)	205 (12)	204 (11)	203 (10)	202 I/O ADDRESS ENCODER	201 I/O CONTROL	REF.
481	OHC2																							481
482	OLC1																							482
483	OLC2																							483
484	IDW1																							484
485	IDW2																							485
486	IHC1																							486
487	IHC2																							487
488	DE1																							488
489	DE2																							489
490	MOD4																							490
491	$\overline{TR16}$																							491
492	SA16																							492
493	MOD5																							493
494	MOD6																							494
495	MOD7																							495
496	MPT1																							496
497	MPT2																							497
498	MPT3																							498
499	MPT4																							499
500	RUN			41		50	←						BUS							→	50	32		500
501	SPARE			84		68	←						BUS							→	68			501
502	$\overline{MOD4/5}$																							502
503	PRL6																						78	503
504	TSA																							504
505	$\overline{MOD6/7}$																							505
506	M14																							506
507	ID0M0																							507
508	ID0M1																							508
509	ID1M0																							509
510	ID1M1																							510
511	ID2M0																							511
512	ID2M1																							512
513	ID3M0																							513
514	ID3M1																							514
515	ID4M0																							515
516	ID4M1																							516
517	ID5M0																							517
518	ID5M1																							518
519	ID6M0																							519
520	ID6M1																							520

NOTES:

▒ SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

		INHIBIT DRIVER 0-1	X-Y DRIVER/ SWITCH 0-1	SENSE AMPLIFIER 0-1	SENSE AMPLIFIER 2-3	X-Y DRIVER/ SWITCH 2-3	INHIBIT DRIVER 2-3	MEMORY PROTECT	PARITY ERROR	MEMORY ADDRESS DECODER	MEMORY DATA BUFFER	INHIBIT DRIVER 4-5	X-Y DRIVER/ SWITCH 4-5	SENSE AMPLIFIER 4-5	SENSE AMPLIFIER 6-7	X-Y DRIVER/ SWITCH 6-7	INHIBIT DRIVER 6-7	POWER FAIL	DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2
REF.	SIGNAL	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
521	ID7M0	41		41																			
522	ID7M1	42		42																			
523	ID8M0	43		43																			
524	ID8M1	44		44																			
525	ID9M0	45		45																			
526	ID9M1	46		46																			
527	ID10M0	49		49																			
528	ID10M1	50		50																			
529	ID11M0	51		51																			
530	ID11M1	52		52																			
531	ID12M0	53		53																			
532	ID12M1	54		54																			
533	ID13M0	55		55																			
534	ID13M1	56		56																			
535	ID14M0	57		57																			
536	ID14M1	58		58																			
537	ID15M0	59		59																			
538	ID15M1	60		60																			
539	ID16M0	61		61																			
540	ID16M1	62		62																			
541	ID0M2				25		25																
542	ID0M3				26		26																
543	ID1M2				27		27																
544	ID1M3				28		28																
545	ID2M2				29		29																
546	ID2M3				30		30																
547	ID3M2				31		31																
548	ID3M3				32		32																
549	ID4M2				33		33																
550	ID4M3				34		34																
551	ID5M2				35		35																
552	ID5M3				36		36																
553	ID6M2				37		37																
554	ID6M3				38		38																
555	ID7M2				41		41																
556	ID7M3				42		42																
557	ID8M2				43		43																
558	ID8M3				44		44																
559	ID9M2				45		45																
560	ID9M3				46		46																
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

												EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
REF.	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
521																						
522																						
523																						
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558																						
559																						
560																						
	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

		I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL	
222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	REF.
																						521
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																						560
222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1 (22)	X-Y DRIVER/ SWITCH 0-1 (21)	SENSE AMPLIFIER 0-1 (20)	SENSE AMPLIFIER 2-3 (19)	X-Y DRIVER/ SWITCH 2-3 (18)	INHIBIT DRIVER 2-3 (17)	MEMORY PROTECT (16)	PARITY ERROR (15)	MEMORY ADDRESS DECODER (14)	MEMORY DATA BUFFER (13)	INHIBIT DRIVER 4-5 (12)	X-Y DRIVER/ SWITCH 4-5 (11)	SENSE AMPLIFIER 4-5 (10)	SENSE AMPLIFIER 6-7 (9)	X-Y DRIVER/ SWITCH 6-7 (8)	INHIBIT DRIVER 6-7 (7)	POWER FAIL (6)	DMA PACKER (5)	DMA CONTROL (4)	DMA ENCODER (3)	DMA REGISTER 1 (2)	DMA REGISTER 2 (1)
561	ID10M2				49		**49**																
562	ID10M3				50		**50**																
563	ID11M2				51		**51**																
564	ID11M3				52		**52**																
565	ID12M2				53		**53**																
566	ID12M3				54		**54**																
567	ID13M2				55		**55**																
568	ID13M3				56		**56**																
569	ID14M2				57		**57**																
570	ID14M3				58		**58**																
571	ID15M2				59		**59**																
572	ID15M3				60		**60**																
573	ID16M2				61		**61**																
574	ID16M3				62		**62**																
575	ID0M4											**25**		25									
576	ID0M5											**26**		26									
577	ID1M4											**27**		27									
578	ID1M5											**28**		28									
579	ID2M4											**29**		29									
580	ID2M5											**30**		30									
581	ID3M4											**31**		31									
582	ID3M5											**32**		32									
583	ID4M4											**33**		33									
584	ID4M5											**34**		34									
585	ID5M4											**35**		35									
586	ID5M5											**36**		36									
587	ID6M4											**37**		37									
588	ID6M5											**38**		38									
589	ID7M4											**41**		41									
590	ID7M5											**42**		42									
591	ID8M4											**43**		43									
592	ID8M5											**44**		44									
593	ID9M4											**45**		45									
594	ID9M5											**46**		46									
495	ID10M4											**49**		49									
596	ID10M5											**50**		50									
597	ID11M4											**51**		51									
598	ID11M5											**52**		52									
599	ID12M4											**53**		53									
600	ID12M5											**54**		54									
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

REF.	122	121	120	119	118	117	116	115	114	113	112	111	EAU LOGIC (110)	EAU TIMING (109)	SHIFT LOGIC (108)	INSTRUCTION DECODER (107)	TIMING GENERATOR (106)	ARITHMETIC LOGIC 0-3 (105)	ARITHMETIC LOGIC 4-7 (104)	ARITHMETIC LOGIC 8-11 (103)	ARITHMETIC LOGIC 12-15 (102)	FRONT PANEL COUPLER (101)
561																						
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599																						
600																						
	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

REF.	222	221	I/O EXTENDER X2 (220)	I/O EXTENDER X1 (219)	27 (218)	26 (217)	25 (216)	24 (215)	23 (214)	22 (213)	21 (212)	20 (211)	17 (210)	16 (209)	15 (208)	14 (207)	13 (206)	12 (205)	11 (204)	10 (203)	I/O ADDRESS ENCODER (202)	I/O CONTROL (201)	REF.
561																							561
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563																							563
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598																							598
599																							599
600																							600
	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:

▒ SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL (shaded values shown in bold)

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1 22	X-Y DRIVER/ SWITCH 0-1 21	SENSE AMPLIFIER 0-1 20	SENSE AMPLIFIER 2-3 19	X-Y DRIVER/ SWITCH 2-3 18	INHIBIT DRIVER 2-3 17	MEMORY PROTECT 16	PARITY ERROR 15	MEMORY ADDRESS DECODER 14	MEMORY DATA BUFFER 13	INHIBIT DRIVER 4-5 12	X-Y DRIVER/ SWITCH 4-5 11	SENSE AMPLIFIER 4-5 10	SENSE AMPLIFIER 6-7 9	X-Y DRIVER/ SWITCH 6-7 8	INHIBIT DRIVER 6-7 7	POWER FAIL 6	DMA PACKER 5	DMA CONTROL 4	DMA ENCODER 3	DMA REGISTER 1 2	DMA REGISTER 2 1
601	MD13M4											**55**		55									
602	ID13M5											**56**		56									
603	ID14M4											**57**		57									
604	ID14M5											**58**		58									
605	ID15M4											**59**		59									
606	ID15M5											**60**		60									
607	ID16M4											**61**		61									
608	ID16M5											**62**		62									
609	ID0M6														25		**25**						
610	ID0M7														26		**26**						
611	ID1M6														27		**27**						
612	ID1M7														28		**28**						
613	ID2M6														29		**29**						
614	ID2M7														30		**30**						
615	ID3M6														31		**31**						
616	ID3M7														32		**32**						
617	ID4M6														33		**33**						
618	ID4M7														34		**34**						
619	ID5M6														35		**35**						
620	ID5M7														36		**36**						
621	ID6M6														37		**37**						
622	ID6M7														38		**38**						
623	ID7M6														41		**41**						
624	ID7M7														42		**42**						
625	ID8M6														43		**43**						
626	ID8M7														44		**44**						
627	ID9M6														45		**45**						
628	ID9M7														46		**46**						
629	ID10M6														49		**49**						
630	ID10M7														50		**50**						
631	ID11M6														51		**51**						
632	ID11M7														52		**52**						
633	ID12M6														53		**53**						
634	ID12M7														54		**54**						
635	ID13M6														55		**55**						
636	ID13M7														56		**56**						
637	ID14M6														57		**57**						
638	ID14M7														58		**58**						
639	ID15M6														59		**59**						
640	ID15M7														60		**60**						
		22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

LOGIC

REF.	122	121	120	119	118	117	116	115	114	113	112	111	EAU LOGIC 110	EAU TIMING 109	SHIFT LOGIC 108	INSTRUCTION DECODER 107	TIMING GENERATOR 106	ARITHMETIC LOGIC 0-3 105	ARITHMETIC LOGIC 4-7 104	ARITHMETIC LOGIC 8-11 103	ARITHMETIC LOGIC 12-15 102	FRONT PANEL COUPLER 101
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639																						
640																						
	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101

INPUT/OUTPUT

222	221	I/O EXTENDER X2 220	I/O EXTENDER X1 219	27 218	26 217	25 216	24 215	23 214	22 213	21 212	20 211	17 210	16 209	15 208	14 207	13 206	12 205	11 204	10 203	I/O ADDRESS ENCODER 202	I/O CONTROL 201	REF.
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																						634
																						635
																						636
																						637
																						638
																						639
																						640
222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	

NOTES:
SHADED PIN NUMBERS INDICATE SOURCE OF SIGNAL (shaded pin numbers shown in bold above)

Table 7-3. Backplane Wiring List (Continued)

MEMORY

REF.	SIGNAL	INHIBIT DRIVER 0-1	X-Y DRIVER/ SWITCH 0-1	SENSE AMPLIFIER 0-1	SENSE AMPLIFIER 2-3	X-Y DRIVER/ SWITCH 2-3	INHIBIT DRIVER 2-3	MEMORY PROTECT	PARITY ERROR	MEMORY ADDRESS DECODER	MEMORY DATA BUFFER	INHIBIT DRIVER 4-5	X-Y DRIVER/ SWITCH 4-5	SENSE AMPLIFIER 4-5	SENSE AMPLIFIER 6-7	X-Y DRIVER/ SWITCH 6-7	INHIBIT DRIVER 6-7	POWER FAIL	DMA PACKER	DMA CONTROL	DMA ENCODER	DMA REGISTER 1	DMA REGISTER 2
REF.	SIGNAL	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
641	ID16M6														61		61						
642	ID16M7														62		62						
643	MITX	4					4				77	4					4						
644	ST0 (NOTE 2)										5/6												
645	ST1 (NOTE 2)										9/10												
646	ST2 (NOTE 2)										13/14												
647	ST3 (NOTE 2)										17/18												
648	ST4 (NOTE 2)										21/22												
649	ST5 (NOTE 2)										25/26												
650	ST6 (NOTE 2)										29/30												
651	ST7 (NOTE 2)										33/34												
652	ST8 (NOTE 2)										37/38												
653	ST9 (NOTE 2)										43/44												
654	ST10 (NOTE 2)										49/50												
655	ST11 (NOTE 2)										53/54												
656	ST12 (NOTE 2)										57/58												
657	ST13 (NOTE 2)										61/62												
658	ST14 (NOTE 2)										65/66												
659	ST15 (NOTE 2)										69/70												
660	ST16 (NOTE 2)								60/86		73/74												
661	STRX										42												
662	MSG			6	6									6	6								
663	MIT										81												
664	MWT2									27													
665	GND			9/1	9									9	9								

LOGIC

REF.	SIGNAL													EAU LOGIC	EAU TIMING	SHIFT LOGIC	INSTRUCTION DECODER	TIMING GENERATOR	ARITHMETIC LOGIC 0-3	ARITHMETIC LOGIC 4-7	ARITHMETIC LOGIC 8-11	ARITHMETIC LOGIC 12-15	FRONT PANEL COUPLER
REF.	SIGNAL	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101
641	ID16M6																						
642	ID16M7																						
643	MITX																						
644	ST0 (NOTE 2)																		49/1				
645	ST1 (NOTE 2)																		4/2				
646	ST2 (NOTE 2)																		52/2				
647	ST3 (NOTE 2)																		11/1				
648	ST4 (NOTE 2)																			49/1			
649	ST5 (NOTE 2)																			4/2			
650	ST6 (NOTE 2)																			52/2			
651	ST7 (NOTE 2)																			11/1			
652	ST8 (NOTE 2)																				49/1		
653	ST9 (NOTE 2)																				4/2		
654	ST10 (NOTE 2)																				52/2		
655	ST11 (NOTE 2)																				11/1		
656	ST12 (NOTE 2)																					49/1	
657	ST13 (NOTE 2)																					4/2	
658	ST14 (NOTE 2)																					52/2	
659	ST15 (NOTE 2)																					11/1	
660	ST16 (NOTE 2)																						
661	STRX																	81					
662	MSG																	19					
663	MIT																	25					
664	MWT2																	20					
665	GND																						

INPUT/OUTPUT

		I/O EXTENDER X2	I/O EXTENDER X1	27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10	I/O ADDRESS ENCODER	I/O CONTROL	
222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204	203	202	201	REF.
																						641
																						642
																						643
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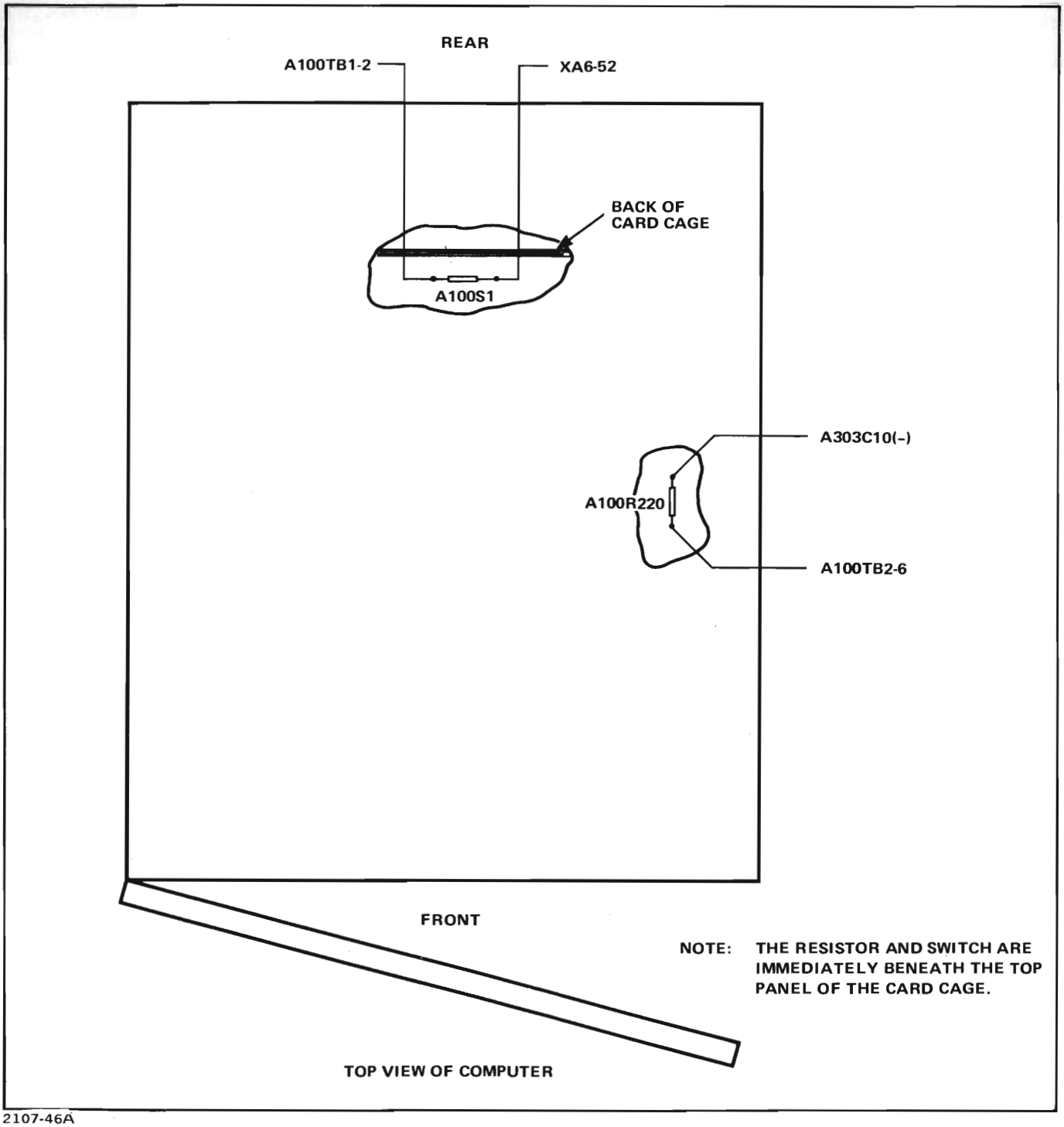
																						663
																						664
																						665

NOTES: 1. [shaded box] SHADED PIN NUMBERS INDICATES SOURCE OF SIGNAL.
2. CONNECTIONS GIVEN ARE FOR A TWISTED PAIR; TOP PIN IS SIGNAL WIRE, BOTTOM PIN IS GROUND WIRE.

Table 7-4. A100R220 Temperature Sensing Resistor and A100S1 Thermal Switch, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
A100R220	0811-2031	Resistor, Fxd, ww, 815 ohms, 3%, 1/4W	28480	0811-2031
A100S1	3103-0004	Thermal Switch	28480	3103-0004



2107-46A

Figure 7-4. A100R220 Temperature Sensing Resistor and A100S1 Thermal Switch, Parts Location and Connection Diagram

Table 7-5. A1 DMA Register Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A1-47 A1-48	None
+4.5V	A100E1	A1-39 A1-40	None
C0 (Carry Bit 0)	A108-71	A1-43	See source
CLC (Clear Control)	A108-53	A1-18	See source
CLF (Clear Flag)	A108-19 A4-14 A109-24	A1-51	See source or option
CRS (Control Reset to I/O)	A201-55	A1-9	See source
DIN1 (DMA Input FF, Channel 1)	A1-4	A4-75	See option
FLG0 (Flag from Group 0)	A203-4 thru A210-4 A203-49 thru A209-49	A1-30	See source
GND (Ground)	A100E2	A1-1 A1-2 A1-85 A1-86	None
IAK (Interrupt Acknowledge)	A201-77	A1-44	See source
IEN6 (Interrupt Enable)	A201-10	A1-35	See source
IOBI0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 · IRS + IOGE(B) · IOI · SCM0 · SCL4 · C10 FF + IOGE · IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C11 FF + IOGE · IOI · SC · DATA BIT 1

Table 7-5. A1 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	= DMA option signal + MP option signal + SWR2 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C12 FF + IOGE · IOI · SC · DATA BIT 2
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C13 FF + IOGE · IOI · SC · DATA BIT 3
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C14 FF + IOGE · IOI · SC · DATA BIT 4
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C15 FF + IOGE · IOI · SC · DATA BIT 5
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	= DMA option signal + MP option signal + SWR6 · ISR + IOGE · IOI · SC · DATA BIT 6

Table 7-5. A1 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	= DMA option signal + MP option signal + SWR7 · ISR + IOGE · IOI · SC · DATA BIT 7
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	= DMA option signal + MP option signal + SWR8 · ISR + IOGE · IOI · SC · DATA BIT 8
IOBI 9 (Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	= DMA option signal + MP option signal + SWR9 · ISR + IOGE · IOI · SC · DATA BIT 9
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	= DMA option signal + MP option signal + SWR10 · ISR + IOGE · IOI · SC · DATA BIT 10
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	= DMA option signal + MP option signal + SWR11 · ISR + IOGE · IOI · SC · DATA BIT 11
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	= DMA option signal + MP option signal + SWR12 · ISR + IOGE · IOI · SC · DATA BIT 12

Table 7-5. A1 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	= DMA option signal + MP option signal + SWR13 · ISR + IOGE · IOI · SC · DATA BIT 13
IOBI 14 (Input/Output Bus, Input Bit 14)	A1-73 A5-82 A16-76 A101-63 A203-82 thru A218-82 A220-80	A102-33	= DMA option signal + MP option signal + SWR14 ; ISR + IOGE · IOI · SC · DATA BIT 14
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60	A1-24	See source
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50	A1-26	See source
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57	A1-32	See source
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35	A1-34	See source
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60	A1-36	See source
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50	A1-42	See source
IOBO 6 (Input/Output Bus, Output Bit 6)	A104-57	A1-52	See source
IOBO 7 (Input/Output Bus, Output Bit 7)	A104-35	A1-50	See source
IOBO 8 (Input/Output Bus, Output Bit 8)	A103-60	A1-56	See source
IOBO 9 (Input/Output Bus, Output Bit 9)	A103-50	A1-62	See source
IOBO 10 (Input/Output Bus, Output Bit 10)	A103-57	A1-66	See source
IOBO 11 (Input/Output Bus, Output Bit 11)	A103-35	A1-64	See source
IOBO 12 (Input/Output Bus, Output Bit 12)	A102-60	A1-68	See source
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-50	A1-74	See source

Table 7-5. A1 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57	A1-76	See source
IOBO 15 (Input/Output Bus, Output Bit 15)	A102-35	A1-78	See source
IOGE(B) (Input/Output Instruction Group, Buffered)	A201-37	A1-11	See source
IOI (Input/Output Input)	A108-44	A1-22	See source
IOO (Input/Output Output)	A108-13	A1-8	See source
IRQ6 (Interrput Request 6)	A216-33 A217-6 A219-60 A4-28	A1-29	See option
ISZ (Increment, Skip if Zero)	A107-76	A1-69	See source
M0 (Memory Address Bit 0)	A14-6 A1-41 A2-41	A8-35 A11-35 A14-6 A18-35 A21-35	= MR0 · PH5 + DMA option signal
M1 (Memory Address Bit 1)	A14-10 A1-46 A2-46	A8-36 A11-36 A14-10 A18-36 A21-36	= MR1 · PH5 + DMA option signal
M2 (Memory Address Bit 2)	A14-14 A1-45 A2-45	A8-37 A11-37 A14-14 A18-37 A21-37	= MR2 · PH5 + DMA option signal
M3 (Memory Address Bit 3)	A14-18 A1-55 A2-55	A8-33 A11-33 A14-18 A18-33 A21-33	= MR3 · PH5 + DMA option signal
M4 (Memory Address Bit 4)	A14-22 A1-65 A2-65	A8-32 A11-32 A14-22 A18-32 A21-32	= MR4 · PH5 + DMA option signal
M5 (Memory Address Bit 5)	A14-26 A1-63 A2-63	A8-31 A11-31 A14-26 A18-31 A21-31	= MR5 · PH5 + DMA option signal

Table 7-5. A1 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
M6 (Memory Address Bit 6)	A14-30 A1-71 A2-71	A8-49 A 11-49 A14-30 A18-49 A21-49	= MR6 · PH5 + DMA option signal
M7 (Memory Address Bit 7)	A14-34 A1-72 A2-72	A8-52 A11-52 A14-34 A18-52 A21-52	= MR7 · PH5 + DMA option signal
M8 (Memory Address Bit 8)	A14-38 A1-83 A2-83	A8-51 A11-51 A14-38 A18-51 A21-51	= MR8 · PH5 + DMA option signal
M9 (Memory Address Bit 9)	A14-44 A1-82 A2-82	A8-53 A11-53 A14-44 A18-53 A21-53	= MR9 · PH5 + DMA option signal
M10 (Memory Address Bit 10)	A14-50 A1-6 A2-6	A8-56 A11-56 A14-50 A18-56 A21-56	= MR10 · PH5
M11 (Memory Address Bit 11)	A14-54 A1-10 A2-10	A8-55 A11-55 A14-54 A18-55 A21-55	= MR11 · PH5 + DMA option signal
M12 (Memory Address Bit 12)	A14-58 A1-12 A2-12	A14-58	= MR12 · PH5 + DMA option signal
M13 (Memory Address Bit 13)	A14-62 A1-16 A2-16	A14-62 A18-23	= MR13 · PH5 + DMA option signal
M14 (Memory Address Bit 14)	A14-66 A1-7 A2-7	A11-23 A 14-66	= MR14 · PH5 + DMA option signal
PH3 (Phase 3, Execute)	A106-60	A1-67	See source
PH5 (Phase 5)	A4-8	A1-70	See option
POPIO (Power On Pulse to I/O)	A106-61	A1-37	See source
PRL6 (Priority Low 6)	A201-78	A1-23	See source

Table 7-5. A1 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PRH6/PRL5 (Priority High Select Code 6/Priority Low Select Code 5)	A15-27 A16-51	A1-33 A201-76 A201-82	See option
RTSB (Read T-Register to the S-Bus)	A107-82 A110-19	A1-60	See source or option
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A1-14	See source
SCL2 (Select Code Least Significant Digit, Octal 2)	A202-61	A1-13	See source
SFS (Skip if Flag Set)	A108-54	A1-31	See source
SIR (Service Interrupt Request)	A201-35	A1-53	See source
SKF (Skip on Flag)	A201-73 A203-12 thru A220-12 A4-29	A1-15	See source or option
SMAR 1 (Step Memory Address Register, DMA Channel 1)	A4-72	A1-38	See source
STC (Set Control)	A108-56	A1-20	See option
SWCR1 (Step Word Count Register, DMA Channel 1)	A4-80	A1-3	See source
T0 (Time Period 0)	A106-28	A1-54	See option
T3(B) (Time Period 3, Buffered)	A201-81	A1-5	See source
T7 (Time Period 7)	A106-18	A1-57	See source
TSA (Time Strobe A)	A106-67	A1-59	See source
WCR1 (Word Count Rollover, DMA Channel 1)	A1-84	A4-77	See option

Table 7-6. A2 DMA Register Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A2-47 A2-48	None
+4.5V	A100E1	A2-39 A2-40	None
CLC (Clear Control)	A108-53	A2-18	See source
CRS (Control Reset to I/O)	A201-55	A2-9	See source
DIN2 (DMA Input FF, Channel 2)	A2-4	A4-74	See option
GND (Ground)	A100E2	A2-1 A2-2 A2-85 A2-86	None
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C10 FF + IOGE · IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C11 FF + IOGE · IOI · SC · DATA BIT 1
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	= DMA option signal + MP option signal + SWR2 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C12 FF + IOGE · IOI · SC · DATA BIT 2
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C13 FF + IOGE · IOI · SC · DATA BIT 3

Table 7-6. A2 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C14 FF + IOGE · IOI · SC · DATA BIT 4
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C15 FF + IOGE · IOI · SC · DATA BIT 5
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	= DMA option signal + MP option signal + SWR6 · ISR + IOGE · IOI · SC · DATA BIT 6
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	= DMA option signal + MP option signal + SWR7 · ISR + IOGE · IOI · SC · DATA BIT 7
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	= DMA option signal + MP option signal + SWR8 · ISR + IOGE · IOI · SC · DATA BIT 8
IOBI 9 (Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	= DMA option + MP option signal + SWR9 · ISR + IOGE · IOI · SC · DATA BIT 9

Table 7-6. A2 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	= DMA option signal + MP option signal + SWR10 · ISR + IOGE · IOI · SC · DATA BIT 10
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	= DMA option signal + MP option signal + SWR11 · ISR + IOGE · IOI · SC · DATA BIT 11
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	= DMA option signal + MP option signal + SWR12 · ISR + IOGE · IOI · SC · DATA BIT 12
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	= DMA option signal + MP option signal + SWR13 · ISR + IOGE · IOI · SC · DATA BIT 13
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60	A2-24	See source
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50	A2-26	See source
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57	A2-32	See source
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35	A2-34	See source
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60	A2-36	See source
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50	A2-42	See source

Table 7-6. A2 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBO 6 (Input/Output Bus, Output Bit 6)	A104-57	A2-52	See source
IOBO 7 (Input/Output Bus, Output Bit 7)	A104-35	A2-50	See source
IOBO 8 (Input/Output Bus, Output Bit 8)	A103-60	A2-56	See source
IOBO 9 (Input/Output Bus, Output Bit 9)	A103-50	A2-62	See source
IOBO 10 (Input/Output Bus, Output Bit 10)	A103-57	A2-66	See source
IOBO 11 (Input/Output Bus, Output Bit 11)	A103-35	A2-64	See source
IOBO 12 (Input/Output Bus, Output Bit 12)	A102-60	A2-68	See source
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-52	A2-74	See source
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57	A2-76	See source
IOBO 15 (Input/Output Bus, Output Bit 15)	A102-35	A2-78	See source
IOI (Input/Output, Input)	A108-44	A2-22	See source
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A2-11	See source
IOO (Input/Output, Output)	A108-13	A2-8	See source
M0 (Memory Address Bit 0)	A14-6 A1-41 A2-41	A8-35 A11-35 A14-6 A18-35 A21-35	= MR0 · PH5 + DMA option signal
M1 (Memory Address Bit 1)	A14-10 A1-46 A2-46	A8-36 A11-36 A14-10 A18-36 A21-36	= MR1 · PH5 + DMA option signal
M2 (Memory Address Bit 2)	A14-14 A1-45 A2-45	A8-37 A11-37 A14-14 A18-37 A21-37	= MR2 · PH5 + DMA option signal
M3 (Memory Address Bit 3)	A14-18 A1-55 A2-55	A8-33 A11-33 A14-18 A18-33 A21-33	= MR3 · PH5 + DMA option signal

Table 7-6. A2 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
M4 (Memory Address Bit 4)	A14-22 A1-65 A2-65	A8-32 A11-32 A14-22 A18-32 A21-32	= MR4 · PH5 + DMA option signal
M5 (Memory Address Bit 5)	A14-26 A1-63 A2-63	A8-31 A11-31 A14-26 A18-31 A21-31	= MR5 · PH5 + DMA option signal
M6 (Memory Address Bit 6)	A14-30 A1-71 A2-71	A8-49 A11-49 A14-30 A18-49 A21-49	= MR6 · PH5 + DMA option signal
M7 (Memory Address Bit 7)	A14-34 A1-72 A2-72	A8-52 A11-52 A14-34 A18-52 A21-52	= MR7 · PH5 + DMA option signal
M8 (Memory Address Bit 8)	A14-38 A1-83 A2-83	A8-51 A11-51 A14-38 A18-51 A21-51	= MR8 · PH5 + DMA option signal
M9 (Memory Address Bit 9)	A14-44 A1-82 A2-82	A8-53 A11-53 A14-44 A18-53 A21-53	= MR9 · PH5 + DMA option signal
M10 (Memory Address Bit 10)	A14-50 A1-6 A2-6	A8-56 A11-56 A14-50 A18-56 A21-56	= MR10 · PH5 + DMA option signal
M11 (Memory Address Bit 11)	A14-54 A1-10 A2-10	A8-55 A11-55 A14-54 A18-55 A21-55	= MR11 · PH5 + DMA option signal
M12 (Memory Address Bit 12)	A14-58 A1-12 A2-12	A14-58	= MR12 · PH5 + DMA option signal
M13 (Memory Address Bit 13)	A14-62 A1-16 A2-16	A14-62 A18-23	= MR13 · PH5 + DMA option signal
M14 (Memory Address Bit 14)	A14-66 A1-7 A2-7	A11-23 A14-66	= MR14 · PH5 + DMA option signal

Table 7-6. A2 DMA Register Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SCL3 (Select Code Least Significant Digit, Octal 3)	A202-63	A2-13	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A2-14	See source
SIR (Service Interrupt Request)	A201-35	A2-53	See source
SMAR2 (Step Memory Address Register, DMA Channel 2)	A4-69	A2-38	See source
STC (Set Control)	A108-56	A2-20	See source
SWCR2 (Step Word Count Register, DMA Channel 2)	A4-79	A2-3	See source
T3(B) (Time Period 3, Buffered)	A201-81	A2-5	See source
TSA (Time Strobe A)	A106-67	A2-59	See source
WCR2 (Word Count Rollover, DMA Channel 2)	A2-84	A4-76	See option

Table 7-7. A3 DMA Address Encoder Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A3-47 A3-48	None
+4.5V	A100E1	A3-39 A3-40	None
CIN (Character In, DMA)	A3-41	A4-70	See option
CM1 (Carry Bit 1) (Character Mode 1)	A3-7	A4-67	See option
CM2 (Carry Bit 2) (Character Mode 2)	A3-81	A4-68	See option
COUT (Character Out, DMA)	A3-36	A4-63	See option
CR1 (Cycle Request, DMA Channel 1)	A3-34	A4-78	See option
CR2 (Cycle Request, DMA Channel 2)	A3-27	A4-71	See option
CRS (Control Reset to I/O)	A201-65	A3-74	See source
DE-1 (not used)	A3-53	None	None
DE-2 (not used)	A3-55	None	None
ENF (Enable Flag)	A201-67	A3-49	See source
GND (Ground)	A100E2	A3-1 A3-2 A3-85 A3-86	None
HIS (Hold Interrupt System)	A3-83	A201-4	See option
IDW1 (Input Data Word from DMA Channel 1)	A3-16	A5-24	See option
IDW2 (Input Data Word from DMA Channel 2)	A3-14	A5-25	See option
IHC1 (Input High Character to DMA Channel 1)	A3-9	A5-32	See option
IHC2 (Input High Character to DMA Channel 2)	A3-8	A5-36	See option
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60	A3-21	See source

Table 7-7. A3 DMA Address Encoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50	A3-42	See source
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57	A3-65	See source
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35	A3-35	See source
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60	A3-63	See source
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50	A3-61	See source
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57	A3-15	See source
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A3-84	See source
IOI (Input/Output, Input)	A108-44	A3-11 A3-43	See source
IOO (Input/Output, Output)	A108-13	A3-30	See source
OHC1 (Output High Character from DMA Channel 1)	A3-10	A5-20	See option
OHC2 (Output High Character from DMA Channel 2)	A3-12	A5-21	See option
OLC1 (Output Low Character from DMA Channel 1)	A3-19	A5-22	See option
OLC2 (Output Low Character from DMA Channel 2)	A3-13	A5-23	See option
OUT (Output High Character, DMA)	A4-65	A3-6	See option
PH5 (Phase 5, DMA)	A4-8	A3-78	See option
PRH5/PRL4 (Priority High Select Code 5/Priority Low Select Code 4)	A6-3	A3-57	See source
SCL0 (Select Code Least Significant Digit, Octal 0)	A202-65	A3-32	See source
SCL1 (Select Code Least Significant Digit, Octal 1)	A202-67	A3-80	See source
SCL2 (Select Code Least Significant Digit, Octal 2)	A202-61	A3-18	See source

Table 7-7. A3 DMA Address Encoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SCL3 (Select Code Least Significant Digit, Octal 3)	A202-63	A3-82	See source
SCL4 (Select Code Least Significant Digit, Octal 4)	A202-51	A3-38	See source
SCL5 (Select Code Least Significant Digit, Octal 5)	A202-52	A3-79	See source
SCL6 (Select Code Least Significant Digit, Octal 6)	A202-49	A3-46	See source
SCL7 (Select Code Least Significant Digit, Octal 7)	A202-50	A3-50	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A3-51	See source
SCM1 (Select Code Most Significant Digit, Octal 1)	A202-77	A3-67	See source
SCM2 (Select Code Most Significant Digit, Octal 2)	A202-71	A3-69	See source
SIR (Service Interrupt Request)	A201-35	A3-70	See source
SRQ10 (Service Request, Select Code 10)	A203-19	A3-22	See option
SRQ11 (Service Request, Select Code 11)	A204-19	A3-28	See option
SRQ12 (Service Request, Select Code 12)	A205-19	A3-20	See option
SRQ13 (Service Request, Select Code 13)	A206-19	A3-26	See option
SRQ14 (Service Request, Select Code 14)	A207-19	A3-33	See option
SRQ15 (Service Request, Select Code 15)	A208-19	A3-44	See option
SRQ16 (Service Request, Select Code 16)	A209-19	A3-29	See option
SRQ17 (Service Request, Select Code 17)	A210-19	A3-37	See option

Table 7-7. A3 DMA Address Encoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SRQ20 (Service Request, Select Code 20)	A211-19	A3-71	See option
SRQ21 (Service Request, Select Code 21)	A212-19	A3-66	See option
SRQ22 (Service Request, Select Code 22)	A213-19	A3-68	See option
SRQ23 (Service Request, Select Code 23)	A214-19	A3-64	See option
SRQ24 (Service Request, Select Code 24)	A215-19	A3-58	See option
SRQ25 (Service Request, Select Code 25)	A216-19	A3-54	See option
SRQ26 (Service Request, Select Code 26)	A217-19	A3-56	See option
SRQ27 (Service Request, Select Code 27)	A218-19	A3-52	See option
STC (Set Control)	A108-56	A3-17	See source
T4T5 (Time Periods 4 and 5)	A106-16	A3-31	See source
T6T7 (Time Periods 6 and 7)	A106-30	A3-73	See source
TE1 (Transfer Enable FF, DMA Channel 1)	A4-66	A3-60	See option
TE2 (Transfer Enable FF, DMA Channel 2)	A4-62	A3-62	See option
TSA (Time Strobe A)	A106-67	A3-45	See source

Table 7-8. A4 DMA Control Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A4-47 A4-48	None
+4.5V	A100E1	A4-39 A4-40	None
ADF (Add Function)	A107-75 A110-12 A4-82	A102-5 A103-5 A104-5 A105-5	See source or option
CIN (Character In, DMA)	A3-41	A4-70	See option
CLC (Clear Control)	A108-53	A4-60	See source
CLF (Clear Flag)	A108-19 A4-14 A109-24	A1-51 A6-7 A15-51 A201-51 A203-7 thru A220-7	See source or option
CM1 (Character Mode 1)	A3-7	A4-67	See option
CM2 (Character Mode 2)	A3-81	A4-68	See option
COUT (Character Out, DMA)	A3-36	A4-63	See option
CR1 (Cycle Request, DMA Channel 1)	A3-34	A4-78	See option
CR2 (Cycle Request, DMA Channel 2)	A3-27	A4-71	See option
CRS (Control Reset to I/O)	A201-65	A4-32	See source
DIN1 (DMA Input FF, Channel 1)	A1-4	A4-75	See option
DIN2 (DMA Input FF, Channel 2)	A2-4	A4-74	See option
EDT (End of Data Transfer)	A4-42	A203-62 thru A218-62 A219-3	See option
ENF (Enable Flag)	A201-67	A4-37	See source
FLG 0 (Flag from Group 0)	A203-4 thru A210-4 A203-49 thru A209-49	A4-25	See option

Table 7-8. A4 DMA Control Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
GND (Ground)	A100E2	A4-1 A4-2 A4-85 A4-86	None
IAK (Interrupt Acknowledge)	A201-77	A4-27	See source
IEN6 (Interrupt Enable)	A201-10	A4-7	See source
IN (not used, DMA)	A4-52	None	See option
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-50	A4-54	See source
IOBO 15 (Input/Output Bus, Output Bit 15)	A102-35	A4-51	See source
IODO (I/O Data Out, DMA)	A4-4	A5-19	See option
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A4-22	See source
IOI (Input/Output, Input)	A108-44	A4-81 A4-84	See source
IOO (Input/Output, Output)	A108-13	A4-56	See source
IRQ6 (Interrupt Request 6)	A216-33 A217-6 A219-60 A4-28	A1-29 A202-25	See option
IRQ7 (Interrupt Request 7)	A217-33 A218-6 A219-62 A4-26	A202-19	See option
ISG (Inhibit Strobe Generator, EAU)	A109-63 A4-3	A106-4	See option
OUT (Output High Character, DMA)	A4-65	A3-6	See option
PH5 (Phase 5, DMA)	A4-8	A1-70 A3-78 A13-84 A14-69 A15-8 A16-7 A109-53 A201-17	See option
$\overline{\text{PH5}}$ (not used, DMA)	A4-5	None	See option
POPIO(B) (Power On Pulse to I/O, Buffered)	A201-72	A4-35	See source

Table 7-8. A4 DMA Control Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PRL6 (Priority Low 6)	A201-78	A4-31	See source
PRH10/PRL7 (Priority High Select Code 10/Priority Low Select Code 7)	A4-9 A201-80	A201-12 A201-14 A203-23	See option
SCL6 (Select Code Least Significant Digit, Octal 6)	A202-49	A4-36	See source
SCL7 (Select Code Least Significant Digit, Octal 7)	A202-50	A4-38	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A4-18	See source
SFC (Skip if Flag Clear)	A108-14	A4-24	See source
SFS (Skip if Flag Set)	A108-54	A4-20	See source
SIR (Service Interrupt Request)	A201-35	A4-34	See source
SKF (Skip On Flag)	A201-73 A203-12 thru A220-12 A4-29	A1-15 A6-12 A108-31	See source or option
SMAR1 (Step Memory Address Register, DMA Channel 1)	A4-72	A1-38	See option
SMAR2 (Step Memory Address Register, DMA Channel 2)	A4-69	A2-38	See option
STC (Set Control)	A108-56	A4-58	See source
STF (Set Flag)	A108-5 A109-15	A4-16	See source or option
SWCR1 (Step Word Count Register, DMA Channel 1)	A4-80	A1-3	See option
SWCR2 (Step Word Count Register, DMA Channel 2)	A4-79	A2-3	See option
SWST (Switch Store in T-Register)	A106-62 A4-83	A107-34 A110-20	See source or option
T3T4 (Time Periods 3 and 4)	A106-15	A4-30	See source

Table 7-8. A4 DMA Control Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
T4T5 (Time Periods 4 and 5)	A106-16	A4-6	See source
T7 (Time Period 7)	A106-18	A4-64	See source
T7S (Time Period 7 with Strobe)	A106-51	A4-10	See source
TE1 (Transfer Enable FF, DMA Channel 1)	A4-66	A3-60	See option
TE2 (Transfer Enable FF, DMA Channel 2)	A4-62	A3-62	See option
WCR1 (Word Count Roll-over, DMA Channel 1)	A1-84	A4-77	See option
WCR2 (Word Count Roll-over, DMA Channel 2)	A2-84	A4-76	See option

Table 7-9. A5 DMA Character Packer Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A5-47 A5-48	None
+4.5V	A100E1	A5-39 A5-40	None
GND (Ground)	A100E2	A5-1 A5-2 A5-85 A5-86	None
IDW1 (Input Data Word from DMA Channel 1)	A3-16	A5-24	See option
IDW2 (Input Data Word from DMA Channel 2)	A3-14	A5-25	See option
IHC1 (Input High Character to DMA Channel 1)	A3-9	A5-32	See option
IHC2 (Input High Character to DMA Channel 2)	A3-8	A5-36	See option
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 · ISR + IOGE(B) · IOI · SCM0 · SCL14 · C10 FF + IOGE · IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C11 FF + IOGE · IOI · SC · DATA BIT 1
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	= DMA option signal + MP option signal + SWR2 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C12 FF + IOGE · IOI · SC · DATA BIT 2

Table 7-9. A5 DMA Character Packer Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C13 FF + IOGE · IOI · SC · DATA BIT 3
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C14 FF + IOGE · IOI · SC · DATA BIT 4
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C15 FF + IOGE · IOI · SC · DATA BIT 5
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	= DMA option signal + MP option signal + SWR6 · ISR + IOGE · IOI · SC · DATA BIT 6
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	= DMA option signal + MP option signal + SWR7 · ISR + IOGE · IOI · SC · DATA BIT 7
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	= DMA option signal + MP option signal + SWR8 · ISR + IOGE · IOI · SC · DATA BIT 8

Table 7-9. A5 DMA Character Packer Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 9 (Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	= DMA option signal + MP option signal + SWR9 · ISR + IOGE · IOI · SC · DATA BIT 9
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	= DMA option signal + MP option signal + SWR10 · ISR + IOGE · IOI · SC · DATA BIT 10
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	= DMA option signal + MP option signal + SWR11 · ISR + IOGE · IOI · SC · DATA BIT 11
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	= DMA option signal + MP option signal + SWR12 · ISR + IOGE · IOI · SC · DATA BIT 12
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	= DMA option signal + MP option signal + SWR13 · ISR + IOGE · IOI · SC · DATA BIT 13
IOBI 14 (Input/Output Bus, Input Bit 14)	A1-73 A5-82 A16-76 A101-63 A203-82 thru A218-82 A220-80	A102-33	= DMA option signal + MP option signal + SWR14 · ISR + IOGE · IOI · SC · DATA BIT 14

Table 7-9. A5 DMA Character Packer Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 15 (Input/Output Bus, Input Bit 15)	A5-83 A15-28 A101-67 A203-83 thru A218-83 A220-82	A102-27	= DMA option signal + PE option signal + SWR15 · ISR + IOGE · IOI · SC · DATA BIT 15
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60 A5-35	A5-35	See source or option
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50 A5-38	A5-38	See source or option
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57 A5-41	A5-41	See source or option
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35 A5-45	A5-45	See source or option
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60 A5-42	A5-42	See source or option
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50 A5-51	A5-51	See source or option
IOBO 6 (Input/Output Bus, Output Bit 6)	A104-57 A5-53	A5-53	See source or option
IOBO 7 (Input/Output Bus, Output Bit 7)	A104-35 A5-52	A5-52	See source or option
IOBO 8 (Input/Output Bus, Output Bit 8)	A103-60 A5-54	A5-54	See source or option
IOBO 9 (Input/Output Bus, Output Bit 9)	A103-50 A5-56	A5-56	See source or option
IOBO 10 (Input/Output Bus, Output Bit 10)	A103-57 A5-58	A5-58	See source or option
IOBO 11 (Input/Output Bus, Output Bit 11)	A103-35 A5-55	A5-55	See source or option
IOBO 12 (Input/Output Bus, Output Bit 12)	A102-60 A5-57	A5-57	See source or option
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-50 A5-61	A5-61	See source or option
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57 A5-65	A5-65	See source or option
IOBO 15 (Input/Output Bus, Output Bit 15)	A102-35 A5-74	A5-74	See source or option
IODO (I/O Data Out, DMA)	A4-4	A5-19	See source or option

Table 7-9. A5 DMA Character Packer Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
OHC1 (Output High Character from DMA Channel 1)	A3-10	A5-20	See option
OHC2 (Output High Character from DMA Channel 2)	A3-12	A5-21	See option
OLC1 (Output Low Character from DMA Channel 1)	A3-19	A5-22	See option
OLC2 (Output Low Character from DMA Channel 2)	A3-13	A5-23	See option
TR0 (T-Register Bit 0)	A105-58	A5-3	See source
TR1 (T-Register Bit 1)	A105-9	A5-5	See source
TR2 (T-Register Bit 2)	A105-56	A5-7	See source
TR3 (T-Register Bit 3)	A105-16	A5-9	See source
TR4 (T-Register Bit 4)	A104-58	A5-11	See source
TR5 (T-Register Bit 5)	A104-9	A5-13	See source
TR6 (T-Register Bit 6)	A104-56	A5-15	See source
TR7 (T-Register Bit 7)	A104-16	A5-17	See source
TR8 (T-Register Bit 8)	A103-58	A5-34	See source
TR9 (T-Register Bit 9)	A103-9	A5-43	See source
TR10 (T-Register Bit 10)	A103-56	A5-46	See source
TR11 (T-Register Bit 11)	A103-16	A5-50	See source
TR12 (T-Register Bit 12)	A102-58	A5-62	See source
TR13 (T-Register Bit 13)	A102-9	A5-66	See source
TR14 (T-Register Bit 14)	A102-56	A5-68	See source
TR15 (T-Register Bit 16)	A102-16	A5-70	See source
TR0(B) (T-Register Bit 0, DMA Buffered)	A5-4	None	See option
TR1(B) (T-Register Bit 1, DMA Buffered)	A5-6	None	See option
TR2(B) (T-Register Bit 2, DMA Buffered)	A5-8	None	See option
TR3(B) (T-Register Bit 3, DMA Buffered)	A5-10	None	See option
TR4(B) (T-Register Bit 4, DMA Buffered)	A5-12	None	See option

Table 7-9. A5 DMA Character Packer Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TR5(B) (T-Register Bit 5, DMA Buffered)	A5-14	None	See option
TR6(B) (T-Register Bit 6, DMA Buffered)	A5-16	None	See option
TR7(B) (T-Register Bit 7, DMA Buffered)	A5-18	None	See option
TR8(B) (T-Register Bit 8, DMA Buffered)	A5-33	None	See option
TR9(B) (T-Register Bit 9, DMA Buffered)	A5-37	None	See option
TR10(B) (T-Register Bit 10, DMA Buffered)	A5-44	None	See option
TR11(B) (T-Register Bit 11, DMA Buffered)	A5-49	None	See option
TR12(B) (T-Register Bit 12, DMA Buffered)	A5-59	None	See option
TR13(B) (T-Register Bit 13, DMA Buffered)	A5-63	None	See option
TR14(B) (T-Register Bit 14, DMA Buffered)	A5-67	None	See option
TR15(B) (T-Register Bit 15, DMA Buffered)	A5-69	None	See option

Table 7-10. A6 Power Fail Interrupt Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A6-47 A6-48	None
+4.5V	A100E1	A6-39 A6-40	None
-5.6V	A100TB1-5	A6-75	None
+12V	A100TB2-1	A6-43 A6-44	None
-12V	A100TB2-2	A6-69 A6-70	None
18V ac	A100TB1-4	A6-80	None
18V ac	A100TB1-3	A6-79	None
+20V	A100TB2-3	A6-31	None
-20V	A100TB2-4	A6-33	None
+32V	A100TB2-7	A6-29	None
CLC (Clear Control)	A108-53	A6-21	See source
CLF (Clear Flag)	A4-14 A108-19 A109-24	A6-7	See source or option
ENF (Enable Flag)	A201-67	A6-46	See source
EPF (Extender Power Fail)	A300J2-3	A6-42	See option
EPO (Extender Power On)	A300J2-4	A6-37	See option
FLAG BUFFER FF			Set = 18V ac · $\overline{\text{FLAG FF}}$ · $\overline{\text{IAK}}$ · $\overline{\text{PRS}}$ + 18V ac · FLAG FF · $\overline{\text{IAK}}$ · 4.5V + 18V ac · $\overline{\text{FLAG FF}}$ · $\overline{\text{IRQ FF}}$ · $\overline{\text{PRS}}$ + 18V ac · FLAG FF · $\overline{\text{IRQ FF}}$ · 4.5V + EXTENDER POWER FAIL · $\overline{\text{FLAG FF}}$ · $\overline{\text{IAK}}$ · $\overline{\text{PRS}}$ + EXTENDER POWER FAIL · FLAG FF · IAK · 4.5V + EXTENDER POWER FAIL · $\overline{\text{FLAG FF}}$ · $\overline{\text{IRQ}}$ · $\overline{\text{PRS}}$ + EXTENDER POWER FAIL · FLAG FF · $\overline{\text{IRQ}}$ · 4.5V Clear = IAK · IRQ FF · $\overline{\text{18V ac}}$ · $\overline{\text{EXTENDER POWER FAIL}}$ + IAK · IRQ FF · FLAG FF + PRS · 4.5V · $\overline{\text{18V ac}}$ · $\overline{\text{EXTENDER POWER FAIL}}$ + PRS · 4.5V · FLAG FF

Table 7-10. A6 Power Fail Interrupt Card, Signal List (Continued)

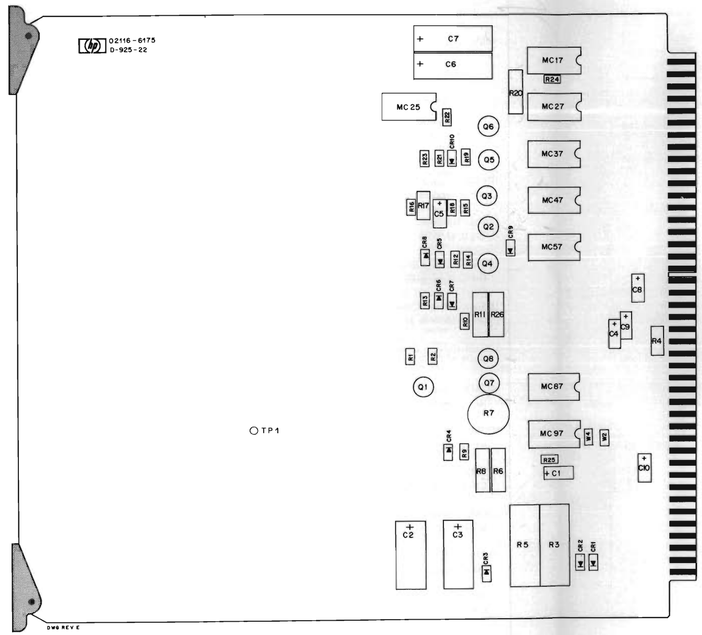
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
FLAG FF			Set = ENF · FLAG BUFFER FF · $\overline{PRS}$ + $\overline{(4.5V)}$ · $\overline{PRS}$ + $\overline{(-2V)}$ · $\overline{PRS}$ Clear = PRS · $\overline{ENF}$ · (+4.5) · (-2V) + PRS · $\overline{FLAG\ BUFFER\ FF}$ · (+4.5V) · (-2V)
GND (Ground)	A100E2	A6-1 A6-2 A6-85 A6-86	None
HLS (Halt Switch Output)	A101-54	A6-72	None
IAK (Interrupt Acknowledge)	A201-77	A6-10	See source
INT (Interrupt)	A6-28 A15-79 A16-31 A202-3	A106-44	See source or option
IOG (Input/Output Instruction Group)	A107-6	A6-38	See source
IOGE (Input/Output Instruction Group, Buffered)	A6-59 A16-19	A108-16 A201-33	= IOG · MPC + MP option
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A6-15	See source
$\overline{IR15}$ ("not" Instruction Register Bit 15)	A16-33 A107-42	A6-4	See source or option
IRQ FF (Interrupt Request FF)			Set = FLAG BUFFER FF · FLAG FF · SIR · $\overline{ENF}$ Clear = ENF · $\overline{FLAG\ BUFFER\ FF}$ + ENF · $\overline{SIR}$ + ENF · $\overline{FLAG\ FF}$
IRQ4 (Interrupt Request 4)	A6-6 A215-6 A219-56	A202-27 A214-33	None
MPC (Memory Protect Control)	A16-25	A6-36	See option
P IND (Power Indicator Lamp)	A6-49	A101-75	+12V
POFP (Power On/Off Pulse)	A6-56	A101-10 A106-77	None
PON (Power On Normal)	A6-58	A8-42 A11-42 A18-42 A21-42 A101-71 A203-66 thru A218-66 A219-41	+4.5V · -2V

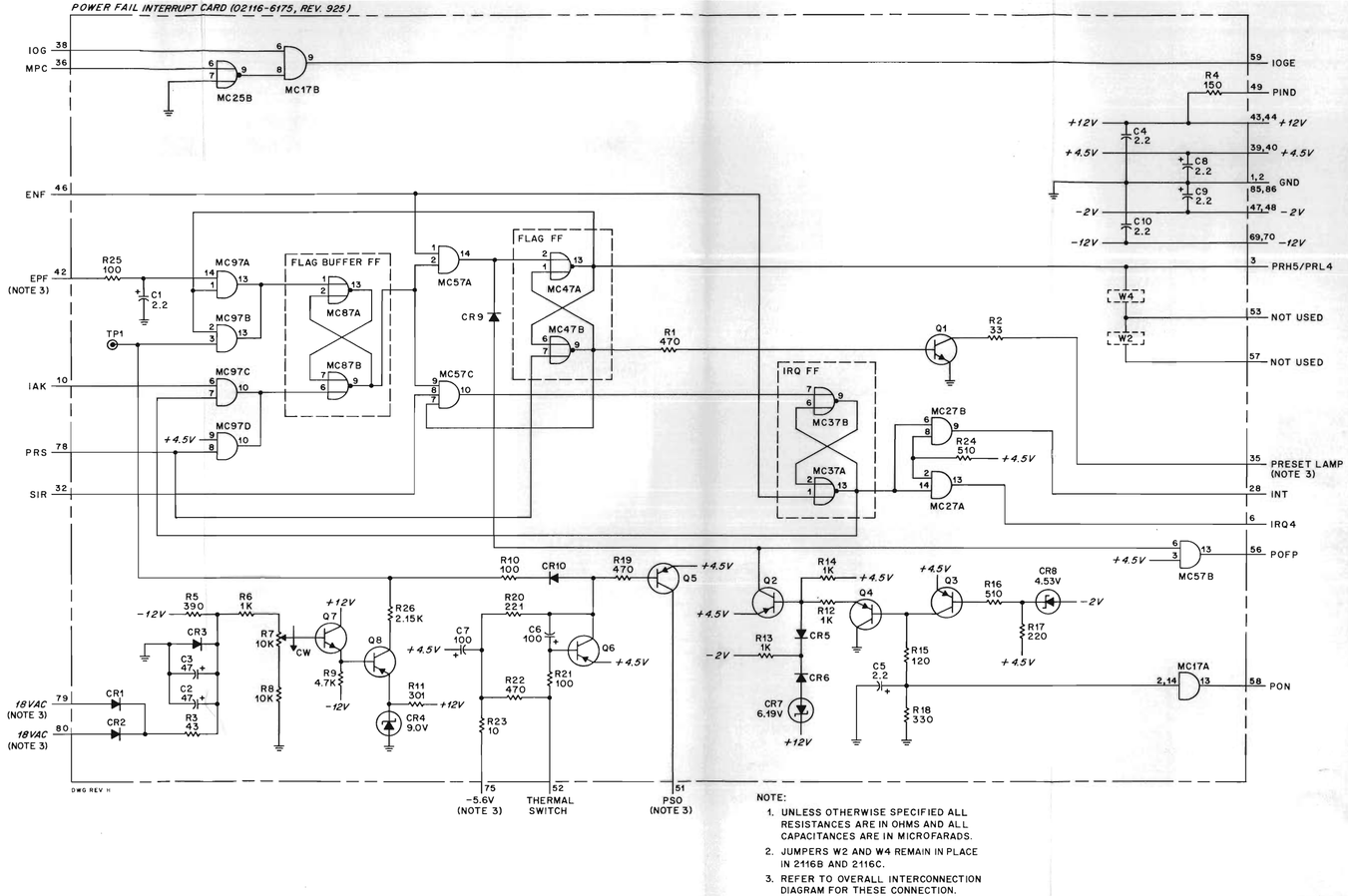
Table 7-10. A6 Power Fail Interrupt Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
PRESET LAMP	A6-35	A200TB1-3	Flag FF, set-side output
PRH5/PRL4 (Priority High Select Code 5/Priority Low Select Code 4)	A6-3	A3-57 A15-25 A16-38 A201-84	Flag FF, set-side output
PRS (Preset Switch Output, Gated)	A101-30	A6-78	See source
PSO (Power Supply On)	A6-51	A100TB1-1	= (+4.5V) · (18V ac) · (-12V) · (+12V) · (-5.6V)
$\overline{RF2}$ ("not" Run FF 2)	A106-58	A6-62	See source
RNS (Run Switch FF)	A101-44	A6-60	See source
SCL4 (Select Code Least Significant Digit, Octal 4)	A202-51	A6-16	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A6-14	See source
SFC (Skip If Flag Clear Instruction)	A108-14	A6-5	See source
SIR (Service Interrupt Request)	A201-35	A6-32	See source
SKF (Skip On Flag)	A4-29 A201-73 A203-12 thru A220-12	A6-12	See source or option
STC (Set Control)	A108-56	A6-22	See source
THERMAL SWITCH	A000S1	A6-52	None

Table 7-11. A6 Power Fail Interrupt Card (02116-6175), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,4,5,C8 thru C10	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	56289	150D225X0020A2
C2,3	0180-0097	Capacitor, Fxd, Elect, 47 uF, 10%, 35 VDCW	28480	0180-0097
C6,7	0180-0094	Capacitor, Fxd, Elect, 100 uF, 25 VDCW	56289	30D107G025DH4
CR1,2	1901-0191	Diode, Si, 100 PIV, 0.75A	28480	1901-0191
CR3,5,6	1901-0025	Diode, Si, 100 WV, 100 mA	28480	1901-0025
CR4	1902-0071	Diode, Breakdown, 9.0V, 5%	28480	1902-0071
CR7	1902-0551	Diode, Breakdown, 6.19V, 5%	28480	1902-0551
CR8	1902-3079	Diode, Breakdown, Si, 4.53V	28480	1902-3079
CR9,10	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG 1088
MC17,27	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC25,37,47,87	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC57	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC97	1820-0971	Integrated Circuit, CTL	07263	SL3467
Q1	1854-0246	Transistor, Si, NPN	07263	2N3643
Q2 thru Q6,8	1853-0036	Transistor, Si, PNP	04713	SP3612
Q7	1854-0215	Transistor, Si, NPN	28480	1854-0215
R1,19,22	0698-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715
R2	0683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4W	01121	CB3305
R3	0811-2084	Resistor, Fxd, ww, 43 ohms, 1%, 5W	28480	0811-2084
R4	0686-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/2W	01121	EB1515
R5	0811-0003	Resistor, Fxd, ww, 390 ohms, 1%, 1/4W	28480	0811-0003
R6	0757-0159	Resistor, Fxd, Flm, 1000 ohms, 1%, 1/2W	28480	0757-0159
R7	2100-1776	Resistor, Var, ww, 10k, 10%, 1/2W	28480	2100-1776
R8	0757-0839	Resistor, Fxd, Flm, 10k, 1%, 1/2W	28480	0757-0839
R9	0683-4725	Resistor, Fxd, Comp, 4700 ohms, 5%, 1/4W	01121	CB4725
R10,21,25	0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4W	01121	CB1015
R11	0757-0808	Resistor, Fxd, Flm, 301 ohms, 1%, 1/4W	28480	0757-0808
R12 thru R14	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R15	0683-1215	Resistor, Fxd, Comp, 120 ohms, 5%, 1/4W	01121	CB1215
R16,24	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4W	01121	CB5115
R17	0686-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/2W	28480	0686-2215
R18	0683-3315	Resistor, Fxd, Comp, 330 ohms, 5%, 1/4W	01121	CB3315
R20	0757-0805	Resistor, Fxd, Flm, 221 ohms, 1%, 1/2W	28480	0757-0805
R23	0683-1005	Resistor, Fxd, Comp, 10 ohms, 5%, 1/2W	01121	CB1005
R26	0698-3408	Resistor, Fxd, Flm, 2.15k, 1%, 1/2W	28480	0698-3408
W2,4	8159-0005	Jumper Wire	28480	8159-0005





NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
2. JUMPERS W2 AND W4 REMAIN IN PLACE IN 2116B AND 2116C.
3. REFER TO OVERALL INTERCONNECTION DIAGRAM FOR THESE CONNECTION.

Figure 7-5. A6 Power Fail Interrupt Card (02116-6175), Parts Location and Schematic Diagram

Table 7-12. A7 Inhibit Driver Card (Module 6/7, 60000-77777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A7-47 A7-48	None
+4.5V	A100E1	A7-39 A7-40	None
+20V	A100TB2-3	A7-15 A7-16 A7-71 A7-72	None
GND (Ground)	A100E2	A7-1 A7-2 A7-85 A7-86	None
ID0M6 (Inhibit Driver, Bit 0, Module 6)	A7-25	A9-25	= MIT · $\overline{TR0}$ · MOD6
ID0M7 (Inhibit Driver, Bit 0, Module 7)	A7-26	A9-26	= MIT · $\overline{TR0}$ · MOD7
ID1M6 (Inhibit Driver, Bit 1, Module 6)	A7-27	A9-27	= MIT · $\overline{TR1}$ · MOD6
ID1M7 (Inhibit Driver, Bit 1, Module 7)	A7-28	A9-28	= MIT · $\overline{TR1}$ · MOD7
ID2M6 (Inhibit Driver, Bit 2, Module 6)	A7-29	A9-29	= MIT · $\overline{TR2}$ · MOD6
ID2M7 (Inhibit Driver, Bit 2, Module 7)	A7-30	A9-30	= MIT · $\overline{TR2}$ · MOD7
ID3M6 (Inhibit Driver, Bit 3, Module 6)	A7-31	A9-31	= MIT · $\overline{TR3}$ · MOD6
ID3M7 (Inhibit Driver, Bit 3, Module 7)	A7-32	A9-32	= MIT · $\overline{TR3}$ · MOD7
ID4M6 (Inhibit Driver, Bit 4, Module 6)	A7-33	A9-33	= MIT · $\overline{TR4}$ · MOD6
ID4M7 (Inhibit Driver, Bit 4, Module 7)	A7-34	A9-34	= MIT · $\overline{TR4}$ · MOD7
ID5M6 (Inhibit Driver, Bit 5, Module 6)	A7-35	A9-35	= MIT · $\overline{TR5}$ · MOD6
ID5M7 (Inhibit Driver, Bit 5, Module 7)	A7-36	A9-36	= MIT · $\overline{TR6}$ · MOD7
ID6M6 (Inhibit Driver, Bit 5, Module 6)	A7-37	A9-37	= MIT · $\overline{TR5}$ · MOD6
ID6M7 (Inhibit Driver, Bit 6, Module 7)	A7-38	A9-38	= MIT · $\overline{TR5}$ · MOD7

Table 7-12. A7 Inhibit Driver Card (Module 6/7, 60000-77777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID7M6 (Inhibit Driver, Bit 7, Module 6)	A7-41	A9-41	= MIT · $\overline{TR7}$ · MOD6
ID7M7 (Inhibit Driver, Bit 7, Module 7)	A7-42	A9-42	= MIT · $\overline{TR7}$ · MOD7
ID8M6 (Inhibit Driver, Bit 8, Module 6)	A7-43	A9-43	= MIT · $\overline{TR8}$ · MOD6
ID8M7 (Inhibit Driver, Bit 8, Module 7)	A7-44	A9-44	= MIT · $\overline{TR8}$ · MOD7
ID9M6 (Inhibit Driver, Bit 9, Module 6)	A7-45	A9-45	= MIT · $\overline{TR9}$ · MOD6
ID9M7 (Inhibit Driver, Bit 9, Module 7)	A7-46	A9-46	= MIT · $\overline{TR9}$ · MOD7
ID10M6 (Inhibit Driver, Bit 10, Module 6)	A7-49	A9-49	= MIT · $\overline{TR10}$ · MOD6
ID10M7 (Inhibit Driver, Bit 10, Module 7)	A7-50	A9-50	= MIT · $\overline{TR10}$ · MOD7
ID11M6 (Inhibit Driver, Bit 11, Module 6)	A7-51	A9-51	= MIT · $\overline{TR11}$ · MOD6
ID11M7 (Inhibit Driver, Bit 11, Module 7)	A7-52	A9-52	= MIT · $\overline{TR11}$ · MOD7
ID12M6 (Inhibit Driver, Bit 12, Module 6)	A7-53	A9-53	= MIT · $\overline{TR12}$ · MOD6
ID12M7 (Inhibit Driver, Bit 12, Module 7)	A7-54	A9-54	= MIT · $\overline{TR12}$ · MOD7
ID13M6 (Inhibit Driver, Bit 13, Module 6)	A7-55	A9-55	= MIT · $\overline{TR13}$ · MOD6
ID13M7 (Inhibit Driver, Bit 13, Module 7)	A7-56	A9-56	= MIT · $\overline{TR13}$ · MOD7
ID14M6 (Inhibit Driver, Bit 14, Module 6)	A7-57	A9-57	= MIT · $\overline{TR14}$ · MOD6
ID14M7 (Inhibit Driver, Bit 14, Module 7)	A7-58	A9-58	= MIT · $\overline{TR14}$ · MOD7
ID15M6 (Inhibit Driver, Bit 15, Module 6)	A7-59	A9-59	= MIT · $\overline{TR15}$ · MOD6
ID15M7 (Inhibit Driver, Bit 15, Module 7)	A7-60	A9-60	= MIT · $\overline{TR15}$ · MOD7
ID16M6 (Inhibit Driver, Bit 16, Module 6)	A7-61	A9-61	= MIT · $\overline{TR16}$ · MOD6
ID16M7 (Inhibit Driver, Bit 16, Module 7)	A7-62	A9-62	= MIT · $\overline{TR16}$ · MOD7

Table 7-12. A7 Inhibit Driver Card (Module 6/7, 60000-77777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
MWTX/MITX (Memory Write Time Excludable/Memory Inhibit Time Excludable)	A13-77	A7-4	See source
MOD6 (Module 6)	A14-63	A7-6	See source
MOD7 (Module 7)	A14-5	A7-12	See source
$\overline{\text{TR0}}$ ("not" T-Register Bit 0)	A105-54	A7-5	See source
$\overline{\text{TR1}}$ ("not" T-Register Bit 1)	A105-10	A7-11	See source
$\overline{\text{TR2}}$ ("not" T-Register Bit 2)	A105-53	A7-13	See source
$\overline{\text{TR3}}$ ("not" T-Register Bit 3)	A105-15	A7-83	See source
$\overline{\text{TR4}}$ ("not" T-Register Bit 4)	A104-54	A7-81	See source
$\overline{\text{TR5}}$ ("not" T-Register Bit 5)	A104-10	A7-77	See source
$\overline{\text{TR6}}$ ("not" T-Register Bit 6)	A104-53	A7-79	See source
$\overline{\text{TR7}}$ ("not" T-Register Bit 7)	A104-15	A7-73	See source
$\overline{\text{TR8}}$ ("not" T-Register Bit 8)	A103-54	A7-75	See source
$\overline{\text{TR9}}$ ("not" T-Register Bit 9)	A103-10	A7-76	See source
$\overline{\text{TR10}}$ ("not" T-Register Bit 10)	A103-53	A7-74	See source
$\overline{\text{TR11}}$ ("not" T-Register Bit 11)	A103-15	A7-80	See source
$\overline{\text{TR12}}$ ("not" T-Register Bit 12)	A102-54	A7-78	See source
$\overline{\text{TR13}}$ ("not" T-Register Bit 13)	A102-10	A7-84	See source
$\overline{\text{TR14}}$ ("not" T-Register Bit 14)	A102-53	A7-82	See source
$\overline{\text{TR15}}$ ("not" T-Register Bit 15)	A102-15	A7-9	See source
$\overline{\text{TR16}}$ ("not" T-Register Bit 16)	A15-53	A7-7	See option

Table 7-13. A12 Inhibit Driver Card (Module 4/5, 40000-57777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A12-47 A12-48	None
+4.5V	A100E1	A12-39 A12-40	None
+20V	A100TB2-3	A12-15 A12-16 A12-71 A12-72	None
GND (Ground)	A100E2	A12-1 A12-2 A12-85 A12-86	None
ID0M4 (Inhibit Driver, Bit 0, Module 4)	A12-25	A10-25	= MIT · $\overline{TR0}$ · MOD4
ID0M5 (Inhibit Driver, Bit 0, Module 5)	A12-26	A10-26	= MIT · $\overline{TR0}$ · MOD5
ID1M4 (Inhibit Driver, Bit 1, Module 4)	A12-27	A10-27	= MIT · $\overline{TR1}$ · MOD4
ID1M5 (Inhibit Driver, Bit 1, Module 5)	A12-28	A10-28	= MIT · $\overline{TR1}$ · MOD5
ID2M4 (Inhibit Driver, Bit 2, Module 4)	A12-29	A10-29	= MIT · $\overline{TR2}$ · MOD4
ID2M5 (Inhibit Driver, Bit 2, Module 5)	A12-30	A10-30	= MIT · $\overline{TR2}$ · MOD5
ID3M4 (Inhibit Driver, Bit 3, Module 4)	A12-31	A10-31	= MIT · $\overline{TR3}$ · MOD4
ID3M5 (Inhibit Driver, Bit 3, Module 5)	A12-32	A10-32	= MIT · $\overline{TR3}$ · MOD5
ID4M4 (Inhibit Driver, Bit 4, Module 4)	A12-33	A10-33	= MIT · $\overline{TR4}$ · MOD4
ID4M5 (Inhibit Driver, Bit 4, Module 5)	A12-34	A10-34	= MIT · $\overline{TR4}$ · MOD5
ID5M4 (Inhibit Driver, Bit 5, Module 4)	A12-35	A10-35	= MIT · $\overline{TR5}$ · MOD4
ID5M5 (Inhibit Driver, Bit 5, Module 5)	A12-36	A10-36	= MIT · $\overline{TR5}$ · MOD5
ID6M4 (Inhibit Driver, Bit 6, Module 4)	A12-37	A10-37	= MIT · $\overline{TR6}$ · MOD4
ID6M5 (Inhibit Driver, Bit 6, Module 5)	A12-38	A10-38	= MIT · $\overline{TR6}$ · MOD5

Table 7-13. A12 Inhibit Driver Card (Module 4/5, 40000-57777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID7M4 (Inhibit Driver, Bit 7, Module 4)	A12-41	A10-41	= MIT · $\overline{TR7}$ · MOD4
ID7M5 (Inhibit Driver, Bit 7, Module 5)	A12-42	A10-42	= MIT · $\overline{TR7}$ · MOD5
ID8M4 (Inhibit Driver, Bit 8, Module 4)	A12-43	A10-43	= MIT · $\overline{TR8}$ · MOD4
ID8M5 (Inhibit Driver, Bit 8, Module 5)	A12-44	A10-44	= MIT · $\overline{TR8}$ · MOD5
ID9M4 (Inhibit Driver, Bit 9, Module 4)	A12-45	A10-45	= MIT · $\overline{TR9}$ · MOD4
ID9M5 (Inhibit Driver, Bit 9, Module 5)	A12-46	A10-46	= MIT · $\overline{TR9}$ · MOD5
ID10M4 (Inhibit Driver, Bit 10, Module 4)	A12-49	A10-49	= MIT · $\overline{TR10}$ · MOD4
ID10M5 (Inhibit Driver, Bit 10, Module 5)	A12-50	A10-50	= MIT · $\overline{TR10}$ · MOD5
ID11M4 (Inhibit Driver, Bit 11, Module 4)	A12-51	A10-51	= MIT · $\overline{TR11}$ · MOD4
ID11M5 (Inhibit Driver, Bit 11, Module 5)	A12-52	A10-52	= MIT · $\overline{TR11}$ · MOD5
ID12M4 (Inhibit Driver, Bit 12, Module 4)	A12-53	A10-53	= MIT · $\overline{TR12}$ · MOD4
ID12M5 (Inhibit Driver, Bit 12, Module 5)	A12-54	A10-54	= MIT · $\overline{TR12}$ · MOD5
ID13M4 (Inhibit Driver, Bit 13, Module 4)	A12-55	A10-55	= MIT · $\overline{TR13}$ · MOD4
ID13M5 (Inhibit Driver, Bit 13, Module 5)	A12-56	A10-56	= MIT · $\overline{TR13}$ · MOD5
ID14M4 (Inhibit Driver, Bit 14, Module 4)	A12-57	A10-57	= MIT · $\overline{TR14}$ · MOD4
ID14M5 (Inhibit Driver, Bit 14, Module 5)	A12-58	A10-58	= MIT · $\overline{TR14}$ · MOD5
ID15M4 (Inhibit Driver, Bit 15, Module 4)	A12-59	A10-59	= MIT · $\overline{TR15}$ · MOD4
ID15M5 (Inhibit Driver, Bit 15, Module 5)	A12-60	A10-60	= MIT · $\overline{TR15}$ · MOD5
ID16M4 (Inhibit Driver, Bit 16, Module 4)	A12-61	A10-61	= MIT · $\overline{TR16}$ · MOD4
ID16M5 (Inhibit Driver, Bit 16, Module 5)	A12-62	A10-62	= MIT · $\overline{TR16}$ · MOD5

Table 7-13. A12 Inhibit Driver Card (Module 4/5, 40000-57777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
MITX (Memory Inhibit Time Excludable)	A13-77	A12-4	See source
MOD4 (Module 4)	A14-5	A12-6	See source
MOD5 (Module 5)	A14-59	A12-12	See source
$\overline{\text{TR0}}$ ("not" T-Register Bit 0)	A105-54	A12-5	See source
$\overline{\text{TR1}}$ ("not" T-Register Bit 1)	A105-10	A12-11	See source
$\overline{\text{TR2}}$ ("not" T-Register Bit 2)	A105-53	A12-13	See source
$\overline{\text{TR3}}$ ("not" T-Register Bit 3)	A105-15	A12-83	See source
$\overline{\text{TR4}}$ ("not" T-Register Bit 4)	A104-54	A12-81	See source
$\overline{\text{TR5}}$ ("not" T-Register Bit 5)	A104-10	A12-77	See source
$\overline{\text{TR6}}$ ("not" T-Register Bit 6)	A104-53	A12-79	See source
$\overline{\text{TR7}}$ ("not" T-Register Bit 7)	A104-15	A12-73	See source
$\overline{\text{TR8}}$ ("not" T-Register Bit 8)	A103-54	A12-75	See source
$\overline{\text{TR9}}$ ("not" T-Register Bit 9)	A103-10	A12-76	See source
$\overline{\text{TR10}}$ ("not" T-Register Bit 10)	A103-53	A12-74	See source
$\overline{\text{TR11}}$ ("not" T-Register Bit 11)	A103-15	A12-80	See source
$\overline{\text{TR12}}$ ("not" T-Register Bit 12)	A102-54	A12-78	See source
$\overline{\text{TR13}}$ ("not" T-Register Bit 13)	A102-10	A12-84	See source
$\overline{\text{TR14}}$ ("not" T-Register Bit 14)	A102-53	A12-82	See source
$\overline{\text{TR15}}$ ("not" T-Register Bit 15)	A102-15	A12-9	See source
$\overline{\text{TR16}}$ ("not" T-Register Bit 16)	A15-53	A12-7	See option

Table 7-14. A17 Inhibit Driver Card (Module 2/3, 20000-37777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A17-47 A17-48	None
+4.5V	A100E1	A17-39 A17-40	None
+20V	A100TB2-3	A17-15 A17-16 A17-71 A17-72	None
GND (Ground)	A100E2	A17-1 A17-2 A17-85 A17-86	None
ID0M2 (Inhibit Driver, Bit 0, Module 2)	A17-25	A19-25	= MIT · $\overline{TR0}$ · MOD2
ID0M3 (Inhibit Driver, Bit 0, Module 3)	A17-26	A19-26	= MIT · $\overline{TR0}$ · MOD3
ID1M2 (Inhibit Driver, Bit 1, Module 2)	A17-27	A19-27	= MIT · $\overline{TR1}$ · MOD2
ID1M3 (Inhibit Driver, Bit 1, Module 3)	A17-28	A19-28	= MIT · $\overline{TR1}$ · MOD3
ID2M2 (Inhibit Driver, Bit 2, Module 2)	A17-29	A19-29	= MIT · $\overline{TR2}$ · MOD2
ID2M3 (Inhibit Driver, Bit 2, Module 3)	A17-30	A19-30	= MIT · $\overline{TR2}$ · MOD3
ID3M2 (Inhibit Driver, Bit 3, Module 2)	A17-31	A19-31	= MIT · $\overline{TR3}$ · MOD 2
ID3M3 (Inhibit Driver, Bit 3, Module 3)	A17-32	A19-32	= MIT · $\overline{TR3}$ · MOD3
ID4M2 (Inhibit Driver, Bit 4, Module 2)	A17-33	A19-33	= MIT · $\overline{TR4}$ · MOD2
ID4M3 (Inhibit Driver, Bit 4, Module 3)	A17-34	A19-34	= MIT · $\overline{TR4}$ · MOD3
ID5M2 (Inhibit Driver, Bit 5, Module 2)	A17-35	A19-35	= MIT · $\overline{TR5}$ · MOD2
ID5M3 (Inhibit Driver, Bit 5, Module 3)	A17-36	A19-36	= MIT · $\overline{TR5}$ · MOD3
ID6M2 (Inhibit Driver, Bit 6, Module 2)	A17-37	A19-37	= MIT · $\overline{TR6}$ · MOD2
ID6M3 (Inhibit Driver, Bit 6, Module 3)	A17-38	A19-38	= MIT · $\overline{TR6}$ - MOD3
ID7M2 (Inhibit Driver, Bit 7, Module 2)	A17-41	A19-41	= MIT · $\overline{TR7}$ · MOD2

Table 7-14. A17 Inhibit Driver Card (Module 2/3, 20000-37777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID7M3 (Inhibit Driver, Bit 7, Module 3)	A17-42	A19-42	= MIT · $\overline{TR7}$ · MOD3
ID8M2 (Inhibit Driver, Bit 8, Module 2)	A17-43	A19-43	= MIT · $\overline{TR8}$ · MOD2
ID8M3 (Inhibit Driver, Bit 8, Module 3)	A17-44	A19-44	= MIT · $\overline{TR8}$ · MOD3
ID9M2 (Inhibit Driver, Bit 9, Module 2)	A17-45	A19-45	= MIT · $\overline{TR9}$ · MOD2
ID9M3 (Inhibit Driver, Bit 9, Module 3)	A17-46	A19-46	= MIT · $\overline{TR9}$ · MOD3
ID10M2 (Inhibit Driver, Bit 10, Module 2)	A17-49	A19-49	= MIT · $\overline{TR10}$ · MOD2
ID10M3 (Inhibit Driver, Bit 10, Module 3)	A17-50	A19-50	= MIT · $\overline{TR10}$ · MOD3
ID11M2 (Inhibit Driver, Bit 11, Module 2)	A17-51	A19-51	= MIT · $\overline{TR11}$ · MOD2
ID11M3 (Inhibit Driver, Bit 11, Module 3)	A17-52	A19-52	= MIT · $\overline{TR11}$ · MOD3
ID12M2 (Inhibit Driver, Bit 12, Module 2)	A17-53	A19-53	= MIT · $\overline{TR12}$ · MOD2
ID12M3 (Inhibit Driver, Bit 12, Module 3)	A17-54	A19-54	= MIT · $\overline{TR12}$ · MOD3
ID13M2 (Inhibit Driver, Bit 13, Module 2)	A17-55	A19-55	= MIT · $\overline{TR13}$ · MOD2
ID13M3 (Inhibit Driver, Bit 13, Module 3)	A17-56	A19-56	= MIT · $\overline{TR13}$ · MOD3
ID14M2 (Inhibit Driver, Bit 14, Module 2)	A17-57	A19-57	= MIT · $\overline{TR14}$ · MOD2
ID14M3 (Inhibit Driver, Bit 14, Module 3)	A17-58	A19-58	= MIT · $\overline{TR14}$ · MOD3
ID15M2 (Inhibit Driver, Bit 15, Module 2)	A17-59	A19-59	= MIT · $\overline{TR15}$ · MOD2
ID15M3 (Inhibit Driver, Bit 15, Module 3)	A17-60	A19-60	= MIT · $\overline{TR15}$ · MOD3
ID16M2 (Inhibit Driver, Bit 16, Module 2)	A17-61	A19-61	= MIT · $\overline{TR16}$ · MOD2
ID16M3 (Inhibit Driver, Bit 16, Module 3)	A17-62	A19-62	= MIT · $\overline{TR16}$ · MOD3

Table 7-14. A17 Inhibit Driver Card (Module 2/3, 20000-37777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
MWTX/MITX (Memory Write Time Excludable/Memory Inhibit Time Excludable)	A13-77	A17-4	See source
MOD2 (Module 2)	A14-45	A17-6	See source
MOD3 (Module 3)	A14-51	A17-12	See source
$\overline{TR0}$ ("not" T-Register Bit 0)	A105-54	A17-5	See source
$\overline{TR1}$ ("not" T-Register Bit 1)	A105-10	A17-11	See source
$\overline{TR2}$ ("not" T-Register Bit 2)	A105-53	A17-13	See source
$\overline{TR3}$ ("not" T-Register Bit 3)	A105-15	A17-83	See source
$\overline{TR4}$ ("not" T-Register Bit 4)	A104-54	A17-81	See source
$\overline{TR5}$ ("not" T-Register Bit 5)	A104-10	A17-77	See source
$\overline{TR6}$ ("not" T-Register Bit 6)	A104-53	A17-79	See source
$\overline{TR7}$ ("not" T-Register Bit 7)	A104-15	A17-73	See source
$\overline{TR8}$ ("not" T-Register Bit 8)	A103-54	A17-75	See source
$\overline{TR9}$ ("not" T-Register Bit 9)	A103-10	A17-76	See source
$\overline{TR10}$ ("not" T-Register Bit 10)	A103-53	A17-74	See source
$\overline{TR11}$ ("not" T-Register Bit 11)	A103-15	A17-80	See source
$\overline{TR12}$ ("not" T-Register Bit 12)	A102-54	A17-78	See source
$\overline{TR13}$ ("not" T-Register Bit 13)	A102-10	A17-84	See source
$\overline{TR14}$ ("not" T-Register Bit 14)	A102-53	A17-82	See source
$\overline{TR15}$ ("not" T-Register Bit 15)	A102-15	A17-9	See source
$\overline{TR16}$ ("not" T-Register Bit 16)	A15-53	A17-7	See option

Table 7-15. A22 Inhibit Driver Card (Module 0/1, 00002-17777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A22-47 A22-48	None
+4.5V	A100E1	A22-39 A22-40	None
+20V	A100TB2-3	A22-15 A22-16 A22-71 A22-72	None
GND (Ground)	A100E2	A22-1 A22-2 A22-85 A22-86	None
ID0M0 (Inhibit Driver, Bit 0, Module 0)	A22-25	A20-25	= MIT · $\overline{\text{TR 0}}$ · MOD0
ID0M1 (Inhibit Driver, Bit 0, Module 1)	A22-26	A20-26	= MIT · $\overline{\text{TR0}}$ · MOD0
ID1M0 (Inhibit Driver, Bit 1, Module 0)	A22-27	A20-27	= MIT · $\overline{\text{TR0}}$ · MOD1
ID1M1 (Inhibit Driver, Bit 1, Module 1)	A22-28	A20-28	= MIT · $\overline{\text{TR1}}$ · MOD0
ID2M0 (Inhibit Driver, Bit 2, Module 0)	A22-29	A20-29	= MIT · $\overline{\text{TR1}}$ · MOD1
ID2M1 (Inhibit Driver, Bit 2, Module 1)	A22-30	A20-30	= MIT · $\overline{\text{TR2}}$ · MOD0
ID3M0 (Inhibit Driver, Bit 3, Module 0)	A22-31	A20-31	= MIT · $\overline{\text{TR2}}$ · MOD1
ID3M1 (Inhibit Driver, Bit 3, Module 1)	A22-32	A20-32	= MIT · $\overline{\text{TR3}}$ · MOD0
ID4M0 (Inhibit Driver, Bit 4, Module 0)	A22-33	A20-33	= MIT · $\overline{\text{TR3}}$ · MOD1
ID4M1 (Inhibit Driver, Bit 4, Module 1)	A22-34	A20-34	= MIT · $\overline{\text{TR4}}$ · MOD0
ID5M0 (Inhibit Driver, Bit 5, Module 0)	A22-35	A20-35	= MIT · $\overline{\text{TR4}}$ · MOD1
ID5M1 (Inhibit Driver, Bit 5, Module 1)	A22-36	A20-36	= MIT · $\overline{\text{TR5}}$ · MOD0
ID6M0 (Inhibit Driver, Bit 6, Module 0)	A22-37	A20-37	= MIT · $\overline{\text{TR5}}$ · MOD1
ID6M1 (Inhibit Driver, Bit 6, Module 1)	A22-38	A20-38	= MIT · $\overline{\text{TR6}}$ · MOD0
ID7M0 (Inhibit Driver, Bit 7, Module 0)	A22-41	A20-41	= MIT · $\overline{\text{TR6}}$ · MOD1

Table 7-15. A22 Inhibit Driver Card (Module 0/1, 00002-17777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID7M1 (Inhibit Driver, Bit 7, Module 1)	A22-42	A20-42	= MIT · $\overline{TR7}$ · MOD1
ID8M0 (Inhibit Driver, Bit 8, Module 0)	A22-43	A20-43	= MIT · $\overline{TR8}$ · MOD0
ID8M1 (Inhibit Driver, Bit 8, Module 1)	A22-44	A20-44	= MIT · $\overline{TR8}$ · MOD1
ID9M0 (Inhibit Driver, Bit 9, Module 0)	A22-45	A20-45	= MIT · $\overline{TR9}$ · MOD0
ID9M1 (Inhibit Driver, Bit 9, Module 1)	A22-46	A20-46	= MIT · $\overline{TR9}$ · MOD1
ID10M0 (Inhibit Driver, Bit 10, Module 0)	A22-49	A20-49	= MIT · $\overline{TR10}$ · MOD0
ID10M1 (Inhibit Driver, Bit 10, Module 1)	A22-50	A20-50	= MIT · $\overline{TR10}$ · MOD1
ID11M0 (Inhibit Driver, Bit 11, Module 0)	A22-51	A20-51	= MIT · $\overline{TR11}$ · MOD0
ID11M1 (Inhibit Driver, Bit 11, Module 1)	A22-52	A20-52	= MIT · $\overline{TR11}$ · MOD1
ID12M0 (Inhibit Driver, Bit 12, Module 0)	A22-53	A20-53	= MIT · $\overline{TR12}$ · MOD0
ID12M1 (Inhibit Driver, Bit 12, Module 1)	A22-54	A20-54	= MIT · $\overline{TR12}$ · MOD1
ID13M0 (Inhibit Driver, Bit 13, Module 0)	A22-55	A20-55	= MIT · $\overline{TR13}$ · MOD0
ID13M1 (Inhibit Driver, Bit 13, Module 1)	A22-56	A20-56	= MIT · $\overline{TR13}$ · MOD1
ID14M0 (Inhibit Driver, Bit 14, Module 0)	A22-57	A20-57	= MIT · $\overline{TR14}$ · MOD0
ID14M1 (Inhibit Driver, Bit 14, Module 1)	A22-58	A20-58	= MIT · $\overline{TR14}$ · MOD1
ID15M0 (Inhibit Driver, Bit 15, Module 0)	A22-59	A20-59	= MIT · $\overline{TR15}$ · MOD0
ID15M1 (Inhibit Driver, Bit 15, Module 1)	A22-60	A20-60	= MIT · $\overline{TR15}$ · MOD1
ID16M0 (Inhibit Driver, Bit 16, Module 0)	A22-61	A20-61	= MIT · $\overline{TR16}$ · MOD0
ID16M1 (Inhibit Driver, Bit 16, Module 1)	A22-62	A20-62	= MIT · $\overline{TR16}$ · MOD1

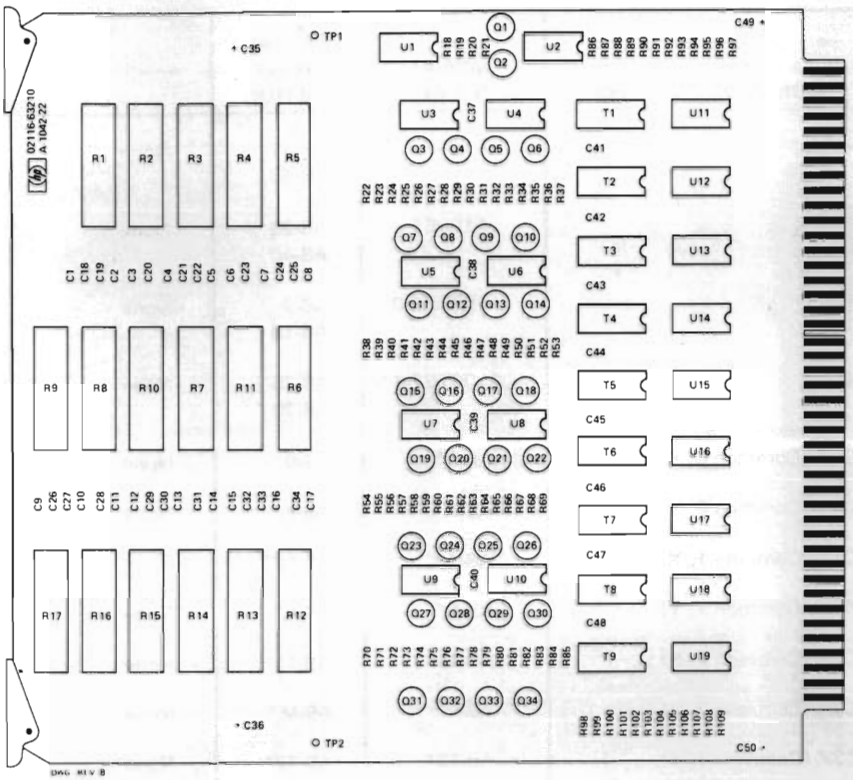
Table 7-15. A22 Inhibit Driver Card (Module 0/1, 00002-17777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
MITX (Memory Inhibit Time Excludable)	A13-77	A22-4	See source
MOD0 (Module 0)	A14-35	A22-6	See source
MOD1 (Module 1)	A14-41	A22-12	See source
$\overline{TR0}$ ("not" T-Register Bit 0)	A105-54	A22-5	See source
$\overline{TR1}$ ("not" T-Register Bit 1)	A105-10	A22-11	See source
$\overline{TR2}$ ("not" T-Register Bit 2)	A105-53	A22-13	See source
$\overline{TR3}$ ("not" T-Register Bit 3)	A105-15	A22-83	See source
$\overline{TR4}$ ("not" T-Register Bit 4)	A104-54	A22-81	See source
$\overline{TR5}$ ("not" T-Register Bit 5)	A104-10	A22-77	See source
$\overline{TR6}$ ("not" T-Register Bit 6)	A104-53	A22-79	See source
$\overline{TR7}$ ("not" T-Register Bit 7)	A104-15	A22-73	See source
$\overline{TR8}$ ("not" T-Register Bit 8)	A103-54	A22-75	See source
$\overline{TR9}$ ("not" T-Register Bit 9)	A103-10	A22-76	See source
$\overline{TR10}$ ("not" T-Register Bit 10)	A103-53	A22-74	See source
$\overline{TR11}$ ("not" T-Register Bit 11)	A103-15	A22-80	See source
$\overline{TR12}$ ("not" T-Register Bit 12)	A102-54	A22-78	See source
$\overline{TR13}$ ("not" T-Register Bit 13)	A102-10	A22-84	See source
$\overline{TR14}$ ("not" T-Register Bit 14)	A102-53	A22-82	See source
$\overline{TR15}$ ("not" T-Register Bit 15)	A102-15	A22-9	See source
$\overline{TR16}$ ("not" T-Register Bit 16)	A15-53	A22-7	See option

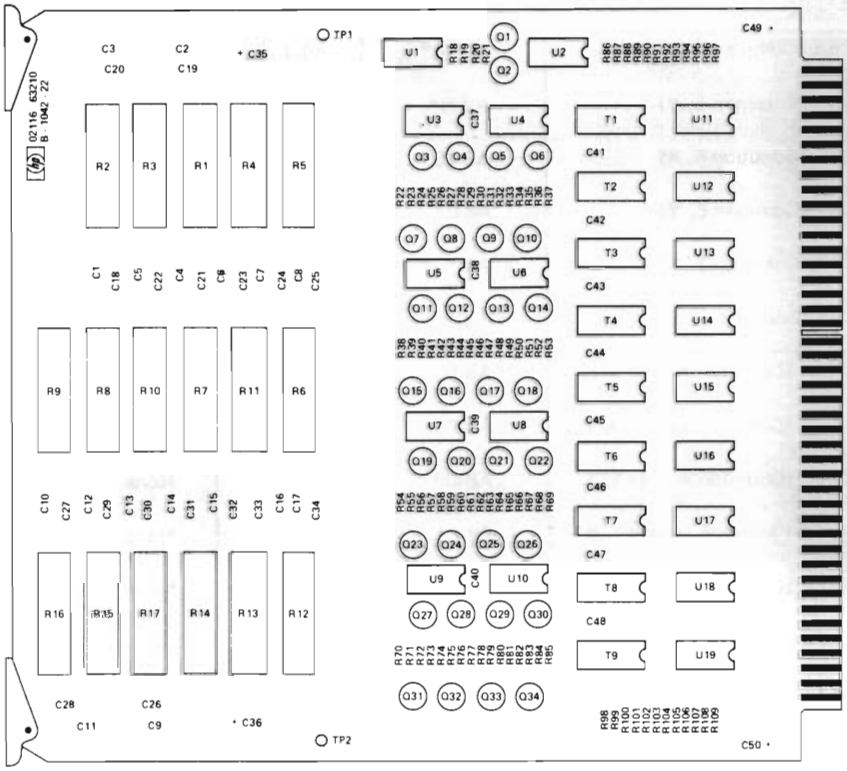
Table 7-16. A7, A12, A17, or A22 Inhibit Driver Card (02116-63210), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C17, C41 thru C48	0160-0127	Capacitor, Fxd, Cer, 1.0 uF, 20%, 25 VDCW	56289	5C13CS-CML
C18 thru C34*	0160-2223	Capacitor, Fxd, Mica, 1600 pF, 5%	28480	0160-2223
C18 thru C34**	0160-3710	Capacitor, Fxd, Mica, 1600 pF, 5%	72136	DM15F162S0
C35,36	0180-0116	Capacitor, Fxd, Elect, 6.8 uF, 10%, 35 VDCW	90201	TA5685K035PIC
C37 thru C40	0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80-20%, 100 VDCW	28480	0160-2055
C49,50	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 10 VDCW	56289	150D225X9020A2-DYS
Q1 thru Q34	1854-0019	Transistor, Si, NPN	28480	1854-0019
R1 thru R17	0811-2988	Resistor, Fxd, ww, 22 ohms	28480	0811-2988
R18,19,23,24,27,28,31,32, 35,36,39,40,43,44,47, 48,51,52,55,56,59,60, 63,64,67,68,71,72,75, 76,79,80,83,84	0698-4037	Resistor, Fxd, Flm, 46.4 ohms, 1%, 1/8W	28480	0698-4037
R20,21,22,25,26,29,30,33, 34,37,38,41,42,45,46, 49,50,53,54,57,58,61, 62,65,66,69,70,73,74, 77,78,81,82,85	0757-0399	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/8W	28480	0757-0399
R86 thru R92	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R93 thru R109	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082
T1 thru T9	9100-3130	Transformer, Pulse	28480	9100-3130
U1,U3 thru U10	1820-0141	Integrated Circuit	28480	1820-0141
U2	1820-0140	Integrated Circuit	28480	1820-0140
U11 thru U19	1821-0006	Integrated Circuit	28480	1821-0006

* Used on card revision A-1042-22
** Used on card revision B-1042-22



A-1042-22



B-1042-22

Table 7-17. A8 X-Y Driver/Switch Card (Module 6/7, 60000-77777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A8-47 A8-48	None
+4.5V	A100E1	A8-39 A8-40	None
+20V	A100TB2-3	A8-9 A8-10	None
-20V	A100TB2-4	A8-75 A8-76	None
C0X (Common 0, X)	A8-9*	A9-9*	None
C0Y (Common 0, Y)	A8-K*	A9-K*	None
C1X (Common 1, X)	A8-10*	A9-10*	None
C1Y (Common 1, Y)	A8-L*	A9-L*	None
C2X (Common 2, X)	A8-11*	A9-11*	None
C2Y (Common 2, Y)	A8-M*	A9-M*	None
C3X (Common 3, X)	A8-12*	A9-12*	None
C3Y (Common 3, Y)	A8-N*	A9-N*	None
C4X (Common 4, X)	A8-13*	A9-13*	None
C4Y (Common 4, Y)	A8-P*	A9-P*	None
C5X (Common 5, X)	A8-14*	A9-14*	None
C5Y (Common 5, Y)	A8-R*	A9-R*	None
C6X (Common 6, X)	A8-15*	A9-15*	None
C6Y (Common 6, Y)	A8-S*	A9-S*	None
C7X (Common 7, X)	A8-16*	A9-16*	None
C7Y (Common 7, Y)	A8-T*	A9-T*	None
CA0X (Common Anode 0, X)	A8-E*	A9-E*	None
CA0Y (Common Anode 0, Y)	A8-D*	A9-D*	None
CA1X (Common Anode 1, X)	A8-U*	A9-U*	None
CA1Y (Common Anode 1, Y)	A8-C*	A9-C*	None
CA2X (Common Anode 2, X)	A8-F*	A9-F*	None
CA2Y (Common Anode 2, Y)	A8-Y*	A9-Y*	None
CA3X (Common Anode 3, X)	A8-V*	A9-V*	None
CA3Y (Common Anode 3, Y)	A8-Z*	A9-Z*	None
CA4X (Common Anode 4, X)	A8-H*	A9-H*	None

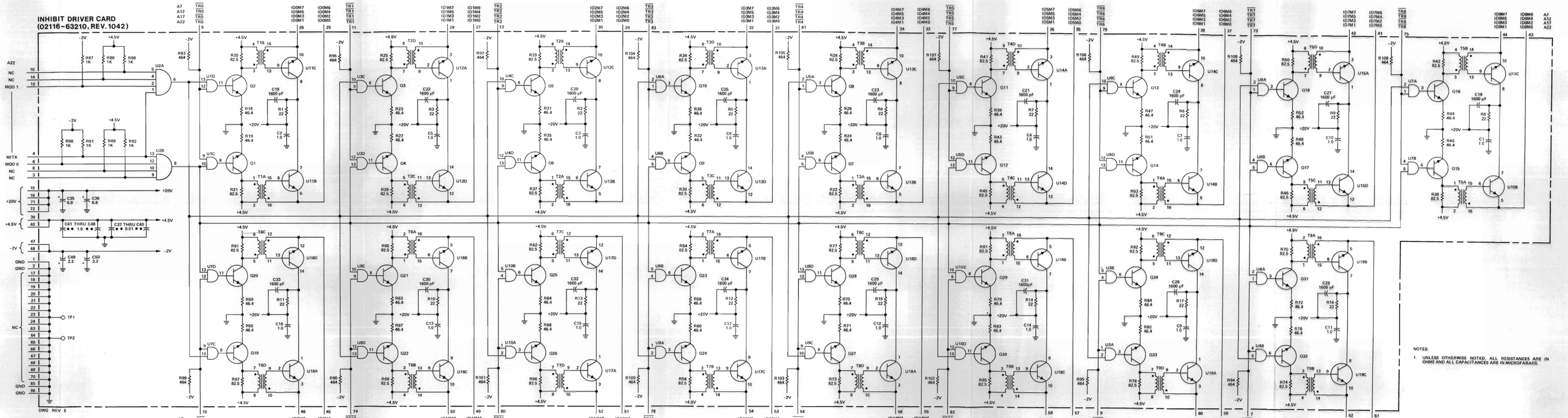


Figure 7-6. A7, A12, A17, A22 Inhibit Driver Card (02116-63210) Parts Location and Schematic Diagram

Table 7-17. A8 X-Y Driver/Switch Card (Module 6/7, 60000-77777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
CA4Y (Common Anode 4, Y)	A8-B*	A9-B*	None
CA5X (Common Anode 5, X)	A8-W*	A9-W*	None
CA5Y (Common Anode 5, Y)	A8-A*	A9-A*	None
CA6X (Common Anode 6, X)	A8-J*	A9-J*	None
CA6Y (Common Anode 6, Y)	A8-AA*	A9-AA*	None
CA7X (Common Anode 7, X)	A8-X*	A9-X*	None
CA7Y (Common Anode 7, Y)	A8-BB*	A9-BB*	None
CC0X (Common Cathode 0, X)	A8-5*	A9-5*	None
CC0Y (Common Cathode 0, Y)	A8-4*	A9-4*	None
CC1X (Common Cathode 1, X)	A8-17*	A9-17*	None
CC1Y (Common Cathode 1, Y)	A8-3*	A9-3*	None
CC2X (Common Cathode 2, X)	A8-6*	A9-6*	None
CC2Y (Common Cathode 2, Y)	A8-21*	A9-21*	None
CC3X (Common Cathode 3, X)	A8-18*	A9-18*	None
CC3Y (Common Cathode 3, Y)	A8-22*	A9-22*	None
CC4X (Common Cathode 4, X)	A8-7*	A9-7*	None
CC4Y (Common Cathode 4, Y)	A8-2*	A9-2*	None
CC5X (Common Cathode 5, X)	A8-19*	A9-19*	None
CC5Y (Common Cathode 5, Y)	A8-1*	A9-1*	None
CC6X (Common Cathode 6, X)	A8-8*	A9-8*	None
CC6Y (Common Cathode 6, Y)	A8-23*	A9-23*	None
CC7X (Common Cathode 7, X)	A8-20*	A9-20*	None
CC7Y (Common Cathode 7, Y)	A8-24*	A9-24*	None
GND (Ground)	A100E2	A8-1 A8-2 A8-85 A8-86	None
M0 (Memory Address Bit 0)	A1-41 A2-41 A14-6	A8-35	See source or option
M1 (Memory Address Bit 1)	A1-46 A2-46 A14-10	A8-36	See source or option
M2 (Memory Address Bit 2)	A1-45 A2-45 A14-14	A8-37	See source or option

Table 7-17. A8 X-Y Driver/Switch Card (Module 6/7, 60000-77777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
M3 (Memory Address Bit 3)	A1-55 A2-55 A14-18	A8-33	See source or option
M4 (Memory Address Bit 4)	A1-65 A2-65 A14-22	A8-32	See source or option
M5 (Memory Address Bit 5)	A1-63 A2-63 A14-26	A8-31	See source or option
M6 (Memory Address Bit 6)	A1-71 A2-71 A14-30	A8-49	See source or option
M7 (Memory Address Bit 7)	A1-72 A2-72 A14-34	A8-52	See source or option
M8 (Memory Address Bit 8)	A1-83 A2-83 A14-38	A8-51	See source or option
M9 (Memory Address Bit 9)	A1-82 A2-82 A14-44	A8-53	See source or option
M10 (Memory Address Bit 10)	A1-6 A2-6 A14-50	A8-56	See source or option
M11 (Memory Address Bit 11)	A1-10 A2-10 A14-54	A8-55	See source or option
$\overline{\text{MOD6/7}}$ ("not" Module 6 or 7)	A14-2	A8-46	See source
MPT3 (Memory Protect, 24K Memory)	A11-27	A8-28	None
MPT4 (Memory Protect, 32K Memory)	A8-27	A14-15	None
MRT1 (Memory Read Time 1)	A106-29	A8-54 A8-57	See source
MWT1 (Memory Write Time 1)	A106-35	A8-50 A8-58	See source
PON (Power On Normal)	A6-58	A8-42	See source
XT1 (X-Drive Time 1)	A14-29	A8-30 A8-38	See source
XT2 (X-Drive Time 2)	A14-37	A8-29 A8-34	See source

Table 7-18. A11 X-Y Driver/Switch Card (Module 4/5, 40000-57777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A11-47 A11-48	None
+4.5V	A100E1	A11-39 A11-40	None
+20V	A100TB2-3	A11-9 A11-10	None
-20V	A100TB2-4	A11-75 A11-76	None
C0X (Common 0, X)	A11-9*	A10-9*	None
C0Y (Common 0, Y)	A11-K*	A10-K*	None
C1X (Common 1, X)	A11-10*	A10-10*	None
C1Y (Common 1, Y)	A11-L*	A10-L*	None
C2X (Common 2, X)	A11-11*	A10-11*	None
C2Y (Common 2, Y)	A11-M*	A10-M*	None
C3X (Common 3, X)	A11-12*	A10-12*	None
C3Y (Common 3, Y)	A11-N*	A10-N*	None
C4X (Common 4, X)	A11-13*	A10-13*	None
C4Y (Common 4, Y)	A11-P*	A10-P*	None
C5X (Common 5, X)	A11-14*	A10-14*	None
C5Y (Common 5, Y)	A11-R*	A10-R*	None
C6X (Common 6, X)	A11-15*	A10-15*	None
C6Y (Common 6, Y)	A11-S*	A10-S*	None
C7X (Common 7, X)	A11-16*	A10-16*	None
C7Y (Common 7, Y)	A11-T*	A10-T*	None
CA0X (Common Anode 0, X)	A11-E*	A10-E*	None
CA0Y (Common Anode 0, Y)	A11-D*	A10-D*	None
CA1X (Common Anode 1, X)	A11-U*	A10-U*	None
CA1Y (Common Anode 1, Y)	A11-C*	A10-C*	None
CA2X (Common Anode 2, X)	A11-F*	A10-F*	None
CA2Y (Common Anode 2, Y)	A11-Y*	A10-Y*	None
CA3X (Common Anode 3, X)	A11-V*	A10-V*	None
CA3Y (Common Anode 3, Y)	A11-Z*	A10-Z*	None
CA4X (Common Anode 4, X)	A11-H*	A10-H*	None
CA4Y (Common Anode 4, Y)	A11-B*	A10-B*	None
CA5X (Common Anode 5, X)	A11-W*	A10-W*	None
CA5Y (Common Anode 5, Y)	A11-A*	A10-A*	None

Table 7-18. A11 X-Y Driver/Switch Card (Module 4/5, 40000-57777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
CA6X (Common Anode 6, X)	A11-J*	A10-J*	None
CA6Y (Common Anode 6, Y)	A11-AA*	A10-AA*	None
CA7X (Common Anode 7, X)	A11-X*	A10-X*	None
CA7Y (Common Anode 7, Y)	A11-BB*	A10-BB*	None
CC0X (Common Cathode 0, X)	A11-5*	A10-5*	None
CC0Y (Common Cathode 0, Y)	A11-4*	A10-4*	None
CC1X (Common Cathode 1, X)	A11-17*	A10-17*	None
CC1Y (Common Cathode 1, Y)	A11-3*	A10-3*	None
CC2X (Common Cathode 2, X)	A11-6*	A10-6*	None
CC2Y (Common Cathode 2, Y)	A11-21*	A10-21*	None
CC3X (Common Cathode 3, X)	A11-18*	A10-18*	None
CC3Y (Common Cathode 3, Y)	A11-22*	A10-22*	None
CC4X (Common Cathode 4, X)	A11-7*	A10-7*	None
CC4Y (Common Cathode 4, Y)	A11-2*	A10-2*	None
CC5X (Common Cathode 5, X)	A11-19*	A10-19*	None
CC5Y (Common Cathode 5, Y)	A11-1*	A10-1*	None
CC6X (Common Cathode 6, X)	A11-8*	A10-8*	None
CC6Y (Common Cathode 6, Y)	A11-23*	A10-23*	None
CC7X (Common Cathode 7, X)	A11-20*	A10-20*	None
CC7Y (Common Cathode 7, Y)	A11-24*	A10-24*	None
GND (Ground)	A100E2	A11-1 A11-2 A11-85 A11-86	None
M0 (Memory Address Bit 0)	A1-41 A2-41 A14-6	A11-35	See source or option
M1 (Memory Address Bit 1)	A1-46 A2-46 A14-10	A11-36	See source or option
M2 (Memory Address Bit 2)	A1-45 A2-45 A14-14	A11-37	See source or option
M3 (Memory Address Bit 3)	A1-55 A2-55 A14-18	A11-33	See source or option
M4 (Memory Address Bit 4)	A1-65 A2-65 A14-22	A11-32	See source or option

Table 7-18. A11 X-Y Driver/Switch Card (Module 4/5, 40000-57777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
M5 (Memory Address Bit 5)	A1-63 A2-63 A14-26	A11-31	See source or option
M6 (Memory Address Bit 6)	A1-71 A2-71 A14-30	A11-49	See source or option
M7 (Memory Address Bit 7)	A1-72 A2-72 A14-34	A11-52	See source or option
M8 (Memory Address Bit 8)	A1-83 A2-83 A14-38	A11-51	See source or option
M9 (Memory Address Bit 9)	A1-82 A2-82 A14-44	A11-53	See source or option
M10 (Memory Address Bit 10)	A1-6 A2-6 A14-50	A11-56	See source or option
M11 (Memory Address Bit 11)	A1-10 A2-10 A14-54	A11-55	See source or option
M14 (Memory Address Bit 14)	A1-7 A2-7 A14-66	A11-23	See source or option
MMD14 (Memory Module Decode, Bit 14)	A11-25	A14-23	= M14 + DMA option signal
$\overline{\text{MOD4/5}}$ ("not" Module 4 or 5)	A14-17	A11-46	See source
MPT2 (Memory Protect, 16K Memory)	A18-27	A11-28	See option
MPT3 (Memory Protect, 24K Memory)	A11-27	A8-28 A14-11	None
MRT1 (Memory Read Time 1)	A106-29	A11-54 A11-57	See source
MWT1 (Memory Write Time 1)	A106-35	A11-50 A11-58	See source
PON (Power On Normal)	A6-58	A11-42	See source
XT1 (X-Drive Time 1)	A14-29	A11-30 A11-38	See source
XT2 (X-Drive Time 2)	A14-37	A11-29 A11-34	See source

Table 7-19. A18 X-Y Driver/Switch Card (Module 2/3, 20000-37777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A18-47 A18-48	None
+4.5V	A100E1	A18-39 A18-40	None
+20V	A100TB2-3	A18-9 A18-10	None
-20V	A100TB2-4	A18-75 A18-76	None
C0X (Common 0, X)	A18-9*	A19-9*	None
C0Y (Common 0, Y)	A18-K*	A19-K*	None
C1X (Common 1, X)	A18-10*	A19-10*	None
C1Y (Common 1, Y)	A18-L*	A19-L*	None
C2X (Common 2, X)	A18-11*	A19-11*	None
C2Y (Common 2, Y)	A18-M*	A19-M*	None
C3X (Common 3, X)	A18-12*	A19-12*	None
C3Y (Common 3, Y)	A18-N*	A19-N*	None
C4X (Common 4, X)	A18-13*	A19-13*	None
C4Y (Common 4, Y)	A18-P*	A19-P*	None
C5X (Common 5, X)	A18-14*	A19-14*	None
C5Y (Common 5, Y)	A18-R*	A19-R*	None
C6X (Common 6, X)	A18-15*	A19-15*	None
C6Y (Common 6, Y)	A18-S*	A19-S*	None
C7X (Common 7, X)	A18-16*	A19-16*	None
C7Y (Common 7, Y)	A18-T*	A19-T*	None
CA0X (Common Anode 0, X)	A18-E*	A19-E*	None
CA0Y (Common Anode 0, Y)	A18-D*	A19-D*	None
CA1X (Common Anode 1, X)	A18-U*	A19-U*	None
CA1Y (Common Anode 1, Y)	A18-C*	A19-C*	None
CA2X (Common Anode 2, X)	A18-F*	A19-F*	None
CA2Y (Common Anode 2, Y)	A18-Y*	A19-Y*	None
CA3X (Common Anode 3, X)	A18-V*	A19-V*	None
CA3Y (Common Anode 3, Y)	A18-Z*	A19-Z*	None
CA4X (Common Anode 4, X)	A18-H*	A19-H*	None
CA4Y (Common Anode 4, Y)	A18-B*	A19-B*	None
CA5X (Common Anode 5, X)	A18-W*	A19-W*	None

Table 7-19. A18 X-Y Driver/Switch Card (Module 2/3, 20000-37777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
CA5Y (Common Anode 5, Y)	A18-A*	A19-A*	None
CA6X (Common Anode 6, X)	A18-J*	A19-J*	None
CA6Y (Common Anode 6, Y)	A18-AA*	A19-AA*	None
CA7X (Common Anode 7, X)	A18-X*	A19-X*	None
CA7Y (Common Anode 7, Y)	A18-BB*	A19-BB*	None
CC0X (Common Cathode 0, X)	A18-5*	A19-5*	None
CC0Y (Common Cathode 0, Y)	A18-4*	A19-4*	None
CC1X (Common Cathode 1, X)	A18-17*	A19-17*	None
CC1Y (Common Cathode 1, Y)	A18-3*	A19-3*	None
CC2X (Common Cathode 2, X)	A18-6*	A19-6*	None
CC2Y (Common Cathode 2, Y)	A18-21*	A19-21*	None
CC3X (Common Cathode 3, X)	A18-18*	A19-18*	None
CC3Y (Common Cathode 3, Y)	A18-22*	A19-22*	None
CC4X (Common Cathode 4, X)	A18-7*	A19-7*	None
CC4Y (Common Cathode 4, Y)	A18-2*	A19-2*	None
CC5X (Common Cathode 5, X)	A18-19*	A19-19*	None
CC5Y (Common Cathode 5, Y)	A18-1*	A19-1*	None
CC6X (Common Cathode 6, X)	A18-8*	A19-8*	None
CC6Y (Common Cathode 6, Y)	A18-23*	A19-23*	None
CC7X (Common Cathode 7, X)	A18-20*	A19-20*	None
CC7Y (Common Cathode 7, Y)	A18-24*	A19-24*	None
GND (Ground)	A100E2	A18-1 A18-2 A18-85 A18-86	None
M0 (Memory Address Bit 0)	A1-41 A2-41 A14-6	A18-35	See source or option
M1 (Memory Address Bit 1)	A1-46 A2-46 A14-10	A18-36	See source or option
M2 (Memory Address Bit 2)	A1-45 A2-45 A14-14	A18-37	See source or option
M3 (Memory Address Bit 3)	A1-55 A2-55 A14-18	A18-33	See source or option

Table 7-19. A18 X-Y Driver/Switch Card (Module 2/3, 20000-37777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
M4 (Memory Address Bit 4)	A1-65 A2-65 A14-22	A18-32	See source or option
M5 (Memory Address Bit 5)	A1-63 A2-63 A14-26	A18-31	See source or option
M6 (Memory Address Bit 6)	A1-71 A2-71 A14-30	A18-49	See source or option
M7 (Memory Address Bit 7)	A1-72 A2-72 A14-34	A18-52	See source or option
M8 (Memory Address Bit 8)	A1-83 A2-83 A14-38	A18-51	See source or option
M9 (Memory Address Bit 9)	A1-82 A2-82 A14-44	A18-53	See source or option
M10 (Memory Address Bit 10)	A1-6 A2-6 A14-50	A18-56	See source or option
M11 (Memory Address Bit 11)	A1-10 A2-10 A14-54	A18-55	See source or option
M13 (Memory Address Bit 13)	A1-16 A2-16 A14-62	A18-23	See source or option
MMD13 (Memory Module Decode Bit 13)	A18-25	A14-19	= M13
$\overline{\text{MOD2/3}}$ ("not" Module 2 or 3)	A14-13	A18-46	See source
MPT1 (Memory Protect, 8K Memory)	A21-27	A18-28	None
MPT2 (Memory Protect, 16K Memory)	A18-27	A11-28 A14-7	None
MRT1 (Memory Read Time 1)	A106-29	A18-54 A18-57	See source
MWT1 (Memory Write Time 1)	A106-35	A18-50 A18-58	See source
PON (Power On Normal)	A6-58	A18-42	See source
XT1 (X-Drive Time 1)	A14-29	A18-30 A18-38	See source
XT2 (X-Drive Time 2)	A14-37	A18-29 A18-34	See source

Table 7-20. A21 X-Y Driver/Switch Card (Module 0/1, 00002-17777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A21-47 A21-48	None
+4.5V	A100E1	A21-39 A21-40	None
+20V	A100TB2-3	A21-9 A21-10	None
-20V	A100TB2-4	A21-75 A21-76	None
C0X (Common 0, X)	A21-9*	A20-9*	None
C0Y (Common 0, Y)	A21-K*	A20-K*	None
C1X (Common 1, X)	A21-10*	A20-10*	None
C1Y (Common 1, Y)	A21-L*	A20-L*	None
C2X (Common 2, X)	A21-11*	A20-11*	None
C2Y (Common 2, Y)	A21-M*	A20-M*	None
C3X (Common 3, X)	A21-12*	A20-12*	None
C3Y (Common 3, Y)	A21-N*	A20-N*	None
C4X (Common 4, X)	A21-13*	A20-13*	None
C4Y (Common 4, Y)	A21-P*	A20-P*	None
C5X (Common 5, X)	A21-14*	A20-14*	None
C5Y (Common 5, Y)	A21-R*	A20-R*	None
C6X (Common 6, X)	A21-15*	A20-15*	None
C6Y (Common 6, Y)	A21-S*	A20-S*	None
C7X (Common 7, X)	A21-16*	A20-16*	None
C7Y (Common 7, Y)	A21-T*	A20-T*	None
CA0X (Common Anode 0, X)	A21-E*	A20-E*	None
CA0Y (Common Anode 0, Y)	A21-D*	A20-D*	None
CA1X (Common Anode 1, X)	A21-U*	A20-U*	None
CA1Y (Common Anode 1, Y)	A21-C*	A20-C*	None
CA2X (Common Anode 2, X)	A21-F*	A20-F*	None
CA2Y (Common Anode 2, Y)	A21-Y*	A20-Y*	None
CA3X (Common Anode 3, X)	A21-V*	A20-V*	None
CA3Y (Common Anode 3, Y)	A21-Z*	A20-Z*	None
CA4X (Common Anode 4, X)	A21-H*	A20-H*	None
CA4Y (Common Anode 4, Y)	A21-B*	A20-B*	None
CA5X (Common Anode 5, X)	A21-W*	A20-W*	None

Table 7-20. A21 X-Y Driver/Switch Card (Module 0/1, 00002-17777), Signal List (Continued)

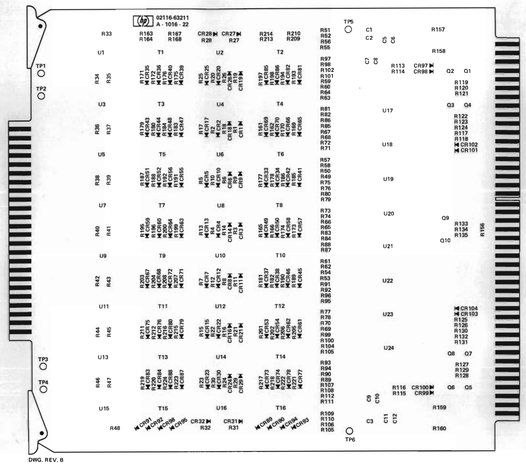
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
CA5Y (Common Anode 5, Y)	A21-A*	A20-A*	None
CA6X (Common Anode 6, X)	A21-J*	A20-J*	None
CA6Y (Common Anode 6, Y)	A21-AA*	A20-AA*	None
CA7X (Common Anode 7, X)	A21-X*	A20-X*	None
CA7Y (Common Anode 7, Y)	A21-BB*	A20-BB*	None
CC0X (Common Cathode 0, X)	A21-5*	A20-5*	None
CC0Y (Common Cathode 0, Y)	A21-4*	A20-4*	None
CC1X (Common Cathode 1, X)	A21-17*	A20-17*	None
CC1Y (Common Cathode 1, Y)	A21-3*	A20-3*	None
CC2X (Common Cathode 2, X)	A21-6*	A20-6*	None
CC2Y (Common Cathode 2, Y)	A21-21*	A20-21*	None
CC3X (Common Cathode 3, X)	A21-18*	A20-18*	None
CC3Y (Common Cathode 3, Y)	A21-22*	A20-22*	None
CC4X (Common Cathode 4, X)	A21-7*	A20-7*	None
CC4Y (Common Cathode 4, Y)	A21-2*	A20-2*	None
CC5X (Common Cathode 5, X)	A21-19*	A20-19*	None
CC5Y (Common Cathode 5, Y)	A21-1*	A20-1*	None
CC6X (Common Cathode 6, X)	A21-8*	A20-8*	None
CC6Y (Common Cathode 6, Y)	A21-23*	A20-23*	None
CC7X (Common Cathode 7, X)	A21-20*	A20-20*	None
CC7Y (Common Cathode 7, Y)	A21-24*	A20-24*	None
GND (Ground)	A100E2	A21-1 A21-2 A21-85 A21-86	None
M0 (Memory Address Bit 0)	A1-41 A2-41 A14-6	A21-35	See source or option
M1 (Memory Address Bit 1)	A1-46 A2-46 A14-10	A21-36	See source or option
M2 (Memory Address Bit 2)	A1-45 A2-45 A14-14	A21-37	See source or option
M3 (Memory Address Bit 3)	A1-55 A2-55 A14-18	A21-33	See source or option

Table 7-20. A21 X-Y Driver/Switch Card (Module 0/1, 00002-17777), Signal List (Continued)

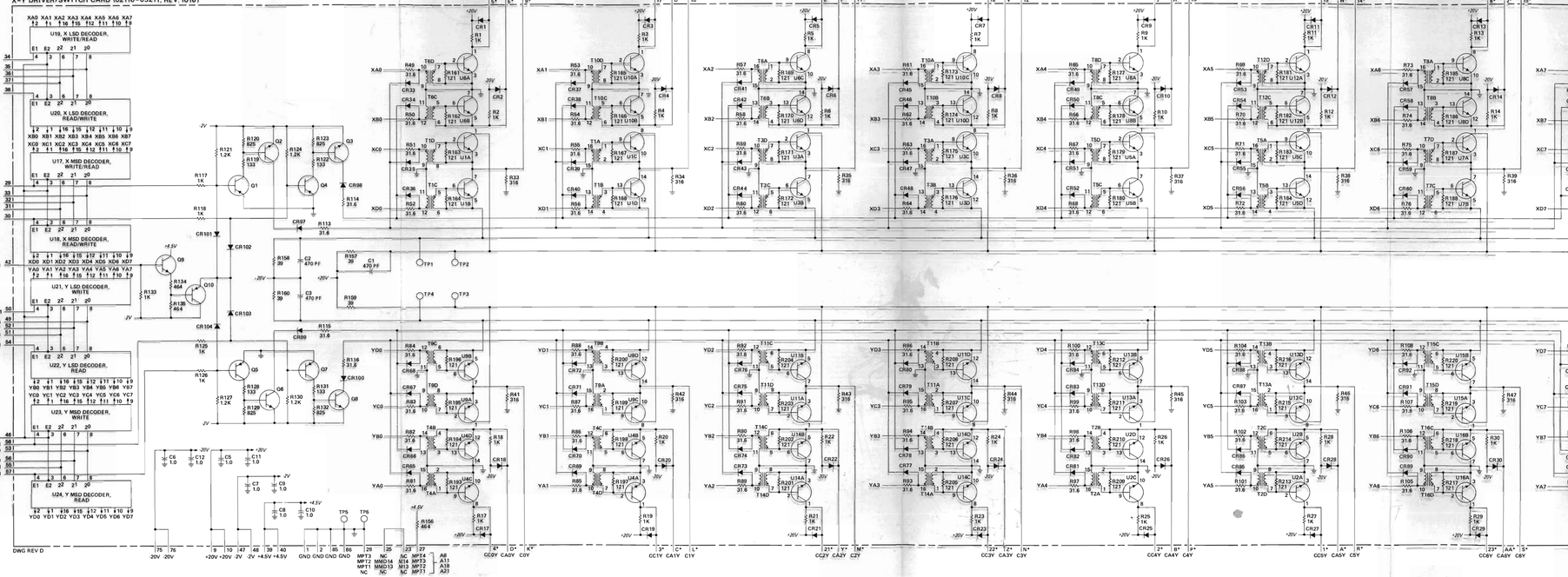
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
M4 (Memory Address Bit 4)	A1-65 A2-65 A14-22	A21-32	See source or option
M5 (Memory Address Bit 5)	A1-63 A2-63 A14-26	A21-31	See source or option
M6 (Memory Address Bit 6)	A1-71 A2-71 A14-30	A21-49	See source or option
M7 (Memory Address Bit 7)	A1-72 A2-72 A14-34	A21-52	See source or option
M8 (Memory Address Bit 8)	A1-83 A2-83 A14-38	A21-51	See source or option
M9 (Memory Address Bit 9)	A1-82 A2-82 A14-44	A21-53	See source or option
M10 (Memory Address Bit 10)	A1-6 A2-6 A14-50	A21-56	See source or option
M11 (Memory Address Bit 11)	A1-10 A2-10 A14-54	A21-55	See source or option
$\overline{\text{MOD0/1}}$ ("not" Module 0 or 1)	A14-9	A21-46	See source
MPT1 (Memory Protect 8K Memory)	A21-27	A14-3 A18-28	None
MRT1 (Memory Read Time 1)	A106-29	A21-54 A21-57	See source
MWT1 (Memory Write Time 1)	A106-35	A21-50 A21-58	See source
PON (Power On Normal)	A6-58	A21-42	See source
XT1 (X-Drive Time 1)	A14-29	A21-30 A21-38	See source
XT2 (X-Drive Time 2)	A14-37	A21-29 A21-34	See source

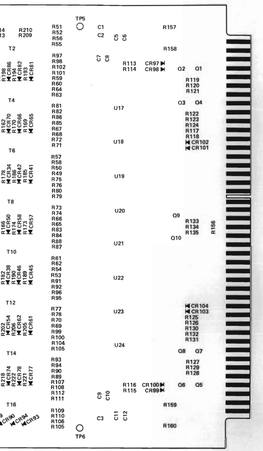
Table 7-21. A8, A11, A18, A21 X-Y Driver/Switch Card (02116-63211), Reference Designation Index

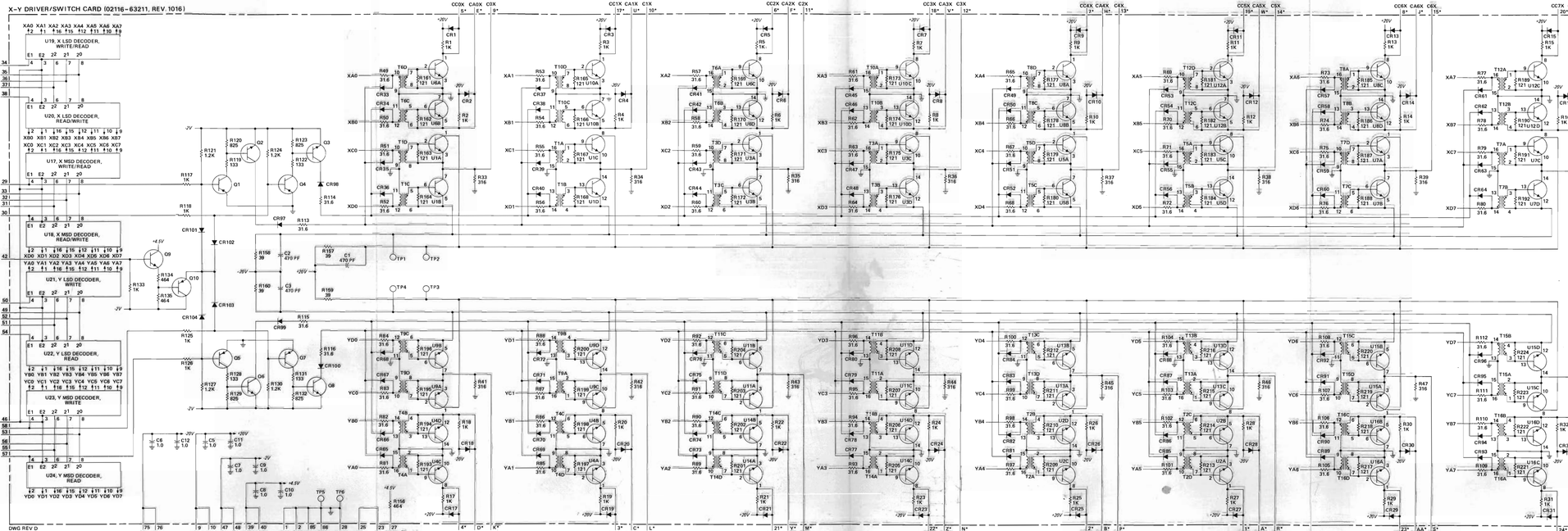
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2,3	0160-2940	Capacitor, Fxd, Mica, 470 pF, 5%, 300 VDCW	72136	RDM15F471J3C
C5 thru C12	0160-0127	Capacitor, Fxd, Cer, 1.0 uF, 20%, VDCW	56289	SC13CS-CML
CR1 thru CR100	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088
CR101 thru CR104	1910-0022	Diode, Ge, 5 WIV	14433	G401
Q1,4,5,7,10	1853-0015	Transistor, Si, PNP	80131	2N3640
Q2,3,6,8,9	1854-0019	Transistor, Si, NPN	28480	1854-0019
R1 thru R32,117,118,125, 126,133	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R33 thru R48	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	28480	0698-3444
R49 thru R116	0757-0180	Resistor, Fxd, Flm, 31.6 ohms, 1%, 1/8W	28480	0757-0180
R119,122,128,131	0698-3437	Resistor, Fxd, Flm, 133 ohms, 1%, 1/8W	28480	0698-3437
R120,123,129,132	0757-0421	Resistor, Fxd, Flm, 825 ohms, 1%, 1/8W	28480	0757-0421
R121,124,127,130	0757-0274	Resistor, Fxd, Flm, 1.21k, 1%, 1/8W	28480	0757-0274
R134,135	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082
R156	0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8W	28480	0698-3132
R157 thru R160	0811-2918	Resistor, Fxd, ww, 391 ohms, 1.0%, 5W	28480	0811-2918
R161 thru R224	0757-0403	Resistor, Fxd, Flm, 121 ohms, 1%, 1/8W	28480	0757-0403
T1 thru T16	9100-3130	Transformer, Pulse	28480	9100-3130
U1 thru U16	1821-0006	Integrated Circuit	28480	1821-0006
U17 thru U24	1820-0482	Integrated Circuit	28480	1820-0482



X-Y DRIVER/SWITCH CARD (02116-63211, REV. 1016)







NOTES:

1. AN ASTERISK INDICATES A PIN ON THE 48-PIN CONNECTOR. ALL OTHER PINS ARE ON THE 86-PIN CONNECTOR.
2. UNLESS OTHERWISE NOTED, ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
3. READ/WRITE DENOTES READ-LOWER MODULE, WRITE-UPPER MODULE. WRITE/READ DENOTES WRITE-LOWER MODULE, READ-UPPER MODULE.

Figure 7-7. A8, A11, A18, A21 X-Y Driver/Switch Card (02116-63211), Parts Location and Schematic Diagram

Table 7-22. A9 Sense Amplifier Card (Module 6/7, 60000-77777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A9-47 A9-48	None
+4.5V	A100E1	A9-39 A9-40	None
+12V	A100TB2-1	A9-13 A9-14	None
-12V	A100TB2-2	A9-73 A9-74	None
C0X (Common 0, X)	A8-9*	A9-9*	See option
C0Y (Common 0, Y)	A8-K*	A9-K*	See option
C1X (Common 1, X)	A8-10*	A9-10*	See option
C1Y (Common 1, Y)	A8-L*	A9-L*	See option
C2X (Common 2, X)	A8-11*	A9-11*	See option
C2Y (Common 2, Y)	A8-M*	A9-M*	See option
C3X (Common 3, X)	A8-12*	A9-12*	See option
C3Y (Common 3, Y)	A8-N*	A9-N*	See option
C4X (Common 4, X)	A8-13*	A9-13*	See option
C4Y (Common 4, Y)	A8-P*	A9-P*	See option
C5X (Common 5, X)	A8-14*	A9-14*	See option
C5Y (Common 5, Y)	A8-R*	A9-R*	See option
C6X (Common 6, X)	A8-15*	A9-15*	See option
C6Y (Common 6, Y)	A8-S*	A9-S*	See option
C7X (Common 7, X)	A8-16*	A9-16*	See option
C7Y (Common 7, Y)	A8-T*	A9-T*	See option
CA0X (Common Anode 0, X)	A8-E*	A9-E*	See option
CA0Y (Common Anode 0, Y)	A8-D*	A9-D*	See option
CA1X (Common Anode 1, X)	A8-U*	A9-U*	See option
CA1Y (Common Anode 1, Y)	A8-C*	A9-C*	See option
CA2X (Common Anode 2, X)	A8-F*	A9-F*	See option
CA2Y (Common Anode 2, Y)	A8-Y*	A9-Y*	See option
CA3X (Common Anode 3, X)	A8-V*	A9-V*	See option
CA3Y (Common Anode 3, Y)	A8-Z*	A9-Z*	See option
CA4X (Common Anode 4, X)	A8-H*	A9-H*	See option
CA4Y (Common Anode 4, Y)	A8-B*	A9-B*	See option
CA5X (Common Anode 5, X)	A8-W*	A9-W*	See option

Table 7-22. A9 Sense Amplifier Card (Module 6/7, 60000-77777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
CA5Y (Common Anode 5, Y)	A8-A*	A9-A*	See option
CA6X (Common Anode 6, X)	A8-J*	A9-J*	See option
CA6Y (Common Anode 6, Y)	A8-AA*	A9-AA*	See option
CA7X (Common Anode 7, X)	A8-X*	A9-X*	See option
CA7Y (Common Anode 7, Y)	A8-BB*	A9-BB*	See option
CC0X (Common Cathode 0, X)	A8-5*	A9-5*	See option
CC0Y (Common Cathode 0, Y)	A8-4*	A9-4*	See option
CC1X (Common Cathode 1, X)	A8-17*	A9-17*	See option
CC1Y (Common Cathode 1, Y)	A8-3*	A9-3*	See option
CC2X (Common Cathode 2, X)	A8-6*	A9-6*	See option
CC2Y (Common Cathode 2, Y)	A8-21*	A9-21*	See option
CC3X (Common Cathode 3, X)	A8-18*	A9-18*	See option
CC3Y (Common Cathode 3, Y)	A8-22*	A9-22*	See option
CC4X (Common Cathode 4, X)	A8-7*	A9-7*	See option
CC4Y (Common Cathode 4, Y)	A8-2*	A9-2*	See option
CC5X (Common Cathode 5, X)	A8-19*	A9-19*	See option
CC5Y (Common Cathode 5, Y)	A8-1*	A9-1*	See option
CC6X (Common Cathode 6, X)	A8-8*	A9-8*	See option
CC6Y (Common Cathode 6, Y)	A8-23*	A9-23*	See option
CC7X (Common Cathode 7, X)	A8-20*	A9-20*	See option
CC7Y (Common Cathode 7, Y)	A8-24*	A9-24*	See option
GND (Ground)	A100E2	A9-1 A9-2 A9-85 A9-86	None
ID0M6 (Inhibit Driver, Bit 0, Module 6)	A7-25	A9-25	See option
ID0M7 (Inhibit Driver, Bit 0, Module 7)	A7-26	A9-26	See option
ID1M6 (Inhibit Driver, Bit 1, Module 6)	A7-27	A9-27	See option
ID1M7 (Inhibit Driver, Bit 1, Module 7)	A7-28	A9-28	See option
ID2M6 (Inhibit Driver, Bit 2, Module 6)	A7-29	A9-29	See option

Table 7-22. A9 Sense Amplifier Card (Module 6/7, 60000-77777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID2M7 (Inhibit Driver, Bit 2, Module 7)	A7-30	A9-30	See option
ID3M6 (Inhibit Driver, Bit 3, Module 6)	A7-31	A9-31	See option
ID3M7 (Inhibit Driver, Bit 3, Module 7)	A7-32	A9-32	See option
ID4M6 (Inhibit Driver, Bit 4, Module 6)	A7-33	A9-33	See option
ID4M7 (Inhibit Driver, Bit 4, Module 7)	A7-34	A9-34	See option
ID5M6 (Inhibit Driver, Bit 5, Module 6)	A7-35	A9-35	See option
ID5M7 (Inhibit Driver, Bit 5, Module 7)	A7-36	A9-36	See option
ID6M6 (Inhibit Driver, Bit 6, Module 6)	A7-37	A9-37	See option
ID6M7 (Inhibit Driver, Bit 6, Module 7)	A7-38	A9-38	See option
ID7M6 (Inhibit Driver, Bit 7, Module 6)	A7-41	A9-41	See option
ID7M7 (Inhibit Driver, Bit 7, Module 7)	A7-42	A9-42	See option
ID8M6 (Inhibit Driver, Bit 8, Module 6)	A7-43	A9-43	See option
ID8M7 (Inhibit Driver, Bit 8, Module 7)	A7-44	A9-44	See option
ID9M6 (Inhibit Driver, Bit 9, Module 6)	A7-45	A9-45	See option
ID9M7 (Inhibit Driver, Bit 9, Module 7)	A7-46	A9-46	See option
ID10M6 (Inhibit Driver, Bit 10, Module 6)	A7-49	A9-49	See option
ID10M7 (Inhibit Driver, Bit 10, Module 7)	A7-50	A9-50	See option
ID11M6 (Inhibit Driver, Bit 11, Module 6)	A7-51	A9-51	See option
ID11M7 (Inhibit Driver, Bit 11, Module 7)	A7-52	A9-52	See option
ID12M6 (Inhibit Driver, Bit 12, Module 6)	A7-53	A9-53	See option
ID12M7 (Inhibit Driver, Bit 12, Module 7)	A7-54	A9-54	See option

Table 7-22. A9 Sense Amplifier Card (Module 6/7, 60000-77777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID13M6 (Inhibit Driver, Bit 13, Module 6)	A7-55	A9-55	See option
ID13M7 (Inhibit Driver, Bit 13, Module 7)	A7-56	A9-56	See option
ID14M6 (Inhibit Driver, Bit 14, Module 6)	A7-57	A9-57	See option
ID14M7 (Inhibit Driver, Bit 14, Module 7)	A7-58	A9-58	See option
ID15M6 (Inhibit Driver, Bit 15, Module 6)	A7-59	A9-59	See option
ID15M7 (Inhibit Driver, Bit 15, Module 7)	A7-60	A9-60	See option
ID16M6 (Inhibit Driver, Bit 16, Module 6)	A7-61	A9-61	See option
ID16M7 (Inhibit Driver, Bit 16, Module 7)	A7-62	A9-62	See option
MOD6 (Module 6)	A14-63	A9-3	See source
MOD7 (Module 7)	A14-5	A9-4	See source
MSG (Memory Strobe Gate)	A106-19	A9-6	See source
SA0 (Sense Amplifier 0)	A9-15	A13-3	None
SA1 (Sense Amplifier 1)	A9-18	A13-7	None
SA2 (Sense Amplifier 2)	A9-17	A13-11	None
SA3 (Sense Amplifier 3)	A9-20	A13-15	None
SA4 (Sense Amplifier 4)	A9-19	A13-19	None
SA5 (Sense Amplifier 5)	A9-22	A13-23	None
SA6 (Sense Amplifier 6)	A9-21	A13-27	None
SA7 (Sense Amplifier 7)	A9-63	A13-31	None
SA8 (Sense Amplifier 8)	A9-64	A13-35	None
SA9 (Sense Amplifier 9)	A9-65	A13-41	None
SA10 (Sense Amplifier 10)	A9-66	A13-45	None
SA11 (Sense Amplifier 11)	A9-67	A13-51	None
SA12 (Sense Amplifier 12)	A9-68	A13-55	None
SA13 (Sense Amplifier 13)	A9-69	A13-59	None
SA14 (Sense Amplifier 14)	A9-70	A13-63	None
SA15 (Sense Amplifier 15)	A9-71	A13-67	None
SA16 (Sense Amplifier 16)	A9-72	A13-71	None

Table 7-23. A10 Sense Amplifier Card (Module 4/5, 40000-57777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A10-47 A10-48	None
+4.5V	A100E1	A10-39 A10-40	None
+12V	A100TB2-1	A10-13 A10-14	None
-12V	A100TB2-2	A10-73 A10-74	None
C0X (Common 0, X)	A11-9*	A10-9*	See option
C0Y (Common 0, Y)	A11-K*	A10-K*	See option
C1X (Common 1, X)	A11-10*	A10-10*	See option
C1Y (Common 1, Y)	A11-L*	A10-L*	See option
C2X (Common 2, X)	A11-11*	A10-11*	See option
C2Y (Common 2, Y)	A11-M*	A10-M*	See option
C3X (Common 3, X)	A11-12*	A10-12*	See option
C3Y (Common 3, Y)	A11-N*	A10-N*	See option
C4X (Common 4, X)	A11-13*	A10-13*	See option
C4Y (Common 4, Y)	A11-P*	A10-P*	See option
C5X (Common 5, X)	A11-14*	A10-14*	See option
C5Y (Common 5, Y)	A11-R*	A10-R*	See option
C6X (Common 6, X)	A11-15*	A10-15*	See option
C6Y (Common 6, Y)	A11-S*	A10-S*	See option
C7X (Common 7, X)	A11-16*	A10-16*	See option
C7Y (Common 7, Y)	A11-T*	A10-T*	See option
CA0X (Common Anode 0, X)	A11-E*	A10-E*	See option
CA0Y (Common Anode 0, Y)	A11-D*	A10-D*	See option
CA1X (Common Anode 1, X)	A11-U*	A10-U*	See option
CA1Y (Common Anode 1, Y)	A11-C*	A10-C*	See option
CA2X (Common Anode 2, X)	A11-F*	A10-F*	See option
CA2Y (Common Anode 2, Y)	A11-Y*	A10-Y*	See option
CA3X (Common Anode 3, X)	A11-V*	A10-V*	See option
CA3Y (Common Anode 3, Y)	A11-Z*	A10-Z*	See option
CA4X (Common Anode 4, X)	A11-H*	A10-H*	See option
CA4Y (Common Anode 4, Y)	A11-B*	A10-B*	See option
CA5X (Common Anode 5, X)	A11-W*	A10-W*	See option

Table 7-23. A10 Sense Amplifier Card (Module 4/5, 40000-57777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
CA5Y (Common Anode 5, Y)	A11-A*	A10-A*	See option
CA6X (Common Anode 6, X)	A11-J*	A10-J*	See option
CA6Y (Common Anode 6, Y)	A11-AA*	A10-AA*	See option
CA7X (Common Anode 7, X)	A11-X*	A10-X*	See option
CA7Y (Common Anode 7, Y)	A11-BB*	A10-BB*	See option
CC0X (Common Cathode 0, X)	A11-5*	A10-5*	See option
CC0Y (Common Cathode 0, Y)	A11-4*	A10-4*	See option
CC1X (Common Cathode 1, X)	A11-17*	A10-17*	See option
CC1Y (Common Cathode 1, Y)	A11-3*	A10-3*	See option
CC2X (Common Cathode 2, X)	A11-6*	A10-6*	See option
CC2Y (Common Cathode 2, Y)	A11-21*	A10-21*	See option
CC3X (Common Cathode 3, X)	A11-18*	A10-18*	See option
CC3Y (Common Cathode 3, Y)	A11-22*	A10-22*	See option
CC4X (Common Cathode 4, X)	A11-7*	A10-7*	See option
CC4Y (Common Cathode 4, Y)	A11-2*	A10-2*	See option
CC5X (Common Cathode 5, X)	A11-19*	A10-19*	See option
CC5Y (Common Cathode 5, Y)	A11-1*	A10-1*	See option
CC6X (Common Cathode 6, X)	A11-8*	A10-8*	See option
CC6Y (Common Cathode 6, Y)	A11-23*	A10-23*	See option
CC7X (Common Cathode 7, X)	A11-20*	A10-20*	See option
CC7Y (Common Cathode 7, Y)	A11-24*	A10-24*	See option
GND (Ground)	A100E2	A10-1 A10-2 A10-85 A10-86	None
ID0M4 (Inhibit Driver, Bit 0, Module 4)	A12-25	A10-25	See option
ID0M5 (Inhibit Driver, Bit 0, Module 5)	A12-26	A10-26	See option
ID1M4 (Inhibit Driver, Bit 1, Module 4)	A12-27	A10-27	See option
ID1M5 (Inhibit Driver, Bit 1, Module 5)	A12-28	A10-28	See option
ID2M4 (Inhibit Driver, Bit 2, Module 4)	A12-29	A10-29	See option
ID2M5 (Inhibit Driver, Bit 2, Module 5)	A12-30	A10-30	See option

Table 7-23. A10 Sense Amplifier Card (Module 4/5, 40000-57777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID3M4 (Inhibit Driver, Bit 3, Module 4)	A12-31	A10-31	See option
ID3M5 (Inhibit Driver, Bit 3, Module 5)	A12-32	A10-32	See option
ID4M4 (Inhibit Driver, Bit 4, Module 4)	A12-33	A10-33	See option
ID4M5 (Inhibit Driver, Bit 4, Module 5)	A12-34	A10-34	See option
ID5M4 (Inhibit Driver, Bit 5, Module 4)	A12-35	A10-35	See option
ID5M5 (Inhibit Driver, Bit 5, Module 5)	A12-36	A10-36	See option
ID6M4 (Inhibit Driver, Bit 6, Module 4)	A12-37	A10-37	See option
ID6M5 (Inhibit Driver, Bit 6, Module 5)	A12-38	A10-38	See option
ID7M4 (Inhibit Driver, Bit 7, Module 4)	A12-41	A10-41	See option
ID7M5 (Inhibit Driver, Bit 7, Module 5)	A12-42	A10-42	See option
ID8M4 (Inhibit Driver, Bit 8, Module 4)	A12-43	A10-43	See option
ID8M5 (Inhibit Driver, Bit 8, Module 5)	A12-44	A10-44	See option
ID9M4 (Inhibit Driver, Bit 9, Module 4)	A12-45	A10-45	See option
ID9M5 (Inhibit Driver, Bit 9, Module 5)	A12-46	A10-46	See option
ID10M4 (Inhibit Driver, Bit 10, Module 4)	A12-49	A10-49	See option
ID10M5 (Inhibit Driver, Bit 10, Module 5)	A12-50	A10-50	See option
ID11M4 (Inhibit Driver, Bit 11, Module 4)	A12-51	A10-51	See option
ID11M5 (Inhibit Driver, Bit 11, Module 5)	A12-52	A10-52	See option
ID12M4 (Inhibit Driver, Bit 12, Module 4)	A12-53	A10-53	See option
ID12M5 (Inhibit Driver, Bit 12, Module 5)	A12-54	A10-54	See option
ID13M4 (Inhibit Driver, Bit 13, Module 4)	A12-55	A10-55	See option

Table 7-23. A10 Sense Amplifier Card (Module 4/5, 40000-57777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID13M5 (Inhibit Driver, Bit 13, Module 5)	A12-56	A10-56	See option
ID14M4 (Inhibit Driver, Bit 14, Module 4)	A12-57	A10-57	See option
ID14M5 (Inhibit Driver, Bit 14, Module 5)	A12-58	A10-58	See option
ID15M4 (Inhibit Driver, Bit 15, Module 4)	A12-59	A10-59	See option
ID15M5 (Inhibit Driver, Bit 15, Module 5)	A12-60	A10-60	See option
ID16M4 (Inhibit Driver, Bit 16, Module 4)	A12-61	A10-61	See option
ID16M5 (Inhibit Driver, Bit 16, Module 5)	A12-62	A10-62	See option
MOD4 (Module 4)	A14-55	A10-3	See source
MOD5 (Module 5)	A14-59	A10-4	See source
MSG (Memory Strobe Gate)	A106-19	A10-6	See source
SA0 (Sense Amplifier 0)	A10-15	A13-3	None
SA1 (Sense Amplifier 1)	A10-18	A13-7	None
SA2 (Sense Amplifier 2)	A10-17	A13-11	None
SA3 (Sense Amplifier 3)	A10-20	A13-15	None
SA4 (Sense Amplifier 4)	A10-19	A13-19	None
SA5 (Sense Amplifier 5)	A10-22	A13-23	None
SA6 (Sense Amplifier 6)	A10-21	A13-27	None
SA7 (Sense Amplifier 7)	A10-63	A13-31	None
SA8 (Sense Amplifier 8)	A10-64	A13-35	None
SA9 (Sense Amplifier 9)	A10-65	A13-41	None
SA10 (Sense Amplifier 10)	A10-66	A13-45	None
SA11 (Sense Amplifier 11)	A10-67	A13-51	None
SA12 (Sense Amplifier 12)	A10-68	A13-55	None
SA13 (Sense Amplifier 13)	A10-69	A13-59	None
SA14 (Sense Amplifier 14)	A10-70	A13-63	None
SA15 (Sense Amplifier 15)	A10-71	A13-67	None
SA16 (Sense Amplifier 16)	A10-72	A13-71	None

Table 7-24. A19 Sense Amplifier Card (Module 2/3, 20000-37777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A19-47 A19-48	None
+4.5V	A100E1	A19-39 A19-40	None
+12V	A100TB2-1	A19-13 A19-14	None
-12V	A100TB2-2	A19-73 A19-74	None
C0X (Common 0, X)	A18-9*	A19-9*	None
C0Y (Common 0, Y)	A18-K*	A19-K*	None
C1X (Common 1, X)	A18-10*	A19-10*	None
C1Y (Common 1, Y)	A18-L*	A19-L*	None
C2X (Common 2, X)	A18-11*	A19-11*	None
C2Y (Common 2, Y)	A18-M*	A19-M*	None
C3X (Common 3, X)	A18-12*	A19-12*	None
C3Y (Common 3, Y)	A18-N*	A19-N*	None
C4X (Common 4, X)	A18-13*	A19-13*	None
C4Y (Common 4, Y)	A18-P*	A19-P*	None
C5X (Common 5, X)	A18-14*	A19-14*	None
C5Y (Common 5, Y)	A18-R*	A19-R*	None
C6X (Common 6, X)	A18-15*	A19-15*	None
C6Y (Common 6, Y)	A18-S*	A19-S*	None
C7X (Common 7, X)	A18-16*	A19-16*	None
C7Y (Common 7, Y)	A18-T*	A19-T*	None
CA0X (Common Anode 0, X)	A18-E*	A19-E*	None
CA0Y (Common Anode 0, Y)	A18-D*	A19-D*	None
CA1X (Common Anode 1, X)	A18-U*	A19-U*	None
CA1Y (Common Anode 1, Y)	A18-C*	A19-C*	None
CA2X (Common Anode 2, X)	A18-F*	A19-F*	None
CA2Y (Common Anode 2, Y)	A18-Y*	A19-Y*	None
CA3X (Common Anode 3, X)	A18-V*	A19-V*	None
CA3Y (Common Anode 3, Y)	A18-Z*	A19-Z*	None
CA4X (Common Anode 4, X)	A18-H*	A19-H*	None
CA4Y (Common Anode 4, Y)	A18-B*	A19-B*	None
CA5X (Common Anode 5, X)	A18-W*	A19-W*	None

Table 7-24. A19 Sense Amplifier Card (Module 2/3, 20000-37777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
CA5Y (Common Anode 5, Y)	A18-A*	A19-A*	None
CA6X (Common Anode 6, X)	A18-J*	A19-J*	None
CA6Y (Common Anode 6, Y)	A18-AA*	A19-AA*	None
CA7X (Common Anode 7, X)	A18-X*	A19-X*	None
CA7Y (Common Anode 7, Y)	A18-BB*	A19-BB*	None
CC0X (Common Cathode 0, X)	A18-5*	A19-5*	None
CC0Y (Common Cathode 0, Y)	A18-4*	A19-4*	None
CC1X (Common Cathode 1, X)	A18-17*	A19-17*	None
CC1Y (Common Cathode 1, Y)	A18-3*	A19-3*	None
CC2X (Common Cathode 2, X)	A18-6*	A19-6*	None
CC2Y (Common Cathode 2, Y)	A18-21*	A19-21*	None
CC3X (Common Cathode 3, X)	A18-18*	A19-18*	None
CC3Y (Common Cathode 3, Y)	A18-22*	A19-22*	None
CC4X (Common Cathode 4, X)	A18-7*	A19-7*	None
CC4Y (Common Cathode 4, Y)	A18-2*	A19-2*	None
CC5X (Common Cathode 5, X)	A18-19*	A19-19*	None
CC5Y (Common Cathode 5, Y)	A18-1*	A19-1*	None
CC6X (Common Cathode 6, X)	A18-8*	A19-8*	None
CC6Y (Common Cathode 6, Y)	A18-23*	A19-23*	None
CC7X (Common Cathode 7, X)	A18-20*	A19-20*	None
CC7Y (Common Cathode 7, Y)	A18-24*	A19-24*	None
GND (Ground)	A100E2	A19-1 A19-2 A19-85 A19-86	None
ID0M2 (Inhibit Driver, Bit 0, Module 2)	A17-25	A19-25	See option
ID0M3 (Inhibit Driver, Bit 0, Module 3)	A17-26	A19-26	See option
ID1M2 (Inhibit Driver, Bit 1, Module 2)	A17-27	A19-27	See option
ID1M3 (Inhibit Driver, Bit 1, Module 3)	A17-28	A19-28	See option
ID2M2 (Inhibit Driver, Bit 2, Module 2)	A17-29	A19-29	See option
ID2M3 (Inhibit Driver, Bit 2, Module 3)	A17-30	A19-30	See option

Table 7-24. A19 Sense Amplifier Card (Module 2/3, 20000-37777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID3M2 (Inhibit Driver, Bit 3, Module 2)	A17-31	A19-31	See option
ID3M3 (Inhibit Driver, Bit 3, Module 3)	A17-32	A19-32	See option
ID4M2 (Inhibit Driver, Bit 4, Module 2)	A17-33	A19-33	See option
ID4M3 (Inhibit Driver, Bit 4, Module 3)	A17-34	A19-34	See option
ID5M2 (Inhibit Driver, Bit 5, Module 2)	A17-35	A19-35	See option
ID5M3 (Inhibit Driver, Bit 5, Module 3)	A17-36	A19-36	See option
ID6M2 (Inhibit Driver, Bit 6, Module 2)	A17-37	A19-37	See option
ID6M3 (Inhibit Driver, Bit 6, Module 3)	A17-38	A19-38	See option
ID7M2 (Inhibit Driver, Bit 7, Module 2)	A17-41	A19-41	See option
ID7M3 (Inhibit Driver, Bit 7, Module 3)	A17-42	A19-42	See option
ID8M2 (Inhibit Driver, Bit 8, Module 2)	A17-43	A19-43	See option
ID8M3 (Inhibit Driver, Bit 8, Module 3)	A17-44	A19-44	See option
ID9M2 (Inhibit Driver, Bit 9, Module 2)	A17-45	A19-45	See option
ID9M3 (Inhibit Driver, Bit 9, Module 3)	A17-46	A19-46	See option
ID10M2 (Inhibit Driver, Bit 10, Module 2)	A17-49	A19-49	See option
ID10M3 (Inhibit Driver, Bit 10, Module 3)	A17-50	A19-50	See option
ID11M2 (Inhibit Driver, Bit 11, Module 2)	A17-51	A19-51	See option
ID11M3 (Inhibit Driver, Bit 11, Module 3)	A17-52	A19-52	See option
ID12M2 (Inhibit Driver, Bit 12, Module 2)	A17-53	A19-53	See option
ID12M3 (Inhibit Driver, Bit 12, Module 3)	A17-54	A19-54	See option
ID13M2 (Inhibit Driver, Bit 13, Module 2)	A17-55	A19-55	See option

Table 7-24. A19 Sense Amplifier Card (Module 2/3, 20000-37777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID13M3 (Inhibit Driver, Bit 13, Module 3)	A17-56	A19-56	See option
ID14M2 (Inhibit Driver, Bit 14, Module 2)	A17-57	A19-57	See option
ID14M3 (Inhibit Driver, Bit 14, Module 3)	A17-58	A19-58	See option
ID15M2 (Inhibit Driver, Bit 15, Module 2)	A17-59	A19-59	See option
ID15M3 (Inhibit Driver, Bit 15, Module 3)	A17-60	A19-60	See option
ID16M2 (Inhibit Driver, Bit 16, Module 2)	A17-61	A19-61	See option
ID16M3 (Inhibit Driver, Bit 16, Module 3)	A17-62	A19-62	See option
MOD2 (Module 2)	A14-45	A19-3	See source
MOD3 (Module 3)	A14-51	A19-4	See source
MSG (Memory Strobe Gate)	A106-19	A19-6	See source
SA0 (Sense Amplifier 0)	A19-15	A13-3	None
SA1 (Sense Amplifier 1)	A19-18	A13-7	None
SA2 (Sense Amplifier 2)	A19-17	A13-11	None
SA3 (Sense Amplifier 3)	A19-20	A13-15	None
SA4 (Sense Amplifier 4)	A19-19	A13-19	None
SA5 (Sense Amplifier 5)	A19-22	A13-23	None
SA6 (Sense Amplifier 6)	A19-21	A13-27	None
SA7 (Sense Amplifier 7)	A19-63	A13-31	None
SA8 (Sense Amplifier 8)	A19-64	A13-35	None
SA9 (Sense Amplifier 9)	A19-65	A13-41	None
SA10 (Sense Amplifier 10)	A19-66	A13-45	None
SA11 (Sense Amplifier 11)	A19-67	A13-51	None
SA12 (Sense Amplifier 12)	A19-68	A13-55	None
SA13 (Sense Amplifier 13)	A19-69	A13-59	None
SA14 (Sense Amplifier 14)	A19-70	A13-63	None
SA15 (Sense Amplifier 15)	A19-71	A13-67	None
SA16 (Sense Amplifier 16)	A19-72	A13-71	None

Table 7-25. A20 Sense Amplifier Card (Module 0/1, 00002-17777), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A20-47 A20-48	None
+4.5V	A100E1	A20-39 A20-40	None
+12V	A100TB2-1	A20-13 A20-14	None
-12V	A100TB2-2	A20-73 A20-74	None
C0X (Common 0, X)	A21-9*	A20-9*	None
C0Y (Common 0, Y)	A21-K*	A20-K*	None
C1X (Common 1, X)	A21-10*	A20-10*	None
C1Y (Common 1, Y)	A21-L*	A20-L*	None
C2X (Common 2, X)	A21-11*	A20-11*	None
C2Y (Common 2, Y)	A21-M*	A20-M*	None
C3X (Common 3, X)	A21-12*	A20-12*	None
C3Y (Common 3, Y)	A21-N*	A20-N*	None
C4X (Common 4, X)	A21-13*	A20-13*	None
C4Y (Common 4, Y)	A21-P*	A20-P*	None
C5X (Common 5, X)	A21-14*	A20-14*	None
C5Y (Common 5, Y)	A21-R*	A20-R*	None
C6X (Common 6, X)	A21-15*	A20-15*	None
C6Y (Common 6, Y)	A21-S*	A20-S*	None
C7X (Common 7, X)	A21-16*	A20-16*	None
C7Y (Common 7, Y)	A21-T*	A20-T*	None
CA0X (Common Anode 0, X)	A21-E*	A20-E*	None
CA0Y (Common Anode 0, Y)	A21-D*	A20-D*	None
CA1X (Common Anode 1, X)	A21-U*	A20-U*	None
CA1Y (Common Anode 1, Y)	A21-C*	A20-C*	None
CA2X (Common Anode 2, X)	A21-F*	A20-F*	None
CA2Y (Common Anode 2, Y)	A21-Y*	A20-Y*	None
CA3X (Common Anode 3, X)	A21-V*	A20-V*	None
CA3Y (Common Anode 3, Y)	A21-Z*	A20-Z*	None
CA4X (Common Anode 4, X)	A21-H*	A20-H*	None
CA4Y (Common Anode 4, Y)	A21-B*	A20-B*	None
CA5X (Common Anode 5, X)	A21-W*	A20-W*	None

Table 7-25. A20 Sense Amplifier Card (Module 0/1, 00002-17777), Signal List (Continued)

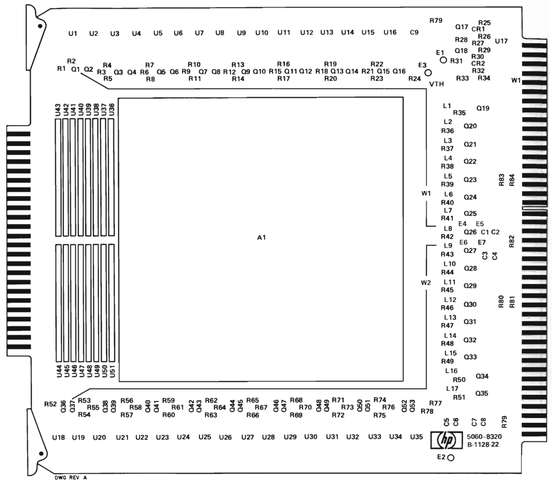
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
CA5Y (Common Anode 5, Y)	A21-A*	A20-A*	None
CA6X (Common Anode 6, X)	A21-J*	A20-J*	None
CA6Y (Common Anode 6, Y)	A21-AA*	A20-AA*	None
CA7X (Common Anode 7, X)	A21-X*	A20-X*	None
CA7Y (Common Anode 7, Y)	A21-BB*	A20-BB*	None
CC0X (Common Cathode 0, X)	A21-5*	A20-5*	None
CC0Y (Common Cathode 0, Y)	A21-4*	A20-4*	None
CC1X (Common Cathode 1, X)	A21-17*	A20-17*	None
CC1Y (Common Cathode 1, Y)	A21-3*	A20-3*	None
CC2X (Common Cathode 2, X)	A21-6*	A20-6*	None
CC2Y (Common Cathode 2, Y)	A21-21*	A20-21*	None
CC3X (Common Cathode 3, X)	A21-18*	A20-18*	None
CC3Y (Common Cathode 3, Y)	A21-22*	A20-22*	None
CC4X (Common Cathode 4, X)	A21-7*	A20-7*	None
CC4Y (Common Cathode 4, Y)	A21-2*	A20-2*	None
CC5X (Common Cathode 5, X)	A21-19*	A20-19*	None
CC5Y (Common Cathode 5, Y)	A21-1*	A20-1*	None
CC6X (Common Cathode 6, X)	A21-8*	A20-8*	None
CC6Y (Common Cathode 6, Y)	A21-23*	A20-23*	None
CC7X (Common Cathode 7, X)	A21-20*	A20-20*	None
CC7Y (Common Cathode 7, Y)	A21-24*	A20-24*	None
GND (Ground)	A100E2	A20-1 A20-2 A20-85 A20-86	None
ID0M0 (Inhibit Driver, Bit 0, Module 0)	A22-25	A20-25	See source
ID0M1 (Inhibit Driver, Bit 0, Module 1)	A22-26	A20-26	See source
ID1M0 (Inhibit Driver, Bit 1, Module 0)	A22-27	A20-27	See source
ID1M1 (Inhibit Driver, Bit 1, Module 1)	A22-28	A20-28	See source
ID2M0 (Inhibit Driver, Bit 2, Module 0)	A22-29	A20-29	See source
ID2M1 (Inhibit Driver, Bit 2, Module 1)	A22-30	A20-30	See source

Table 7-25. A20 Sense Amplifier Card (Module 0/1, 00002-17777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID3M0 (Inhibit Driver, Bit 3, Module 0)	A22-31	A20-31	See source
ID3M1 (Inhibit Driver, Bit 3, Module 1)	A22-32	A20-32	See source
ID4M0 (Inhibit Driver, Bit 4, Module 0)	A22-33	A20-33	See source
ID4M1 (Inhibit Driver, Bit 4, Module 1)	A22-34	A20-34	See source
ID5M0 (Inhibit Driver, Bit 5, Module 0)	A22-35	A20-35	See source
ID5M1 (Inhibit Driver, Bit 5, Module 1)	A22-36	A20-36	See source
ID6M0 (Inhibit Driver, Bit 6, Module 0)	A22-37	A20-37	See source
ID6M1 (Inhibit Driver, Bit 6, Module 1)	A22-38	A20-38	See source
ID7M0 (Inhibit Driver, Bit 7, Module 0)	A22-41	A20-41	See source
ID7M1 (Inhibit Driver, Bit 7, Module 1)	A22-42	A20-42	See source
ID8M0 (Inhibit Driver, Bit 8, Module 0)	A22-43	A20-43	See source
ID8M1 (Inhibit Driver, Bit 8, Module 1)	A22-44	A20-44	See source
ID9M0 (Inhibit Driver, Bit 9, Module 0)	A22-45	A20-45	See source
ID9M1 (Inhibit Driver, Bit 9, Module 1)	A22-46	A20-46	See source
ID10M0 (Inhibit Driver, Bit 10, Module 0)	A22-49	A20-49	See source
ID10M1 (Inhibit Driver, Bit 10, Module 1)	A22-50	A20-50	See source
ID11M0 (Inhibit Driver, Bit 11, Module 0)	A22-51	A20-51	See source
ID11M1 (Inhibit Driver, Bit 11, Module 1)	A22-52	A20-52	See source
ID12M0 (Inhibit Driver, Bit 12, Module 0)	A22-53	A20-53	See source
ID12M1 (Inhibit Driver, Bit 12, Module 1)	A22-54	A20-54	See source
ID13M0 (Inhibit Driver, Bit 13, Module 0)	A22-55	A20-55	See source

Table 7-25. A20 Sense Amplifier Card (Module 0/1, 00002-17777), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ID13M1 (Inhibit Driver, Bit 13, Module 1)	A22-56	A20-56	See source
ID14M0 (Inhibit Driver, Bit 14, Module 0)	A22-57	A20-57	See source
ID14M1 (Inhibit Driver, Bit 14, Module 1)	A22-58	A20-58	See source
ID15M0 (Inhibit Driver, Bit 15, Module 0)	A22-59	A20-59	See source
ID15M1 (Inhibit Driver, Bit 15, Module 1)	A22-60	A20-60	See source
ID16M0 (Inhibit Driver, Bit 16, Module 0)	A22-61	A20-61	See source
ID16M1 (Inhibit Driver, Bit 16, Module 1)	A22-62	A20-62	See source
MOD0 (Module 0)	A14-35	A20-3	See source
MOD1 (Module 1)	A14-41	A20-4	See source
MSG (Memory Strobe Gate)	A106-19	A20-6	See source
SA0 (Sense Amplifier 0)	A20-15	A13-3	None
SA1 (Sense Amplifier 1)	A20-18	A13-7	None
SA2 (Sense Amplifier 2)	A20-17	A13-11	None
SA3 (Sense Amplifier 3)	A20-20	A13-15	None
SA4 (Sense Amplifier 4)	A20-19	A13-19	None
SA5 (Sense Amplifier 5)	A20-22	A13-23	None
SA6 (Sense Amplifier 6)	A20-21	A13-27	None
SA7 (Sense Amplifier 7)	A20-63	A13-31	None
SA8 (Sense Amplifier 8)	A20-64	A13-35	None
SA9 (Sense Amplifier 9)	A20-65	A13-41	None
SA10 (Sense Amplifier 10)	A20-66	A13-45	None
SA11 (Sense Amplifier 11)	A20-67	A13-51	None
SA12 (Sense Amplifier 12)	A20-68	A13-55	None
SA13 (Sense Amplifier 13)	A20-69	A13-59	None
SA14 (Sense Amplifier 14)	A20-70	A13-63	None
SA15 (Sense Amplifier 15)	A20-71	A13-67	None
SA16 (Sense Amplifier 16)	A20-72	A13-71	None



CAUTION

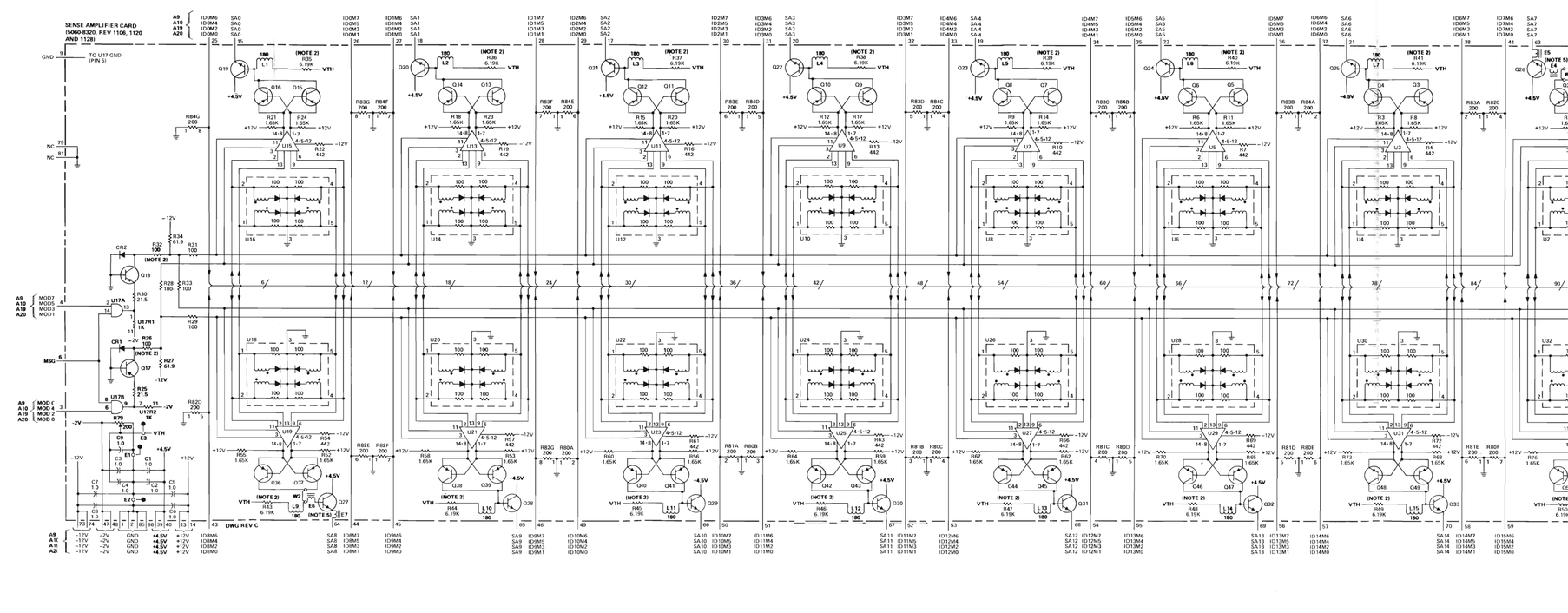
RETURN THIS CIRCUIT CARD TO THE FACTORY FOR REPAIR. FIELD REPLACEMENT OF ANY COMPONENT WILL VOID THE WARRANTY ON THE CARD.

TO AVOID BREAKING WIRES IN CORE STACK A1, DO NOT PRESS ON THE TOP OR BOTTOM OF THE STACK.

INTEGRATED CIRCUIT	PART NO.
U1, 3, 5, 7, 9, 11, 13, 15, 19, 21, 23, 25, 27, 29, 31, 33, 35	1858-0001
U2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34	0960-0111
U17	1820-0956
U36 THROUGH U51	1906-0012 OR 5087-1013

NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. ELECTRICAL VALUES R26, R32, AND R35 THROUGH R51 SELECTED AT FACTORY. NOMINAL VALUES SHOWN.
3. DIODES CR1 AND CR2 MOUNTED WITH CATHODE END AWAY FROM CARD.
4. *THIS CARD MUST NOT BE REPAIRED IN THE FIELD. FIELD REMOVAL OR REPLACEMENT OF ANY COMPONENT VOIDS THE WARRANTY ON THE CARD.*
5. FERRITE CORES E4 THROUGH E7 NOT USED ON CARD REV. 1106.

(Sense amplifier cards with part numbers 02116-63207 and 5060-8320 are interchangeable.)



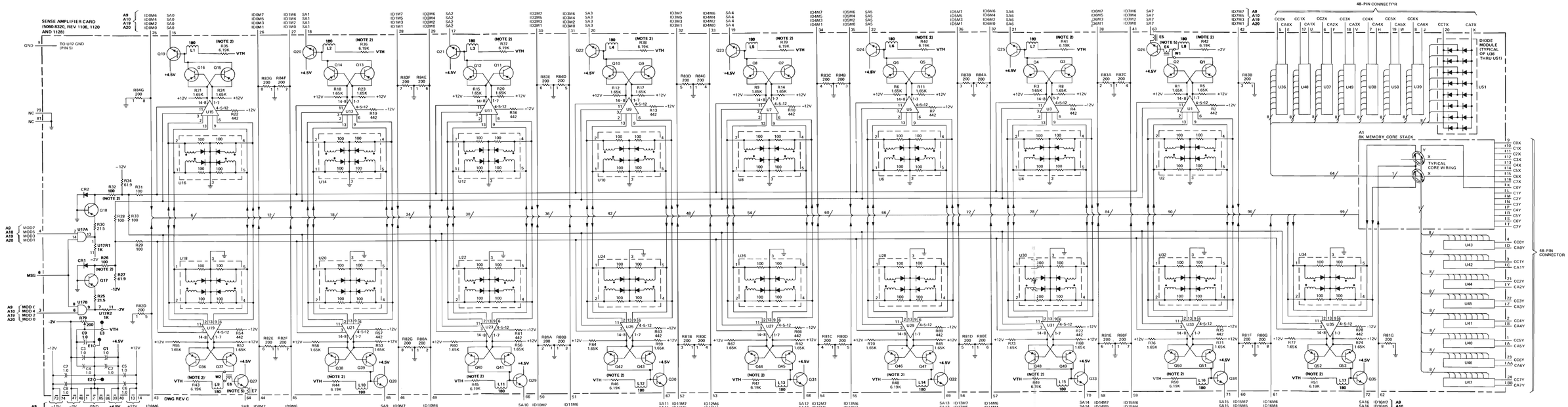
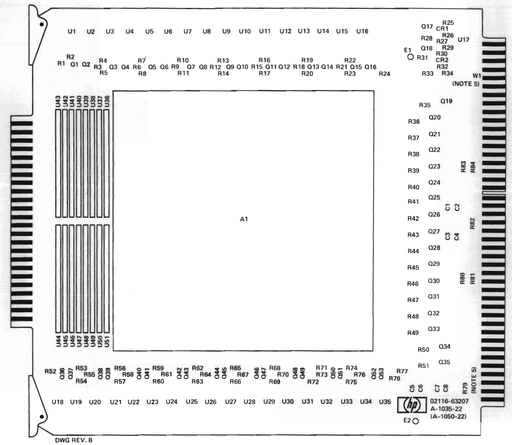


Figure 7-7A. A9, A10, A19, A20 Sense Amplifier Card (5060-8320) Parts Location and Schematic Diagram



CAUTION

DO NOT ATTEMPT REPAIR OF THIS CIRCUIT CARD.
RETURN THE CARD TO THE FACTORY FOR REPAIR.
FIELD REMOVAL OF ANY COMPONENT WILL VOID THE CARD WARRANTY.
TO AVOID BREAKING WIRES IN CORE STACK AT U1, DO NOT DO NOT PRESS ON THE TOP OR BOTTOM OF THE STACK.

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS.
2. ELECTRICAL VALUES MARKED WITH ASTERISK (*) ARE SELECTED AT THE FACTORY. NOMINAL VALUE IS SHOWN.

SELECTED RESISTORS AND VALUES

RESISTORS	SELECTED VALUES
R26 AND R32	100,110,121,130,140,150
R35 THRU R51	6.19K, 7.50K, 8.25K, 9.09K, 10.0K

3. DIODES MOUNTED WITH CATHODE END AWAY FROM CARD.
4. *THIS CARD MUST NOT BE REPAIRED IN THE FIELD. FIELD REMOVAL OR REPLACEMENT OF ANY COMPONENT VOIDS THE WARRANTY ON THE CARD.*
5. THESE COMPONENTS ARE NOT ON CARD REV. 1050.

MICROCIRCUIT	HP TYPE
U1, 3, 5, 7, 9, 11, 13, 15, 19, 21, 23, 25, 27, 29, 31, 33, 35	1858-0061
U2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34	0960-0111
U17	1820-0956
U36 THROUGH U51	1906-0012

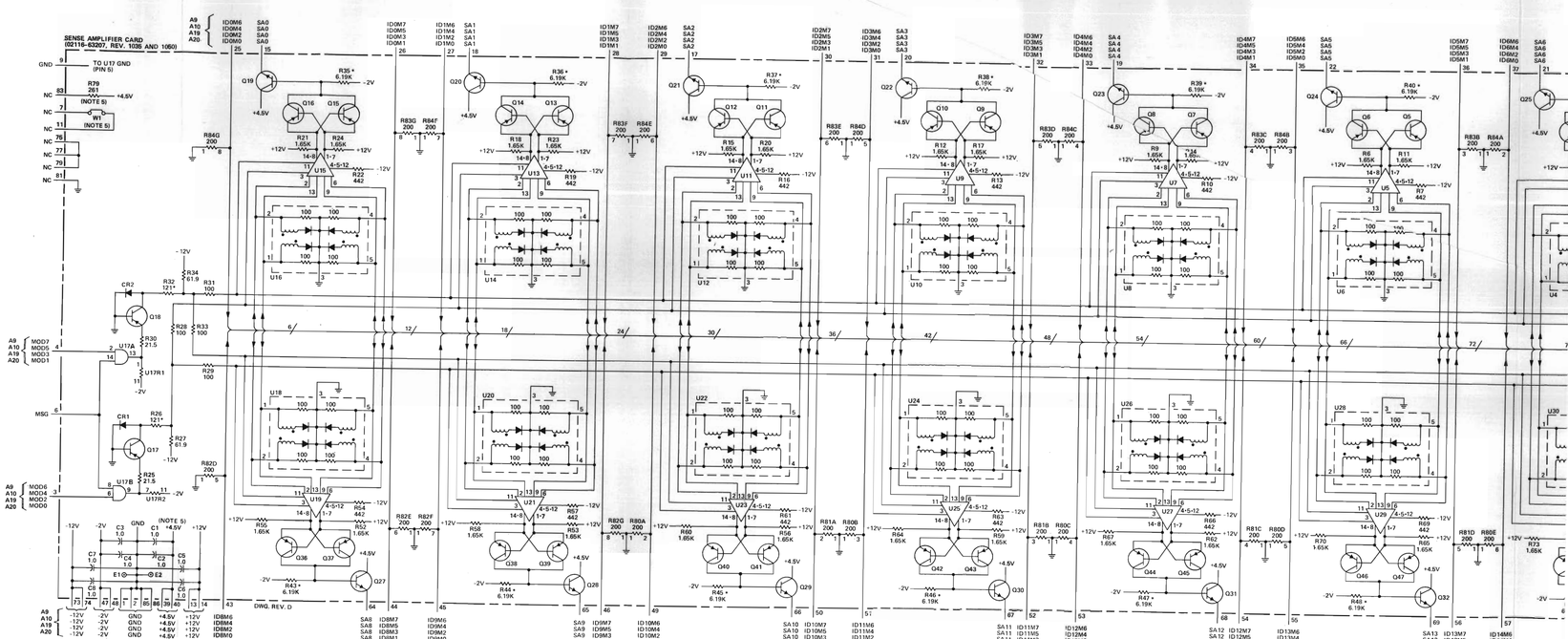


Table 7-26. A13 Memory Data Buffer Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A13-47 A13-48	None
+4.5V	A100E1	A13-39 A13-40	None
GND (Ground)	A100E2	A13-1 A13-2 A13-85 A13-86	None
M5 (Memory Address Bit 5)	A14-26	A13-75	See source
M6 (Memory Address Bit 6)	A14-30	A13-79	See source
MST (Memory Strobe Time)	A106-32	A13-83 A13-36	See source
MIT (Memory Inhibit Time)	A106-25	A13-81	See source
MITX (Memory Inhibit Time, Excludable)	A13-77	A7-4 A12-4 A17-4 A22-4	= MIT · M5 · M6 + MIT · $\overline{M5}$ + MIT · $\overline{M6}$ + MIT · $\overline{M5}$ · $\overline{M6}$ + MIT · M5 + MIT · M6 + MIT · +4.5V
PH1 (Phase 1, Fetch)	A106-41	A13-76	See source
PH2 (Phase 2, Indirect)	A106-37	A13-78	See source
PH3 (Phase 3, Execute)	A106-60	A13-80	See source
PH4 (Phase 4, Interrupt)	A106-13	A13-82	See source
PH5 (Phase 5)	A4-8	A13-84	See option
SA0 (Sense Amplifier 0)	A9-15 A10-15 A19-15 A20-15	A13-3	See source
SA1 (Sense Amplifier 1)	A9-18 A10-18 A19-18 A20-18	A13-7	See source
SA2 (Sense Amplifier 2)	A9-17 A10-17 A19-17 A20-17	A13-11	See source
SA3 (Sense Amplifier 3)	A9-20 A10-20 A19-20 A20-20	A13-15	See source

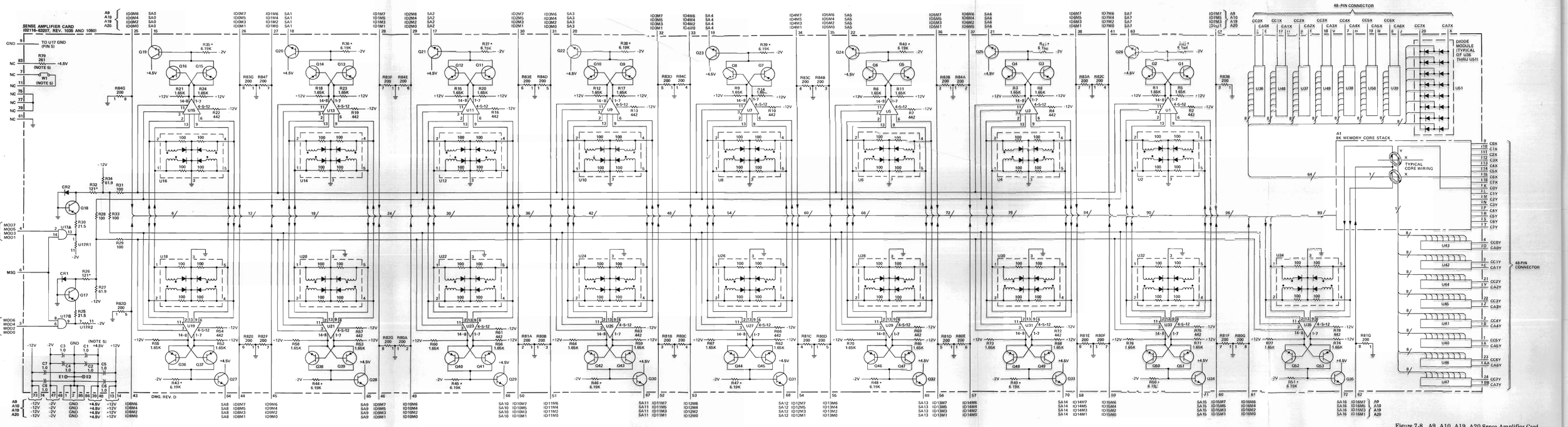


Figure 7-8. A9, A10, A19, A20 Sense Amplifier Card (02116-63207), Parts Location and Schematic Diagram

Table 7-26. A13 Memory Data Buffer Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SA4 (Sense Amplifier 4)	A9-19 A10-19 A19-19 A20-19	A13-19	See source
SA5 (Sense Amplifier 5)	A9-22 A10-22 A19-22 A20-22	A13-23	See source
SA6 (Sense Amplifier 6)	A9-21 A10-21 A19-21 A20-21	A13-27	See source
SA7 (Sense Amplifier 7)	A9-63 A10-63 A19-63 A20-63	A13-31	See source
SA8 (Sense Amplifier 8)	A9-64 A10-64 A19-64 A20-64	A13-35	See source
SA9 (Sense Amplifier 9)	A9-65 A10-65 A19-65 A20-65	A13-41	See source
SA10 (Sense Amplifier 10)	A9-66 A10-66 A19-66 A20-66	A13-45	See source
SA11 (Sense Amplifier 11)	A9-67 A10-67 A19-67 A20-67	A13-51	See source
SA12 (Sense Amplifier 12)	A9-68 A10-68 A19-68 A20-68	A13-55	See source
SA13 (Sense Amplifier 13)	A9-69 A10-69 A19-69 A20-69	A13-59	See source
SA14 (Sense Amplifier 14)	A9-70 A10-70 A19-70 A20-70	A13-63	See source
SA15 (Sense Amplifier 15)	A9-71 A10-71 A19-71 A20-71	A13-67	See source

Table 7-26. A13 Memory Data Buffer Card, Signal List (Continued)

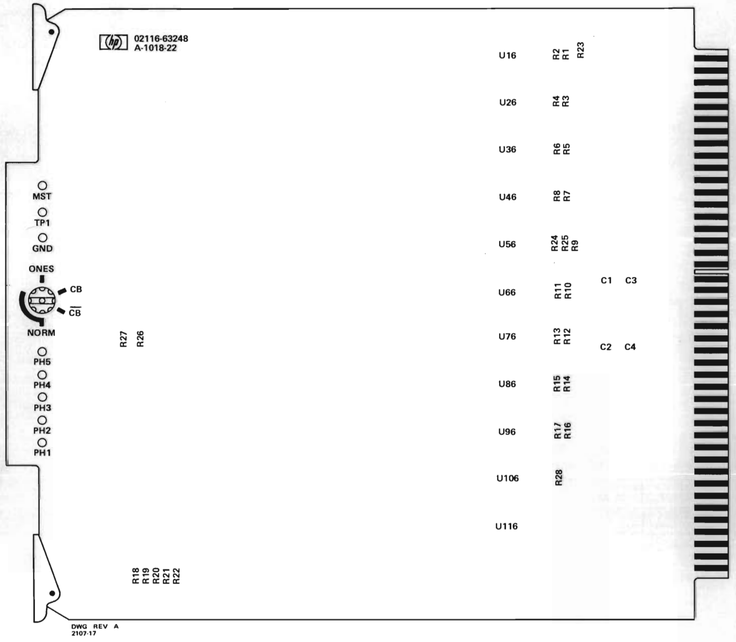
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SA16 (Sense Amplifier 16)	A9-72 A10-72 A19-72 A20-72	A13-71	See source
ST0 (Set T-Register Bit 0)	A13-5	A105-49	= MST · SA0
ST0 GND (Set T-Register Bit 0, Ground Return)	A13-6	A105-1	None
ST1 (Set T-Register Bit 1)	A13-9	A105-4	= MST · SA1
ST1 GND (Set T-Register Bit 1, Ground Return)	A13-10	A105-2	None
ST2 (Set T-Register Bit 2)	A13-13	A105-52	= MST · SA2
ST2 GND (Set T-Register Bit 2, Ground Return)	A13-14	A105-2	None
ST3 (Set T-Register Bit 3)	A13-17	A105-11	= MST · SA3
ST3 GND (Set T-Register Bit 3, Ground Return)	A13-18	A105-1	None
ST4 (Set T-Register Bit 4)	A13-21	A104-49	= MST · SA4
ST4 GND (Set T-Register Bit 4, Ground Return)	A13-22	A104-1	None
ST5 (Set T-Register Bit 5)	A13-25	A104-2	= MST · SA5
ST5 GND (Set T-Register Bit 5, Ground Return)	A13-26	A104-2	None
ST6 (Set T-Register Bit 6)	A13-29	A104-52	= MST · SA6
ST6 GND (Set T-Register Bit 6, Ground Return)	A13-30	A104-2	None
ST7 (Set T-Register Bit 7)	A13-33	A104-11	= MST · SA7
ST7 GND (Set T-Register Bit 7, Ground Return)	A13-34	A104-1	None
ST8 (Set T-Register Bit 8)	A13-37	A103-49	= MST · SA8
ST8 GND (Set T-Register Bit 8, Ground Return)	A13-38	A103-1	None
ST9 (Set T-Register Bit 9)	A13-43	A103-2	= MST · SA9
ST9 GND (Set T-Register Bit 9, Ground Return)	A13-44	A103-2	None
ST10 (Set T-Register Bit 10)	A13-49	A103-52	= MST · SA10
ST10 GND (Set T-Register Bit 10, Ground Return)	A13-50	A103-2	None

Table 7-26. A13 Memory Data Buffer Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ST11 (Set T-Register Bit 11)	A13-53	A103-11	= MST · SA11
ST11 GND (Set T-Register Bit 11, Ground Return)	A13-54	A103-1	None
ST12 (Set T-Register Bit 12)	A13-57	A102-49	= MST · SA12
ST12 GND (Set T-Register Bit 12, Ground Return)	A13-58	A102-1	None
ST13 (Set T-Register Bit 13)	A13-61	A102-4	= MST · SA13
ST13 GND (Set T-Register Bit 13, Ground Return)	A13-62	A102-2	None
ST14 (Set T-Register Bit 14)	A13-65	A102-52	= MST · SA14
ST14 GND (Set T-Register Bit 14, Ground Return)	A13-66	A102-2	None
ST15 (Set T-Register Bit 15)	A13-69	A102-11	= MST · SA15
ST15 GND (Set T-Register Bit 15, Ground Return)	A13-70	A102-1	None
ST16 (Set T-Register Bit 16)	A13-73	A15-60	= MST · SA16
ST16 GND (Set T-Register Bit 16, Ground Return)	A13-74	A15-86	None
STR (Store Instruction)	A107-64	A13-46	See source
STRX (Store, Excludable)	A13-42	A106-81	= STR · +4.5V

Table 7-27. A13 Memory Data Buffer Card (02116-63248), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C4	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X9020A2-DYS
R1 thru R17,25,27,28	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R18 thru R23	0683-2015	Resistor, Fxd, Comp, 2000 ohms, 5%, 1/4W	01121	CB2025
R24	0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4W	01121	CB1025
R26	0683-4715	Resisotr, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715
S1	3100-2687	Switch	28480	3100-2687
U16,26,36,46,56,66,76,86, 96,106	1820-0956	Integrated Circuit, CTL	07263	SL3459
U116	1820-0952	Integrated Circuit, CTL	07263	SL3455



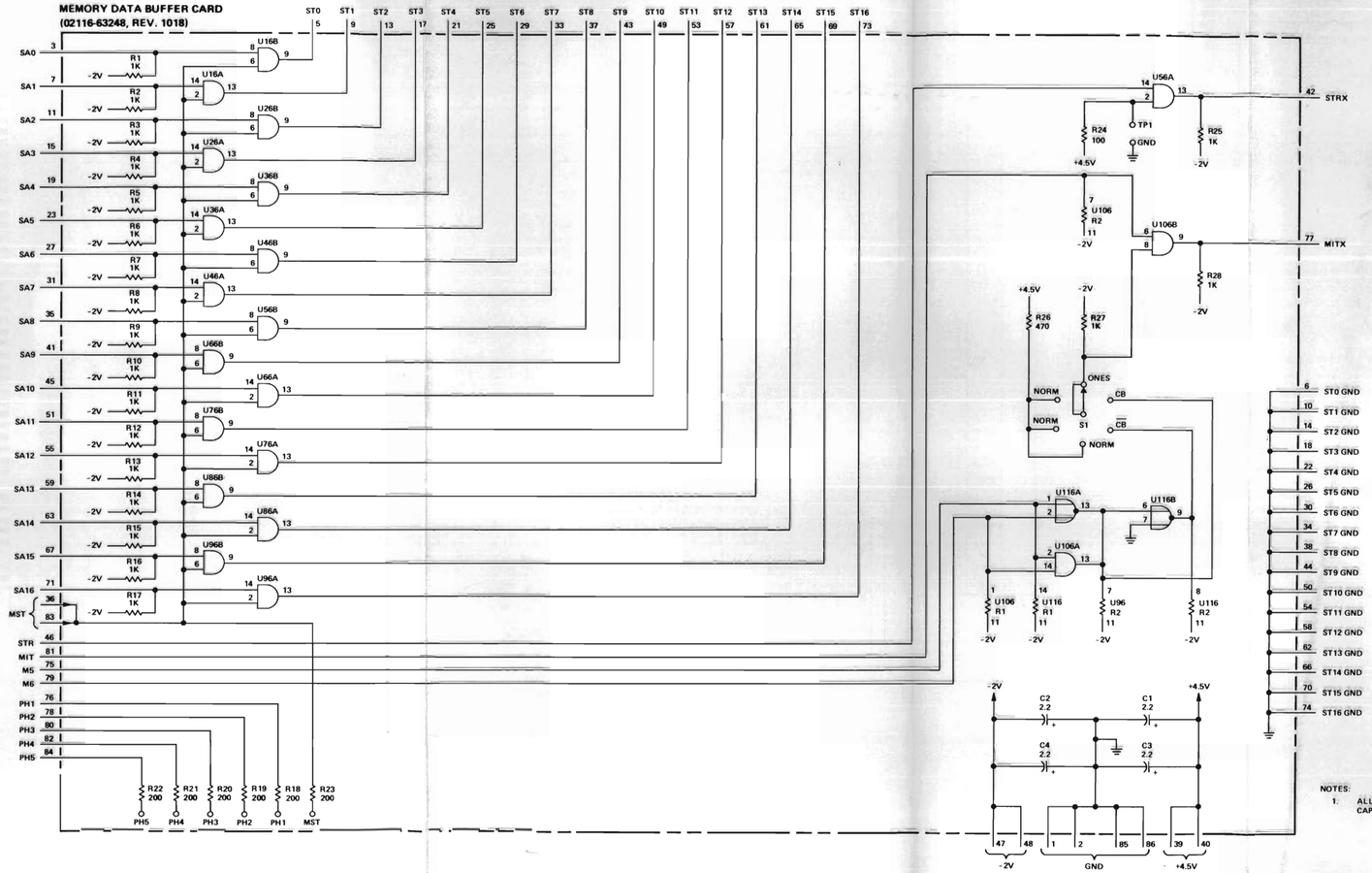


Figure 7-9. A13 Memory Data Buffer Card (02116-63248), Parts Location and Schematic Diagram

Table 7-28. A14 Memory Address Decoder Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A14-47 A14-48	None
+4.5V	A100E1	A14-39 A14-40	None
$\overline{\text{CMF}}$ ("not" Complement Function)	A14-79	A102-64 A103-64 A104-64 A105-64	= $\overline{\text{CMFE}} \cdot \overline{\text{CMFH}}$
CMFB ("not" Complement Function, Buffered)	A110-72	A14-80	See option
$\overline{\text{CMFE}}$ ("not" Complement Function)	A107-65	A14-81	See source
$\overline{\text{EOF}}$ ("not" Exclusive OR Function)	A14-75	A102-76 A103-76 A104-76 A105-76	= $\overline{\text{EOFE}} \cdot \overline{\text{EOFH}}$
EOFB (Exclusive OR Function, Buffered)	A110-26	A14-82	See option
$\overline{\text{EOFE}}$ ("not" Exclusive OR Function)	A107-67	A14-83	See source
EPH (Enable Phase)	A14-72	A106-14	= $\overline{\text{PH5}}$ + $\overline{\text{IIR}}$
GND (Ground)	A100E2	A14-1 A14-2 A14-85 A14-86	None
IIR (Inhibit Instruction Register)	A109-77	A14-71	See option
LPS (Loader Protect Switch Output)	A101-82	A14-31	None
M0 (Memory Address Bit 0)	A1-41 A2-41 A14-6	A8-35 A11-35 A18-35 A21-35	= MR0 · $\overline{\text{PH5}}$ + DMA option signal
M1 (Memory Address Bit 1)	A1-46 A2-46 A14-10	A8-36 A11-36 A18-36 A21-36	= MR1 · $\overline{\text{PH5}}$ + DMA option signal
M2 (Memory Address Bit 2)	A1-45 A2-45 A14-14	A8-37 A11-37 A18-37 A21-37	= MR2 · $\overline{\text{PH5}}$ + DMA option signal
M3 (Memory Address Bit 3)	A1-55 A2-55 A14-18	A8-33 A11-33 A18-33 A21-33	= MR3 · $\overline{\text{PH5}}$ + DMA option signal

Table 7-28. A14 Memory Address Decoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
M4 (Memory Address Bit 4)	A1-65 A2-65 A14-22	A8-32 A11-32 A18-32 A21-32	= MR4 · $\overline{PH5}$ + DMA option signal
M5 (Memory Address Bit 5)	A1-63 A2-63 A14-26	A8-31 A11-31 A18-31 A21-31	= MR5 · $\overline{PH5}$ + DMA option signal
M6 (Memory Address Bit 6)	A1-71 A2-71 A14-30	A8-49 A11-49 A18-49 A21-49	= MR6 · $\overline{PH5}$ + DMA option signal
M7 (Memory Address Bit 7)	A1-72 A2-72 A14-34	A8-52 A11-52 A18-52 A21-52	= MR7 · $\overline{PH5}$ + DMA option signal
M8 (Memory Address Bit 8)	A1-83 A2-83 A14-38	A8-51 A11-51 A18-51 A21-51	= MR8 · $\overline{PH5}$ + DMA option signal
M9 (Memory Address Bit 9)	A1-82 A2-82 A14-44	A8-53 A11-53 A18-53 A21-53	= MR9 · $\overline{PH5}$ + DMA option signal
M10 (Memory Address Bit 10)	A1-6 A2-6 A14-50	A8-56 A11-56 A18-56 A21-56	= MR10 · $\overline{PH5}$ + DMA option signal
M11 (Memory Address Bit 11)	A1-10 A2-10 A14-54	A8-55 A11-55 A18-55 A21-55	= MR11 · $\overline{PH5}$ + DMA option signal
M12 (Memory Address Bit 12)	A1-12 A2-12 A14-58	A14-58	= MR12 · $\overline{PH5}$ + DMA option signal
M13 (Memory Address Bit 13)	A1-16 A2-16 A14-62	A18-23	= MR13 · $\overline{PH5}$ + DMA option signal
M14 (Memory Address Bit 14)	A1-7 A2-7 A14-66	A11-23	= MR14 · $\overline{PH5}$ + DMA option signal
MMD13 (Memory Module Decode Bit 13)	A18-25	A14-19	See option
MMD14 (Memory Module Decode Bit 14)	A11-25	A14-23	See option
MOD0 (Module 0)	A14-35	A20-3 A22-6	= $\overline{MMD14}$ · $\overline{MMD13}$ · $\overline{MR12}$ · $\overline{PH5}$ · $\overline{MPT}$ + MMD14 · MMD13 · $\overline{MR12}$ · $\overline{PH5}$ · MPT3 + $\overline{MMD14}$ · $\overline{MMD13}$ · $\overline{M12}$ · PH5 · $\overline{MPT}$ + MMD14 · MMD13 · $\overline{M12}$ · PH5 · MPT3

Table 7-28. A14 Memory Address Decoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
$\overline{\text{MOD0/1}}$ ("not" Module 0 or 1)	A14-9	A21-46	= MOD0 + MOD1
MOD1 (Module 1)	A14-41	A20-4 A22-12	= $\overline{\text{MMD14}} \cdot \overline{\text{MMD13}} \cdot \text{MR12} \cdot \overline{\text{PH5}} \cdot \overline{\text{MPT}}$ + MMD14 · MMD13 · MR12 · $\overline{\text{PH5}}$ · MPT3 + $\overline{\text{MMD14}} \cdot \overline{\text{MMD13}} \cdot \text{M12} \cdot \text{PH5} \cdot \overline{\text{MPT}}$ + MMD14 · MMD13 · M12 · PH5 · MPT3
MOD2 (Module 2)	A14-45	A17-6 A19-3	= $\overline{\text{MMD14}} \cdot \text{MMD13} \cdot \overline{\text{MR12}} \cdot \overline{\text{PH5}} \cdot \overline{\text{MPT}}$ + MMD14 · MMD13 · M12 · PH5 · MPT
MOD2/3 ("not" Module 2 or 3)	A14-13	A18-46	= MOD2 + MOD3
MOD3 (Module 3)	A14-51	A17-12 A19-4	= $\overline{\text{MMD14}} \cdot \text{MMD13} \cdot \text{MR12} \cdot \overline{\text{PH5}} \cdot \overline{\text{MPT}}$ + $\overline{\text{MMD14}} \cdot \text{MMD13} \cdot \text{M12} \cdot \text{PH5} \cdot \overline{\text{MPT}}$
MOD4 (Module 4)	A14-55	A10-3 A12-6	= MMD14 · $\overline{\text{MMD13}} \cdot \overline{\text{MR12}} \cdot \overline{\text{PH5}} \cdot \overline{\text{MPT}}$ + MMD14 · $\overline{\text{MMD13}} \cdot \overline{\text{M12}} \cdot \text{PH5} \cdot \overline{\text{MPT}}$
MOD4/5 ("not" Module 4 or 5)	A14-17	A11-46	= MOD4 + MOD5
MOD5 (Module 5)	A14-59	A10-4 A12-12	= MMD14 · $\overline{\text{MMD13}} \cdot \text{MR12} \cdot \overline{\text{PH5}} \cdot \overline{\text{MPT}}$ + MMD14 · $\overline{\text{MMD13}} \cdot \text{M12} \cdot \text{PH5} \cdot \overline{\text{MPT}}$
MOD6 (Module 6)	A14-63	A7-6 A9-3	= MMD14 · MMD13 · $\overline{\text{MR12}} \cdot \overline{\text{PH5}} \cdot \overline{\text{MPT}}$ + MMD14 · MMD13 · $\overline{\text{M12}} \cdot \text{PH5} \cdot \overline{\text{MPT}}$
$\overline{\text{MOD6/7}}$ ("not" Module 6 or 7)	A14-21	A8-46	= MOD6 + MOD7
MOD7 (Module 7)	A14-5	A7-12 A9-4	= MMD14 · MMD13 · MR12 · $\overline{\text{PH5}} \cdot \overline{\text{MPT}}$ + MMD14 · MMD13 · M12 · PH5 · $\overline{\text{MPT}}$
MPT (Memory Protect)	A14-25	A15-34	= LPS · MR6 · MR7 · MR8 · MR9 · MR10 · MR11 · $\overline{\text{PH5}}$ · MR12 · $\overline{\text{MMD13}} \cdot \overline{\text{MMD14}}$ · MPT1 + LPS · MR6 · MR7 · MR8 · MR9 · MR10 · MR11 · $\overline{\text{PH5}}$; MR12 · MMD13 · $\overline{\text{MMD14}}$ · MPT2 + LPS · MR6 · MR7 · MR8 · MR9 · MR10 · MR11 · $\overline{\text{PH5}}$ · MR12 · $\overline{\text{MMD13}}$ · MMD14 · MPT3 + LPS · MR6 · MR7 · MR8 · MR9 · MR10 · MR11 · $\overline{\text{PH5}}$ · MR12 · MMD13 · MMD14 · MPT4 + LPS · M6 · M7 · M8 · M9 · M10 · M11 · PH5 · M12 · $\overline{\text{MMD13}} \cdot \overline{\text{MMD14}}$ · MPT1 + LPS · M6 · M7 · M8 · M9 · M10 · M11 · PH5 · M12 · MMD13 · $\overline{\text{MMD14}}$ · MPT2 + LPS · M6 · M7 · M8 · M9 · M10 · M11 · PH5 · M12 · $\overline{\text{MMD13}}$ · MMD14 · MPT3 + LPS · M6 · M7 · M8 · M9 · M10 · M11 · PH5 · M12 · MMD13 · MMD14 · MPT4
MPT1 (Memory Protect 8K)	A21-27	A14-3	See source
MPT2 (Memory Protect 16K)	A18-27	A14-7	See option
MPT3 (Memory Protect 24K)	A11-27	A14-11	See option
MPT4 (Memory Protect 32K)	A8-27	A14-15	See option
MR0 (M-Register Bit 0)	A105-68	A14-4	See source

Table 7-28. A14 Memory Address Decoder Card, Signal List (Continued)

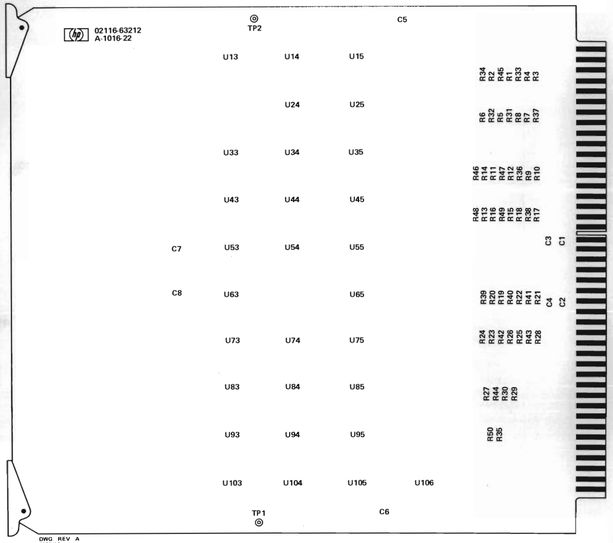
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
MR1 (M-Register Bit 1)	A105-18	A14-8	See source
MR2 (M-Register Bit 2)	A105-65	A14-12	See source
MR3 (M-Register Bit 3)	A105-25	A14-16	See source
MR4 (M-Register Bit 4)	A104-68	A14-20	See source
MR5 (M-Register Bit 5)	A104-18	A14-24	See source
MR6 (M-Register Bit 6)	A104-65	A14-28	See source
MR7 (M-Register Bit 7)	A104-25	A14-32	See source
MR8 (M-Register Bit 8)	A103-68	A14-36	See source
MR9 (M-Register Bit 9)	A103-18	A14-42	See source
MR10 (M-Register Bit 10)	A103-65	A14-46	See source
MR11 (M-Register Bit 11)	A103-25	A14-52	See source
MR12 (M-Register Bit 12)	A102-68	A14-56	See source
MR13 (M-Register Bit 13)	A102-18	A14-60	See source
MR14 (M-Register Bit 14)	A102-65	A14-64	See source
MRT2 (Memory Read Time 2)	A106-26	A14-33	See source
MWT2 (Memory Write Time 2)	A106-20	A14-27	See source
P123 (Phase 1, 2, or 3)	A106-23 A109-13	A14-68	See source or option
P123G (Phase 1, Phase 2, or Phase 3, with "not" Phase 5)	A14-65	A108-69	= P123 · $\overline{PH5}$
PH5 (Phase 5)	A4-8	A14-69	See option
$\overline{SL14}$ ("not" Shift Left, Bit 14)	A14-74	A102-82	= $\overline{SL14E}$ · $\overline{SL14B}$
SL14B ("not" Shift Left, Bit 14, Buffered)	A109-49	A14-84	See option
$\overline{SL14E}$ ("not" Shift Left, Bit 14)	A108-38	A14-67	See source
$\overline{SLM}$ ("not" Shift Left Magnitude)	A14-77	A102-80 A103-41 A103-80 A103-82 A104-41 A104-80 A104-82 A105-41 A105-80 A105-82	= $\overline{SLME}$ · $\overline{SLMB}$

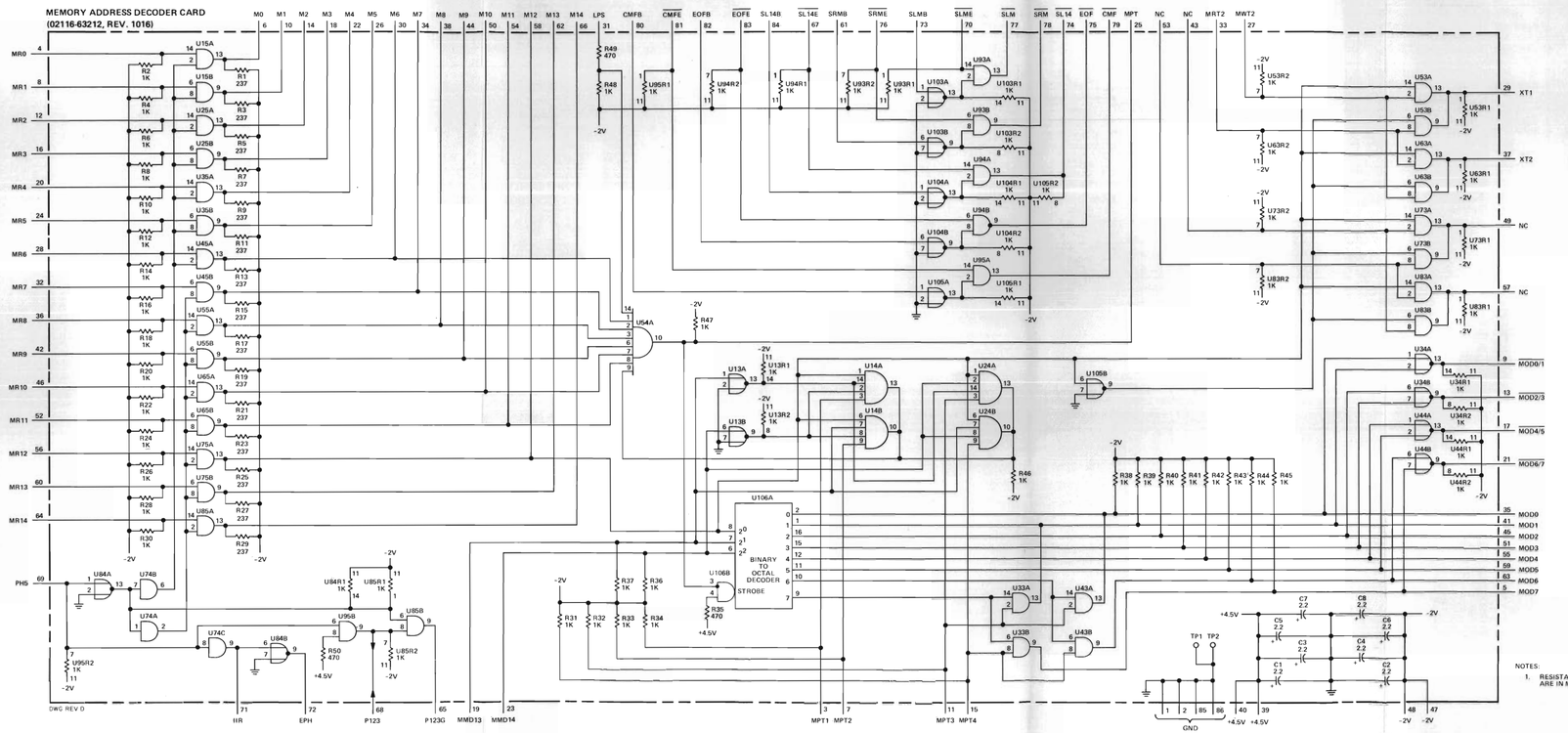
Table 7-28. A14 Memory Address Decoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SLMB (Shift Left Magnitude, Buffered)	A109-44	A14-73	See option
$\overline{\text{SLME}}$ ("not" Shift Left Magnitude)	A108-8	A14-70	See source
$\overline{\text{SRM}}$ ("not" Shift Right Magnitude)	A14-78	A102-74 A102-83 A103-74 A103-83 A104-74 A104-83 A105-74	$= \overline{\text{SRME}} \cdot \overline{\text{SRMB}}$
SRMB (Shift Right Magnitude Buffered)	A109-41	A14-61	See option
$\overline{\text{SRME}}$ ("not" Shift Right Magnitude, Buffered)	A108-32	A14-76	See source
XT1 (X-Drive Time 1)	A14-29	A8-30 A8-38 A11-30 A11-38 A18-30 A18-38 A21-30 A21-38	$= \text{MWT2} \cdot \text{M12}$ $+ \text{MRT2} \cdot \overline{\text{M12}}$
XT2 (X-Drive Time 2)	A14-37	A8-29 A8-34 A11-29 A11-34 A18-29 A18-34 A21-29 A21-34	$= \text{MWT2} \cdot \overline{\text{M12}}$ $+ \text{MRT2} \cdot \text{M12}$

Table 7-29. A14 Memory Address Decoder Card (02116-63212), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C8	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X902A2-DYS
R1,3,5,7,9,11,13,15,17,19, 21,23,25,27,29	0698-3442	Resistor, Fxd, Flm, 237 ohms, 1%, 1/8W	28480	0698-3442
R2,4,6,8,10,12,14,16,18,20, 22,24,26,28,R30 thru R34, R36 thru R48	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R35,49,50	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715
U13,34,44,84,103,104,105	1820-0187	Integrated Circuit	28480	1820-0187
U14,24	1820-0954	Integrated Circuit, CTL	07263	SL3457
U15,25,33,35,43,45,53,55, 63,65,73,75,83,85,U93 thru U95	1820-0186	Integrated Circuit	28480	1820-0186
U54	1820-0955	Integrated Circuit, CTL	07263	SL3458
U74	1820-0965	Integrated Circuit, CTL	07263	SL3462
U106	1820-0482	Integrated Circuit	28480	1820-0482





NOTES:
1. RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.

Figure 7-10. A14 Memory Address Decoder Card (02116-63212), Parts Location and Schematic Diagram

Table 7-30. A15 Parity Error Interrupt Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A15-47 A15-48	None
+4.5V	A100E1	A15-39 A15-40	None
AAF (A-Addressable FF, set-side output	A108-77	A15-49	See source
BAF (B-Addressable FF, set-side output	A108-80	A15-50	See source
CLF (Clear Flag)	A108-19 A4-14 A109-24	A15-51	See source or option
ENF (Enable Flag)	A201-67	A15-71	See source
GND (Ground)	A100E2	A15-1 A15-2 A15-85 A15-86	None
HIN (Halt Instruction)	A108-26 A15-69	A106-66 A16-55	See source or option
IAK (Interrupt Acknowledge)	A201-77	A15-38	See source
INT (Interrupt)	A6-28 A15-79 A16-31 A202-3	A106-44	See source or option
IOBI 15 (Input/Output Bus, Input Bit 15)	A102-27	A15-28	See source
IOG (Input/Output Instruction)	A107-6	A15-59	See source
IOI (Input/Output, Input)	A108-44 A4-81 A4-84	A15-15	See source or option
IRQ5 (Interrupt Request 5)	A16-35 A215-33 A216-6 A210-58	A15-77	See option
ISZ (Increment, skip if Zero)	A107-76	A15-44	See source
MPC (Memory Protect Control)	A16-25	A15-63	See option
MPT (Memory Protect)	A14-25	A15-34	See source
MWL (Memory Write Level)	A106-33	A15-54	See source

Table 7-30. A15 Parity Error Interrupt Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
P123 (Phase 1, Phase 2, or Phase 3)	A106-23 A109-13	A15-52	See source or option
PEH (Parity Error Halt)	A15-62	A106-57	See option
PEI (Parity Error Indicator)	A15-61	A106-7	See option
PH5 (Phase 5, DMA)	A4-8	A15-8	See option
POPIO (Power On Pulse to I/O)	A106-61	A15-45	See source
PRH5/PRL4 (Priority High Select Code 5/Priority Low Select Code 4)	A6-3	A15-25	See source
PRH6/PRL5 (Priority High Select Code 6/Priority Low Select Code 5)	A15-27 A16-51	A1-33 A201-76 A201-82	See option
RPB (Reset Parity Bit)	A106-27	A15-46	See source
RSDS (Reset, Double Store Operation)	A16-15	A15-72	See source
SCL5 (Select Code Least Significant Digit, Octal 5)	A202-52	A15-9	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A15-7	See source
SIR (Service Interrupt Request)	A201-35	A15-37	See source
ST16 (Set T-Register Bit 16)	A13-73	A15-60	See source
ST16 GND (Set T-Register Bit 16 Ground)	A13-74	A15-86	See source
STF (Set Flag)	A108-5 A109-15	A15-18	See source or option
T3 (Time Period 3)	A106-63	A15-23	See source
T7 (Time Period 7)	A106-18	A15-26	See source
TR0 (T-Register Bit 0)	A105-58	A15-84	See source
$\overline{\text{TR0}}$ ("not" T-Register Bit 0)	A105-54	A15-82	See source
TR1 (T-Register Bit 1)	A105-9	A15-83	See source

Table 7-30. A15 Parity Error Interrupt Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
$\overline{TR1}$ ("not" T-Register Bit 1)	A105-10	A15-81	See source
TR2 (T-Register Bit 2)	A105-56	A15-76	See source
$\overline{TR2}$ ("not" T-Register Bit 2)	A105-53	A15-74	See source
TR3 (T-Register Bit 3)	A105-16	A15-75	See source
$\overline{TR3}$ ("not" T-Register Bit 3)	A105-15	A15-73	See source
TR4 (T-Register Bit 4)	A104-58	A15-68	See source
$\overline{TR4}$ ("not" T-Register Bit 4)	A104-54	A15-66	See source
TR5 (T-Register Bit 5)	A104-9	A15-67	See source
$\overline{TR5}$ ("not" T-Register Bit 5)	A104-10	A15-65	See source
TR6 (T-Register Bit 6)	A104-56	A15-58	See source
$\overline{TR6}$ ("not" T-Register Bit 6)	A104-53	A15-56	See source
TR7 (T-Register Bit 7)	A104-16	A15-57	See source
$\overline{TR7}$ ("not" T-Register Bit 7)	A104-15	A15-55	See source
TR8 (T-Register Bit 8)	A103-58	A15-32	See source
$\overline{TR8}$ ("not" T-Register Bit 8)	A103-54	A15-30	See source
TR9 (T-Register Bit 9)	A103-9	A15-31	See source
$\overline{TR9}$ ("not" T-Register Bit 9)	A103-10	A15-29	See source
TR10 (T-Register Bit 10)	A103-56	A15-22	See source
$\overline{TR10}$ ("not" T-Register Bit 10)	A103-53	A15-20	See source
TR11 (T-Register Bit 11)	A103-16	A15-21	See source
$\overline{TR11}$ ("not" T-Register Bit 11)	A103-15	A15-19	See source
TR12 (T-Register Bit 12)	A102-58	A15-14	See source
$\overline{TR12}$ ("not" T-Register Bit 12)	A102-54	A15-12	See source

Table 7-30. A15 Parity Error Interrupt Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TR13 (T-Register Bit 13)	A102-9	A15-13	See source
$\overline{\text{TR13}}$ ("not" T-Register Bit 13)	A102-10	A15-11	See source
TR14 (T-Register Bit 14)	A102-56	A15-6	See source
$\overline{\text{TR14}}$ ("not" T-Register Bit 14)	A102-53	A15-4	See source
TR15 (T-Register Bit 15)	A102-16	A15-5	See source
$\overline{\text{TR15}}$ ("not" T-Register Bit 15)	A102-15	A15-3	See source
$\overline{\text{TR16}}$ ("not" T-Register Bit 16)	A15-53	A7-7 A12-7 A17-7 A22-7	See option
TSA (Time Strobe A)	A106-67	A15-17	See source

Table 7-31. A16 Memory Protect Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A16-47 A16-48	None
+4.5V	A100E1	A16-39 A16-40	None
AAF (A-Addressable FF, set-side output)	A108-77	A16-17	See source
BAF (B-Addressable FF, set-side output)	A108-80	A16-13	See source
GND (Ground)	A100E2	A16-1 A16-2 A16-85 A16-86	None
HIN (Halt Instruction)	A15-69 A108-26	A16-55	See source or option
IAK (Interrupt Acknowledge)	A201-77	A16-56	See source
IEN6 (Interrupt Enable)	A201-10	A16-53	See source
IIR (Inhibit Instruction Register)	A109-77	A16-69	See option
INT (Interrupt)	A6-28 A15-79 A16-31 A202-3	A106-44	See source or option
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI0 FF + IOGE : IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI1 FF + IOGE · IOI · SC · DATA BIT 1
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30	A105-33	= DMA option signal + MP option signal + SWR2 · ISR (Continued on next page)

Table 7-31. A16 Memory Protect Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOBI 2 (Continued)	A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54		+ IOGE(B) · IOI · SCM0 · SCL4 · CI2 FF + IOGE · IOI · SC · DATA BIT 2
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI3 FF + IOGE · IOI · SC · DATA BIT 3
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI4 FF + IOGE · IOI · SC · DATA BIT 4
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI5 FF + IOGE · IOI · SC · DATA BIT 5
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	= DMA option signal + MP option signal + SWR6 · ISR + IOGE · IOI · SC · DATA BIT 6
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	= DMA option signal + MP option signal + SWR7 · ISR + IOGE · IOI · SC · DATA BIT 7

Table 7-31. A16 Memory Protect Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	= DMA option signal + MP option signal + SWR8 · ISR + IOGE · IOI · SC · DATA BIT 8
IOBI 9 (Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	= DMA option signal + MP option signal + SWR9 · ISR + IOGE · IOI · SC · DATA BIT 9
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	= DMA option signal + MP option signal + SWR10 · ISR + IOGE · IOI · SC · DATA BIT 10
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	= DMA option signal + MP option signal + SWR11 · ISR + IOGE · IOI · SC · DATA BIT 11
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	= DMA option signal + MP option signal + SWR12 · ISR + IOGE · IOI · SC · DATA BIT 12
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	= DMA option signal + MP option signal + SWR13 · ISR + IOGE · IOI · SC · DATA BIT 13

Table 7-31. A16 Memory Protect Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOBI 14 (Input/Output Bus, Input Bit 14)	A1-73 A5-82 A16-76 A101-63 A203-82 thru A218-82 A220-80	A102-33	= DMA option signal + MP option signal + SWR14 · ISR + IOGE · IOI · SC · DATA BIT 14
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60	A16-6	See source
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50	A16-5	See source
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57	A16-4	See source
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35	A16-3	See source
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60	A16-26	See source
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50	A16-28	See source
IOBO 6 (Input/Output Bus, Output Bit 6)	A104-57	A16-22	See source
IOBO 7 (Input/Output Bus, Output Bit 7)	A104-35	A16-20	See source
IOBO 8 (Input/Output Bus, Output Bit 8)	A103-60	A16-45	See source
IOBO 9 (Input/Output Bus, Output Bit 9)	A103-50	A16-54	See source
IOBO 10 (Input/Output Bus, Output Bit 10)	A103-57	A16-50	See source
IOBO 11 (Input/Output Bus, Output Bit 11)	A103-35	A16-52	See source
IOBO 12 (Input/Output Bus, Output Bit 12)	A102-60	A16-44	See source
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-50	A16-46	See source
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57	A16-43	See source
IOG (Input/Output Instruction Group, Buffered)	A107-6	A16-16	See source
IOGE (Input/Output Instruction Group, Buffered)	A6-59 A16-19	A108-16 A201-33	See source or option

Table 7-31. A16 Memory Protect Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOI (Input/Output, Input)	A4-81 A4-84 A108-44	A16-59	See source or option
IOO (Input/Output, Output)	A108-13	A16-57	See source
$\overline{\text{IR15}}$ ("not" Instruction Register Bit 15)	A16-33 A107-42	A6-4 A106-49	See source or option
IRQ5 (Interrupt Request 5)	A16-35 A215-33 A216-6 A219-58	A15-77 A202-29	See option
JMP (Jump Instruction)	A107-79	A16-11	See source
MPC (Memory Protect Control)	A16-25	A6-36 A15-63	See option
MR0 (M-Register Bit 0)	A105-68	A16-14	See source
MR1 (M-Register Bit 1)	A105-18	A16-10	See source
MR2 (M-Register Bit 2)	A105-65	A16-8	See source
MR3 (M-Register Bit 3)	A105-25	A16-18	See source
MR4 (M-Register Bit 4)	A104-68	A16-30	See source
MR5 (M-Register Bit 5)	A104-18	A16-42	See source
MR6 (M-Register Bit 6)	A104-65	A16-37	See source
MR7 (M-Register Bit 7)	A104-25	A16-32	See source
MR8 (M-Register Bit 8)	A103-68	A16-66	See source
MR9 (M-Register Bit 9)	A103-18	A16-68	See source
MR10 (M-Register Bit 10)	A103-65	A16-58	See source
MR11 (M-Register Bit 11)	A103-25	A16-60	See source
MR12 (M-Register Bit 12)	A102-68	A16-74	See source
MR13 (M-Register Bit 13)	A102-18	A16-77	See source
MR14 (M-Register Bit 14)	A102-65	A16-72	See source
MWL (Memory Write Level)	A106-33	A16-34	See source
P123 (Phase 1, Phase 2, or Phase 3)	A6-78 A106-78	A16-63	See source or option
PH1 (Phase 1, Fetch)	A106-41	A16-21	See source
PH2 (Phase 2, Indirect)	A106-37	A16-49	See source
PH5 (Phase 5)	A4-8	A16-7	See option

Table 7-31. A16 Memory Protect Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
POPIO(B) (Power On Pulse to I/O, Buffered)	A201-72	A16-29	See source
PRH5/PRL4 (Priority High Select Code 5/Priority Low Select Code 4)	A6-3	A16-38	See source
PRH6/PRL5 (Priority High Select Code 6/Priority Low Select Code 5)	A15-27 A16-51	A1-33 A201-76 A201-82	See option
RSDS (Reset, Double Store Operation)	A16-15	A15-72 A109-65	See option
SCL1 (Select Code Least Significant Digit, Octal 1)	A202-67	A16-71	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A16-9	See source
SCL5 (Select Code Least Significant Digit, Octal 5)	A202-52	A16-12	See source
SIR (Service Interrupt Request)	A201-35	A16-36	See source
STC (Set Control)	A108-56	A16-41	See source
T1 (Time Period 1)	A106-53	A16-24	See source
T3 (Time Period 3)	A106-63	A16-23	See source
T7 (Time Period 7)	A106-18	A16-61	See source
TSA (Time Strobe A)	A106-67	A16-27	See source

Table 7-32. A101 Front Panel Coupler Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V, Card Input	A100E3	A101-47 A101-48	None
-2V, Card Output	A101-B*	A502S0-3	None
+4.5V, Card Input	A100E1	A101-39 A101-40	None
+4.5V, Card Output	A101-M*	A502S109-4	None
+4.5V/-5.6V, Card Input	A502S109-3	A101-Z*	None
+4.5V/-5.6V, Card Output	A100TB1-8	A101-84	None
-5.6V, Card Input	A100TB1-5	A101-79	None
-5.6V, Card Output	A101-19*	A502S109-2	None
Display Memory FF	--	--	Set = DMSW ; $\overline{RF2}$ Clear = $\overline{DMSW}$
DMS (Display Memory FF, set-side output)	A101-74	A106-59	= Display Memory FF, set-side output
DMSW (Display Memory Switch Output)	A502S101-4	A101-W*	None
$\overline{DMSW}$ ("not" Display Memory Switch Output)	A502S101-3	A101-BB*	None
E IND (Extend FF Indicator), Card Input	A108-37	A101-83	See source
E IND (Extend FF Indicator), Card Output	A101-20*	A501-20	See source
GND (Ground)	A100E2	A101-1 A101-2 A101-85 A101-86	None
HLS (Halt Switch Output), Card Input	A502S106-4	A101-R*	None
HLS (Halt Switch Output), Card Output	A101-54	A6-72 A106-50	None
$\overline{HLS}$ ("not" Halt Switch Output), Card Input	A502S106-3	A101-P*	None
$\overline{HLS}$ ("not" Halt Switch Output), Card Output	A101-50	A106-45	None
ILS (Instruction Loop Switch Output), Card Input	A501-H	A101-H*	None
ILS (Instruction Loop Switch Output), Card Output	A101-26	A107-73	None

Table 7-32. A101 Front Panel Coupler Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI0 FF + IOGE · IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI1 FF + IOGE · IOI · SC · DATA BIT 1
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	= DMA option signal + MP option signal + SWR2 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI2 FF + IOGE · IOI · SC · DATA BIT 2
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI3 FF + IOGE · IOI · SC · DATA BIT 3
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI4 FF + IOGE · IOI · SC · DATA BIT 4

Table 7-32. A101 Front Panel Coupler Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI5 FF + IOGE · IOI · SC · DATA BIT 5
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	= DMA option signal + MP option signal + SWR6 · ISR + IOGE · IOI · SC · DATA BIT 6
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	= DMA option signal + MP option signal + SWR7 · ISR + IOGE · IOI · SC · DATA BIT 7
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	= DMA option signal + MP option signal + SWR8 · ISR + IOGE · IOI · SC · DATA BIT 8
IOBI 9 (Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	= DMA option signal + MP option signal + SWR9 · ISR + IOGE · IOI · SC · DATA BIT 9
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	= DMA option signal + MP option signal + SWR10 · ISR + IOGE · IOI · SC · DATA BIT 10

Table 7-32. A101 Front Panel Coupler Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	= DMA option signal + MP option signal + SWR11 · ISR + IOGE · IOI · SC · DATA BIT 11
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	= DMA option signal + MP option signal + SWR12 · ISR + IOGE · IOI · SC · DATA BIT 12
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	= DMA option signal + MP option signal + SWR13 · ISR + IOGE · IOI · SC · DATA BIT 13
IOBI 14 (Input/Output Bus, Input Bit 14)	A1-73 A5-82 A16-76 A101-63 A203-82 thru A218-82 A220-80	A102-33	= DMA option signal + MP option signal + SWR14 · ISR + IOGE · IOI · SC · DATA BIT 14
IOBI 15 (Input/Output Bus, Input Bit 15)	A5-83 A15-28 A101-67 A203-83 thru A218-83 A220-82	A102-27	= DMA option signal + PE option signal + SWR15 · ISR + IOGE · IOI · SC · DATA BIT 15
ISR (Input Switch Register)	A108-84	A101-6	See source
LADS (Load Address FF, set-side output)	A101-70	A106-68	= Load Address FF, set-side output
LADSW (Load Address Switch Output)	A502S102-4	A101-V*	None
$\overline{\text{LADSW}}$ ("not" Load Address Switch Output)	A502S102-3	A101-23*	None
LAS (Load A FF, set-side output)	A101-62	A106-80	= Load A FF, set-side output

Table 7-32. A101 Front Panel Coupler Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
LASW (Load A Switch Output)	A502S104-4	A101-T*	None
$\overline{\text{LASW}}$ ("not" Load A Switch Output)	A502S104-3	A101-22*	None
LBS (Load B FF, set-side output)	A101-66	A106-65	= Load B FF, set-side output
LBSW (Load B Switch Output)	A502S103-4	A101-U*	None
$\overline{\text{LBSW}}$ ("not" Load B Switch Output)	A502S103-3	A101-AA*	None
LMS (Load Memory FF, set-side output)	A101-58	A106-46 A203-59 thru A218-59	= Load Memory FF, set-side output
LMSW (Load Memory Switch Output)	A502S105-3	A101-S*	None
$\overline{\text{LMSW}}$ ("not" Load Memory Switch Output)	A502S105-3	A101-21*	None
Load A FF	– –	– –	Set = LASW · $\overline{\text{RF2}}$ Clear = $\overline{\text{LASW}}$
Load Address FF	– –	– –	Set = LADS · $\overline{\text{RF2}}$ Clear = $\overline{\text{LADS}}$
Load B FF	– –	– –	Set = LBSW · $\overline{\text{RF2}}$ Clear = $\overline{\text{LBSW}}$
Load Memory FF	– –	– –	Set = LMSW · $\overline{\text{RF2}}$ Clear = $\overline{\text{LMSW}}$
LPS (Loader Protect Switch Output), Card Input	A502S110-2	A101-Y*	None
LPS (Loader Protect Switch Output), Card Output	A101-82	A14-31	None
MNS (Memory Normal Switch Output), Card Input	A501-F	A101-F*	None
MNS (Memory Normal Switch Output), Card Output	A101-22	A106-12	None
OVF IND (Overflow Indicator), Card Input	A108-9	A101-4	See source
OVF IND (Overflow Indicator), Card Output	A101-A*	A501-A	See source
P IND (Power Indicator Lamp), Card Input	A6-49	A101-75	See source
P IND (Power Indicator Lamp), Card Output	A101-18*	A502DS109	See source

Table 7-32. A101 Front Panel Coupler Card, Signal List (Continued)

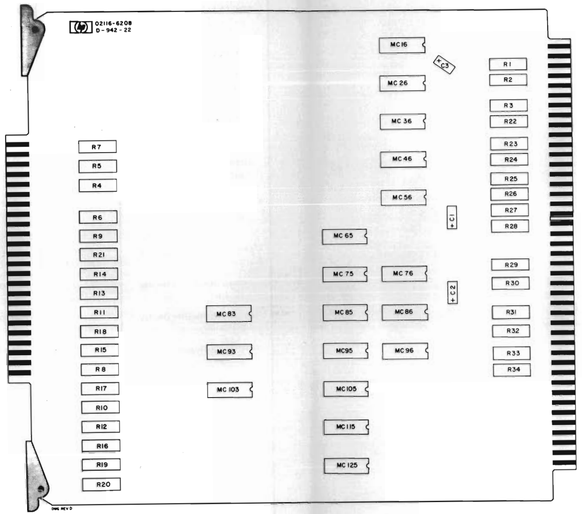
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PNS (Phase Normal Switch Output), Card Input	A501-E	A101-E*	None
PNS (Phase Normal Switch Output), Card Output	A101-18	A106-43	None
POFP (Power On/Off Pulse)	A6-56	A101-10	See source
PON (Power On Normal), Card Input	A6-58	A101-71	See source
PON (Power On Normal), Card Output	A1-58	A101-17*	See source
PRS (Preset Switch Output, Gated)	A101-30	A6-78 A106-78	= PRSW ; $\overline{RF2}$
PRSW (Preset Switch Output)	A502S108-4	A101-J*	None
$\overline{PRSW}$ ("not" Preset Switch Output), Card Input	A502S108-3	A101-K*	None
$\overline{PRSW}$ ("not" Preset Switch Output), Card Output	A101-34	A106-79	None
$\overline{RF2}$ ("not" Run FF 2)	A106-58	A101-14	See source
RNS (Run Switch FF, set-side output)	A101-44	A6-60 A106-70	= Run Switch FF, set-side output
RNSW (Run Switch Output)	A502S107-4	A101-N*	None
$\overline{RNSW}$ ("not" Run Switch Output), Card Input	A502S107-3	A101-L*	None
Run Switch FF	– –	– –	Set = RNSW Clear = $\overline{RNSW}$
SCS (Single Cycle FF, set-side output)	A101-78	A106-56	= Single Cycle FF, set-side output
SCSW (Single Cycle Switch Output)	A502S100-4	A101-X*	None
$\overline{SCSW}$ ("not" Single Cycle Switch Output)	A502S100-3	A101-24*	None
Single Cycle FF	– –	– –	Set = SCSW · $\overline{RF2}$ Clear = $\overline{SCSW}$
SWR0 (Switch Register Bit 0)	A502S0-2	A101-1*	None
SWR1 (Switch Register Bit 1)	A502S1-2	A101-2*	None
SWR2 (Switch Register Bit 2)	A502S2-2	A101-3*	None
SWR3 (Switch Register Bit 3)	A502S3-2	A101-4*	None
SWR4 (Switch Register Bit 4)	A502S4-2	A101-5*	None
SWR5 (Switch Register Bit 5)	A502S5-2	A101-6*	None

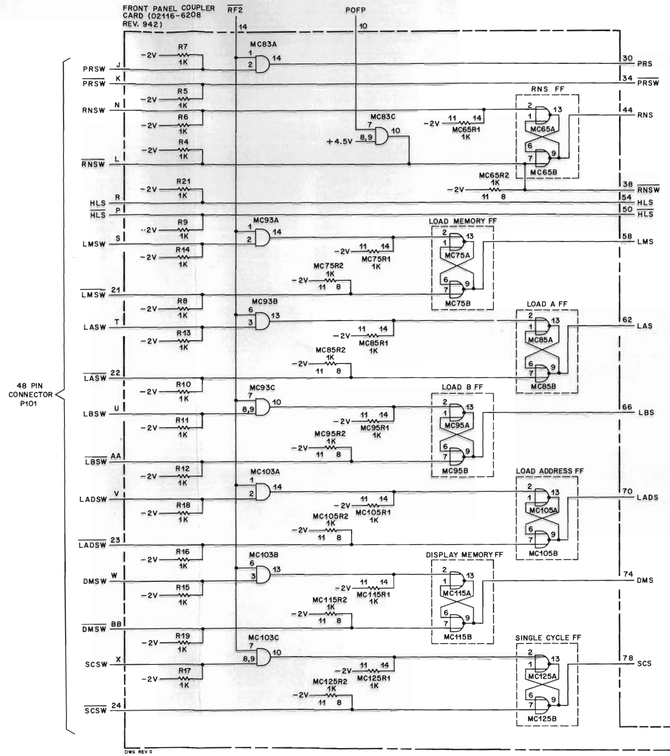
Table 7-32. A101 Front Panel Coupler Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SWR6 (Switch Register Bit 6)	A502S6-2	A101-7*	None
SWR7 (Switch Register Bit 7)	A502S7-2	A101-8*	None
SWR8 (Switch Register Bit 8)	A502S8-2	A101-9*	None
SWR9 (Switch Register Bit 9)	A502S9-2	A101-10*	None
SWR10 (Switch Register Bit 10)	A502S10-2	A101-11*	None
SWR11 (Switch Register Bit 11)	A502S11-2	A101-12*	None
SWR12 (Switch Register Bit 12)	A502S12-2	A101-13*	None
SWR13 (Switch Register Bit 13)	A502S13-2	A101-14*	None
SWR14 (Switch Register Bit 14)	A502S14-2	A101-15*	None
SWR15 (Switch Register Bit 15)	A502S15-2	A101-16*	None

Table 7-33. A101 Front Panel Coupler Card (02116-6208) Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	56289	150D225X0020A2-DYS
C3	0160-0154	Capacitor, Fxd, My, 0.0022 uF, 10%, 200 VDCW	56289	192P22292-PTS
MC16,26,36,46,56,76,86,96	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC65,75,85,95,105,115,125	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC83,93,103	1820-0953	Integrated Circuit, CTL	07263	SL3456
R1 thru R3,R22 thru R34	0698-3400	Resistor, Fxd, Flm, 147 ohms, 1%, 1/2W	28480	0698-3400
R4 thru R21	0698-3399	Resistor, Fxd, Flm, 133 ohms, 1%, 1/2W	28480	0698-3399





NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
2. RESISTORS R4 THRU R21 ARE 133 OHMS.

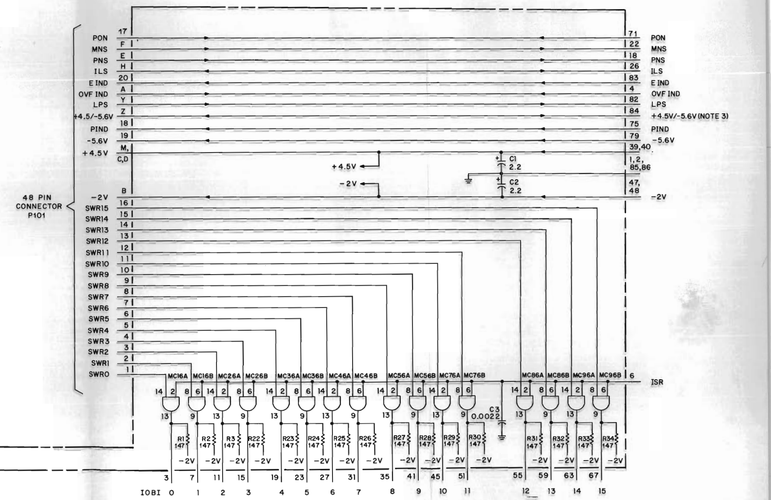


Figure 7-11. A101 Front Panel Coupler Card (02116-6208), Parts Location and Schematic Diagram

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A102-47 A102-48	None
+4.5V	A100E1	A102-39 A102-40	None
ADF (Add Function)	A4-82 A107-75 A110-12	A102-5	See source or option
ANF (And Function)	A107-56	A102-72	See source
AR12 FF (A-Register Bit 12 FF)			J = TB12 K = $\overline{TB12}$ Clock = STBA
AR13 FF (A-Register Bit 13 FF)			J = TB13 K = $\overline{TB13}$ Clock = STBA
AR14 FF (A-Register Bit 14 FF)			J = TB14 K = $\overline{TB14}$ Clock = STBA
AR15 FF (A-Register Bit 15 FF)			J = TB15 K = $\overline{TB15}$ Clock = STBA
ARD12 (A-Register Display Bit 12)	A102-7* A102-H*	A501DS61	= AR12 FF, set-side output
ARD13 (A-Register Display Bit 13)	A102-8* A102-J*	A501DS62	= AR13 FF, set-side output
ARD14 (A-Register Display Bit 14)	A102-9* A102-K*	A501DS63	= AR14 FF, set-side output
ARD15 (A-Register Display Bit 15)	A102-10* A102-L*	A501DS64	= AR15 FF, set-side output
BR12 FF (B-Register Bit 12 FF)			J = TB12 K = $\overline{TB12}$ Clock = STBB
BR13 FF (B-Register Bit 13 FF)			J = TB13 K = $\overline{TB13}$ Clock = STBB
BR14 FF (B-Register Bit 14 FF)			J = TB14 K = $\overline{TB14}$ Clock = STBB
BR15 FF (B-Register Bit 15 FF)			J = TB15 K = $\overline{TB15}$ Clock = STBB
BRD12 (B-Register Display Bit 12)	A102-6* A102-F*	A501DS77	= BR12 FF, set-side output
BRD13 (B-Register Display Bit 13)	A102-5* A102-E*	A501DS78	= BR13 FF, set-side output

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
BRD14 (B-Register Display Bit 14)	A102-4* A102-D*	A501DS79	= BR14 FF, set-side output
BRD15 (B-Register Display Bit 15)	A102-3* A102-C*	A501DS80	= BR15 FF, set-side output
C12 (Carry Bit 12)	A103-36	A102-67	See source
C16 (Carry Bit 16)	A102-36	A108-64 A110-50	= C15 · RB15 + C15 · SB15 + RB15 · SB15
$\overline{\text{CMF}}$ ("not" Complement Function)	A14-79	A102-64	See source
$\overline{\text{EOF}}$ ("not" Exclusive OR Function)	A14-75	A102-76	See source
GND (Ground, Card Input)	A100E2	A102-1 A102-2 A102-85 A102-86	None
GND (Ground) Card Output	A102-1* A102-2* A102-A* A102-B*	A501-1 A501-2	None
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	See source or option
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	See source or option
IOBI 14 (Input/Output Bus, Input Bit 14)	A1-73 A5-82 A16-76 A101-63 A203-82 thru A218-82 A220-80	A102-33	See source or option
IOBI 15 (Input/Output Bus, Input Bit 15)	A5-83 A15-28 A101-67 A203-83 thru A218-83 A220-82	A102-27	See source or option

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOBO 12 (Input/Output Bus, Output Bit 12)	A102-60	A1-68 A2-68 A5-57 A16-44 A203-57 thru A218-57 A219-75	= IOCO · RB12 + DMA option signal + MP option signal
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-50	A1-74 A2-74 A4-54 A5-61 A16-46 A203-61 thru A218-61 A219-77	= IOCO · RB13 + DMA option signal + MP option signal
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57	A1-76 A2-76 A3-15 A5-65 A16-43 A203-65 thru A218-65 A219-79	= IOCO · RB14 + DMA option signal + MP option signal
IOBO 15 (Input/Output Bus, Output Bit 15)	A102-35	A1-78 A2-78 A4-51 A5-74 A203-74 thru A218-74 A219-81	= IOCO · RB15 + DMA option signal
IOCO (Input/Output Control, Output)	A108-34	A102-70	See source
$\overline{\text{IOF}}$ ("not" Inclusive OR Function)	A107-84	A102-73	See source
IOI (Input/Output, Input)	A4-81 A4-84 A108-44	A102-31	See source or option
MR12 (M-Register Bit 12)	A102-68	A14-56 A16-74	= MR12 FF, set-side output
$\overline{\text{MR12}}$ ("not" M-Register Bit 12)	A102-63	None	= MR12 FF, clear-side output
MR12 FF (M-Register Bit 12 FF)			J = TB12 K = $\overline{\text{TB12}}$ Clock = STM12-15 Direct Clear = RSM10-15
MR13 (M-Register Bit 13)	A102-18	A14-60 A16-77	= MR13 FF, set-side output

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
$\overline{MR13}$ ("not" M-Register Bit 13)	A102-19	None	= MR13 FF, clear-side output
MR13 FF (M-Register Bit 14 FF)			J = TB13 K = $\overline{TB13}$ Clock = STM12-15 Direct Clear = RSM10-15
MR14 (M-Register Bit 14)	A102-65	A14-64 A16-72	= MR14 FF, set-side output
$\overline{MR14}$ ("not" M-Register Bit 14)	A102-66	NOne	= MR14 FF, clear-side output
MR14 FF (M-Register Bit 15 FF)			J = TB14 K = $\overline{TB14}$ Clock = STM12-15 Direct Clear = RSM10-15
MR15 (M-Register Bit 15)	A102-25	None	= MR15 FF, set-side output
$\overline{MR15}$ ("not" M-Register Bit 15)	A102-24	None	= MR15 FF, clear-side output
MR15 FF (M-Register Bit 15 FF)			J = TB15 K = $\overline{TB15}$ Clock = STM12-15 Direct Clear = RSM10-15
MRD12 (M-Register Display Bit 12)	A102-11* A102-M*	A501-DS45	= MR12 FF, set-side output
MRD13 (M-Register Display Bit 13)	A102-12* A102-N*	A501-DS46	= MR13 FF, set-side output
MRD14 (M-Register Display Bit 14)	A102-14* A102-R*	A501DS47	= MR14 FF, set-side output
MRD15 (M-Register Display Bit 15)	A102-13* A102-P*	A501DS48	= MR15 FF, set-side output
PR12 FF (P-Register Bit 12 FF)			J = TB12 K = $\overline{TB12}$ Clock = STP12-15
PR13 FF (P-Register Bit 13 FF)			J = TB13 K = $\overline{TB13}$ Clock = STP12-15
PR14 FF (P-Register Bit 14 FF)			J = TB14 K = $\overline{TB14}$ Clock = STP12-15
PR15 FF (P-Register Bit 15 FF)			J = TB15 K = $\overline{TB15}$ Clock = STP12-15
PRD12 (P-Register Display Bit 12)	A102-15* A102-S*	A501DS29	= PR12 FF, set-side output

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PRD13 (P-Register Display Bit 13)	A102-18* A102-V*	A501DS30	= PR13 FF, set-side output
PRD14 (P-Register Display Bit 14)	A102-19* A102-W*	A501DS31	= PR14 FF, set-side output
PRD15 (P-Register Display Bit 15)	A102-17* A102-U*	A501DS32	= PR15 FF, set-side output
RARB (Read A-Register to the R Bus)	A107-19 A110-65	A102-34	See source or option
RB12 (R Bus Bit 12)	A102-37	None	= RARB · AR12 FF + RBRB · BR12 FF + RPRB · PR12 FF
RB13 (R Bus Bit 13)	A102-62	None	= RARB · AR13 FF + RPRB · BR13 FF + RPRB · PR13 FF
RB14 (R Bus Bit 14)	A102-71	A110-25	= RARB · AR14 FF + RBRB · BR14 FF + RPRB · PR14 FF
RB15 (R Bus Bit 15)	A102-30	A108-66 A110-77	= RARB · AR15 FF + RBRB · BR15 FF + RPRB · PR15 FF
RBRB (Read B-Register to the R Bus)	A107-18 A110-58	A102-28	See source or option
$\overline{\text{RL4}}$ ("not" Rotate Left 4 Bits)	A108-28	A102-78	See source
$\overline{\text{RLL}}$ ("not" Rotate Left to Least Significant Bit)	A108-42	A102-41	See source
RMSB (Read M-Register to the S Bus)	A107-68 A110-34	A102-8	See source or option
RPRB (Read P-Register to the R Bus)	A107-72 A110-4	A102-12	See source or option
RSM10-15 (Reset M-Register Bits 10 thru 15)	A107-11	A102-14 A102-21	See source
RST (Reset T-Register)	A107-58	A102-7	See source
RTSB (Read T-Register to the S Bus)	A107-82 A110-19	A102-20	See source or option
SB12 (S Bus Bit 12)	A102-42	None	= IOBI · IOBI 12 + RMSB · MR12 + RTSB · TR12
SB13 (S Bus Bit 13)	A102-59	None	= IOI · IOBI 13 + RMSB · MR13 + RTSB · TR13

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SB14 (S Bus Bit 14)	A102-61	None	= IOI · IOBI14 + RMSB · MR14 + RTSB · TR14
SB15 (S Bus Bit 15)	A102-6	A108-50	= IOI · IOBI 15 + RMSB · MR15 + RTSB · TR15
$\overline{\text{SL14}}$ ("not" Shift Left, Bit 14)	A14-74	A102-82	See source
$\overline{\text{SLM}}$ ("not" Shift Left Magnitude)	A14-77	A102-80	See source
$\overline{\text{SRM}}$ ("not" Shift Right Magnitude)	A14-78	A102-74 A102-83	See source
ST12 (Set T-Register Bit 12)	A13-57	A102-49	See source
ST12 GND (Set T-Register Bit 12, Ground Return)	A13-58	A102-1	None
ST13 (Set T-Register Bit 13)	A13-61	A102-4	See source
ST13 GND (Set T-Register Bit 13, Ground Return)	A13-62	A102-2	None
ST14 (Set T-Register Bit 14)	A13-65	A102-52	See source
ST14 GND (Set T-Register Bit 14, Ground Return)	A13-66	A102-2	None
ST15 (Set T-Register Bit 15)	A13-69	A102-11	See source
ST15 GND (Set T-Register Bit 15, Ground Return)	A13-69	A102-1	None
STBA (Store T Bus in A-Register)	A107-50	A102-38	See source
STBB (Store T Bus in B-Register)	A107-51	A102-26	See source
STBT (Store T Bus in T-Register)	A107-63	A102-51	See source
STM12-15 (Store T Bus Bit 12 thru 15 in M-Register)	A107-28	A102-22 A102-29	See source
STP12-15 (Store T Bus Bits 12 thru 15 in P-Register)	A107-8	A102-23 A102-44	See source
TAN4 (T Bus Bits 12 thru 15 "anded")	A102-43	A108-59	= $\overline{\text{TB15}}$ · $\overline{\text{TB14}}$ · $\overline{\text{TB13}}$ · $\overline{\text{TB12}}$

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB0 (T Bus Bit 0)	A102-81 A105-69 A108-51 A110-79 A202-10	A105-69 A110-79	= ADF · RB0 · SB0 · C0 + ADF · RB0 · SB0 · C0 + ADF · RB0 · SB0 · C0 + ADF · RB0 · SB0 · C0 + ADF · RB0 · SB0 + CMF · RB0 + EFF · SRG · T3 · TR8 · TR7 · TR6 + EFF · SRG · T5 · TR2 · TR1 · TR0 + EOF · RB0 · SB0 + EOF · RB0 · SB0 + IOF · RB0 + IOF · SB0 + RL4 · RB12 + RL4 · SB12 + RLL · RB15 + RLL · SB15 + RSM6-9 · SRA0 + SLM · RB15 + SLM · SB15 + SRM · RB1 + SRM · SB1 + EAU option signal
TB1 (T Bus Bit 1)	A102-75 A105-13 A202-9	A105-13 A108-75	= ADF · RB1 · SB1 · C1 + ADF · RB1 · SB1 · C1 + ADF · RB1 · SB1 · C1 + ADF · RB1 · SB1 · C1 + ANF · RB1 · SB1 + CMFE · RB1 + EOF · RB1 · SB1 + EOF · RB1 · SB1 + IOF · RB1 + IOF · SB1 + RL4 · SB12 + RL4 · SB13 + RLL · RB0 + RLL · SB0 + RSM6-9 · SRA1 + SLM · RB0 + SLM · SB0 + SRM · RB0 + SRM · RB2 + SRM · SB2
TB2 (T Bus Bit 2)	A102-84 A105-55 A202-8	A105-55 A108-67	= ADF · RB2 · SB2 · C2 + ADF · RB2 · SB2 · C2 + ADF · RB2 · SB2 · C2 + ADF · RB2 · SB2 · C2 + ANF · RB2 · SB2 + CMFE · RB2 + EOF · RB2 · SB2 + EOF · RB2 · SB2 + IOF · RB2 + IOF · SB2 + RL4 · RB14 + RL4 · SB14 + RLL · RB1 + RLL · SB1 + RSM6-9 · SRA2 + SLM · RB1 + SLM · SB1 + SRM · RB3 + SRM · SB3

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB3 (T Bus Bit 3)	A102-45 A104-77 A105-17 A202-7	A105-17 A108-78	= ADF · RB3 · SB3 · C3 + ADF · RB3 · $\overline{SB3}$ · $\overline{C3}$ + ADF · $\overline{RB3}$ · $\overline{SB3}$ · C3 + ADF · $\overline{RB3}$ · SB3 · $\overline{C3}$ + ANF · RB3 · SB3 + CMFE · $\overline{RB3}$ + EOF · RB3 · $\overline{SB3}$ + EOF · $\overline{RB3}$ · SB3 + IOF · RB3 + IOF · SB3 + RL4 · RB15 + RL4 · SB15 + RLL · RB2 + RLL · SB2 + RSM6-9 · SRA3 + SLM · RB2 + SLM · SB2 + SRM · RB4 + SRM · SB4
TB11 (T Bus Bit 11)	A102-77 A103-17 A104-45	A103-17	= ADF · RB11 · SB11 · C11 + ADF · $\overline{RB11}$ · SB11 · $\overline{C11}$ + ADF · $\overline{RB11}$ · $\overline{SB11}$ · C11 + ADF · RB11 · $\overline{SB11}$ · $\overline{C11}$ + ANF · RB11 · SB11 + CMFE · $\overline{RB11}$ + EOF · RB11 · $\overline{SB11}$ + EOF · $\overline{RB11}$ · SB11 + IOF · RB11 · + IOF · SB11 + RL4 · RB7 + RL4 · SB7 + RLL · RB10 + RLL · SB10 + RSM6-9 · SRA11 + SLM · RB10 + SLM · SB10 + SRM · RB12 + SRM · SB12
TB12 (T Bus Bit 12)	A102-69 A103-81	A102-69 A108-76	= ADF · RB12 · SB12 · C12 + ADF · $\overline{RB12}$ · SB12 · $\overline{C12}$ + ADF · $\overline{RB12}$ · $\overline{SB12}$ · C12 + ADF · RB12 · $\overline{SB12}$ · $\overline{C12}$ + ANF · RB12 · SB12 + CMFE · $\overline{RB12}$ + EOF · RB12 · $\overline{SB12}$ + EOF · RB12 · $\overline{SB12}$ + IOF · RB12 + IOF · SB12 + RL4 · RB8 + RL4 · SB8 + RLL · RB11 + RLL · SB11 + RSM6-9 · SRA12 + SLM · RB11 + SLM · SB11 + SRM · RB13 + SRM · SB13

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
TB13 (T Bus Bit 13)	A102-13 A103-75	A102-13 A108-73	= ADF · RB13 · SB13 · C13 + ADF · $\overline{RB13}$ · SB13 · $\overline{C13}$ + ADF · $\overline{RB13}$ · $\overline{SB13}$ · C13 + ADF · RB13 · $\overline{SB13}$ · $\overline{C13}$ + ANF · RB13 · SB13 + CMFE · $\overline{RB13}$ + EOF · RB13 · $\overline{SB13}$ + EOF · $\overline{RB13}$ · SB13 + IOF · RB13 + IOF · SB13 + RL4 · RB9 + RL4 · SB9 + RLL · RB12 + RLL · SB12 + RSM6-9 · SRA13 + SLM · RB12 + SLM · SB12 + SRM · RB14 + SRM · SB14
TB14 (T Bus Bit 14)	A102-55 A103-84	A102-55 A108-70	= ADF · RB14 · SB14 · C14 + ADF · $\overline{RB14}$ · SB14 · $\overline{C14}$ + ADF · $\overline{RB14}$ · $\overline{SB14}$ · C14 + ADF · RB14 · $\overline{SB14}$ · $\overline{C14}$ + ANF · RB14 · SB14 + CMFE · $\overline{RB14}$ + EOF · RB14 · $\overline{SB14}$ + EOF · $\overline{RB14}$ · SB14 + IOF · RB14 + IOF · SB14 + RL4 · RB10 + RL4 · SB10 + RLL · RB13 + RLL · SB13 + RSM6-9 · SRA14 + SLM · RB13 + SLM · SB13 + SRM · RB15 + SRM · SB15
TB15 (T Bus Bit 15)	A102-17 A103-45 A105-77 A108-20 A110-80	A102-17 A108-20 A109-64 A110-80	= ADF · RB15 · SB15 · C15 + ADF · $\overline{RB15}$ · SB15 · $\overline{C15}$ + ADF · $\overline{RB15}$ · $\overline{SB15}$ · C15 + ADF · RB15 · $\overline{SB15}$ · $\overline{C15}$ + ANF · RB15 · SB15 + CMFE · $\overline{RB15}$ + EOF · RB15 · $\overline{SB15}$ + EOF · $\overline{RB15}$ · SB15 + IOF · RB15 + IOF · SB15 + RL4 · RB11 + RL4 · SB11 + RLL · RB14 + RLL · SB14 + RSM6-9 · SRA15 + SLM · RB14 + SLM · SB14 (Continued on next page)

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
TB15 (Continued)			+ SRG · T3 · $\overline{TR8}$ · $\overline{TR7}$ · RB15(B) + SRG · T5 · $\overline{TR2}$ · $\overline{TR1}$ · TB15(B) + SRG · EFF · T3 · TR8 · $\overline{TR7}$ · TR6 + SRG · EFF · T5 · TR2 · $\overline{TR1}$ · TR0 + SRM · RB0 + SRM · SB0 + EAU option signal
TR12 (T-Register Bit 12)	A102-58	A5-62 A15-14 A107-17	= TR12 FF, set-side output
$\overline{TR12}$ ("not" T-Register Bit 12)	A102-54	A7-78 A12-78 A15-12 A17-78 A22-78	= TR12 FF, clear-side output
TR12 FF (T-Register Bit 12 FF)			J = TB12 K = $\overline{TB12}$ Clock = STBT Direct Set = ST12 Direct Clear = RST
TR13 (T-Register Bit 13)	A102-9	A5-66 A15-13 A107-30	= TR13 FF, set-side output
$\overline{TR13}$ ("not" T-Register Bit 13)	A102-10	A7-84 A12-84 A15-11 A17-84 A22-84	= TR13 FF, clear-side output
TR13 FF (T-Register Bit 13 FF)			J = TB13 K = $\overline{TB13}$ Clock = STBT Direct Set = ST13 Direct Clear = RST
TR14 (T-Register Bit 14)	A102-56	A5-68 A15-6 A107-33	= TR14 FF, set-side output
$\overline{TR14}$ ("not" T-Register Bit 14)	A102-53	A7-82 A12-82 A15-4 A17-82 A22-82	= TR14 FF, clear-side output
TR14 FF (T-Register Bit 14 FF)			J = TB14 K = $\overline{TB14}$ Clock = STBT Direct Set = ST14 Direct Clear = RST
TR15 (T-Register Bit 15)	A102-16	A5-70 A15-5 A106-38 A107-41	= TR15 FF, set-side output

Table 7-34. A102 Arithmetic Logic Card (Bits 15-12), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
$\overline{\text{TR15}}$ ("not" T-Register Bit 15)	A102-15	A7-9 A12-9 A15-3 A17-9 A22-9 A106-36	= TR15 FF, clear-side output
TR15 FF (T-Register Bit 15 FF)			J = TB15 K = $\overline{\text{TB15}}$ Clock = STBT Direct Set = ST15 Direct Clear = RST
TRD12 (T-Register Display Bit 12)	A102-21* A102-Y*	A501DS13	= TR12 FF, set-side output
TRD13 (T-Register Display Bit 13)	A102-22* A102-Z*	A501DS14	= TR13 FF, set-side output
TRD14 (T-Register Display Bit 14)	A102-20* A102-X*	A501DS15	= TR14 FF, set-side output
TRD15 (T-Register Display Bit 15)	A102-16* A102-T*	A501DS16	= TR15 FF, set-side output

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A103-47 A103-48	None
+4.5V	A100E1	A103-39 A103-40	None
ADF (Add Function)	A4-82 A107-75 A110-12	A103-5	See source or option
ANF (And Function)	A107-56	A103-72	See source
AR8 FF (A-Register Bit 8 FF)			J = $\overline{TB8}$ K = TB8 Clock = STBA
AR9 FF (A-Register Bit 9 FF)			J = $\overline{TB9}$ K = TB9 Clock = STBA
AR10 FF (A-Register Bit 10 FF)			J = $\overline{TB10}$ K = TB10 Clock = STBA
AR11 FF (A-Register Bit 11 FF)			J = $\overline{TB11}$ K = TB11 Clock = STBA
ARD8 (A-Register Display Bit 8)	A103-7* A103-H*	A501DS57	= AR8 FF, set-side output
ARD9 (A-Register Display Bit 9)	A103-8* A103-J*	A501DS58	= AR9 FF, set-side output
ARD10 (A-Register Display Bit 10)	A103-9* A103-K*	A501DS59	= AR10 FF, set-side output
ARD11 (A-Register Display Bit 11)	A103-10* A103-L*	A501-DS60	= AR11 FF, set-side output
BR8 FF (B-Register Bit 8 FF)			J = $\overline{TB8}$ K = TB8 Clock = STB8
BR9 FF (B-Register Bit 9 FF)			J = $\overline{TB9}$ K = TB9 Clock = STBB
BR10 (B-Register Bit 10 FF)			J = $\overline{TB10}$ K = TB10 Clock = STBB
BR11 FF (B-Register Bit 11 FF)			J = $\overline{TB11}$ K = TB11 Clock = STBB
BRD8 (B-Register Display Bit 8)	A103-6* A103-F*	A501DS73	= BR8 FF, set-side output
BRD9 (B-Register Display Bit 9)	A103-5* A103-E*	A501DS74	= BR9 FF, set-side output

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
BRD10 (B-Register Display Bit 10)	A103-4* A103-D*	A501DS75	= BR10 FF, set-side output
BRD11 (B-Register Display Bit 11)	A103-3* A103-C*	A501DS76	= BR11 FF, set-side output
C8 (Carry Bit 8)	A104-36	A103-67	See source
C12 (Carry Bit 12)	A103-36	A102-67	= C11 · RB11 + C11 · SB11 + RB11 · SB11
$\overline{\text{CMF}}$ ("not" Complement Function)	A14-79	A103-64	See source
$\overline{\text{EOF}}$ ("not" Exclusive OR Function)	A14-75	A103-76	See source
GND (Ground), Card Input	A100E2	A103-1 A103-2 A103-85 A103-86	None
GND (Ground), Card Output	A103-1* A103-2* A103-A* A103-B*	A501-1 A501-2	None
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	See source or option
IOBI 9 (Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	See source or option
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	See source or option

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	See source or option
IOBO 8 (Input/Output Bus, Output Bit 8)	A103-60	A1-56 A2-56 A5-54 A16-45 A203-54 thru A218-54 A219-65	= IOCO · RB8 + DMA option signal + MP option signal
IOBO 9 (Input/Output Bus, Output Bit 9)	A103-50	A1-62 A2-62 A5-56 A16-54 A203-56 thru A218-56 A219-67	= IOCO · RB9 + DMA option signal + MP option signal
IOBO 10 (Input/Output Bus, Output Bit 10)	A103-57	A1-66 A2-66 A5-58 A16-50 A203-58 thru A218-58 A219-71	= IOCO · RB10 + DMA option signal + MP option signal
IOBO 11 (Input/Output Bus, Output Bit 11)	A103-35	A1-64 A2-64 A5-55 A16-52 A203-55 thru A218-55 A219-73	= IOCO · RB11 + DMA option signal + MP option signal
IOCO (Input/Output Control, Output)	A108-34	A103-70	See source
$\overline{\text{IOF}}$ ("not" Inclusive OR Function)	A107-84	A103-73	See source
IOI (Input/Output, Input)	A4-81 A4-84 A108-44	A103-31	See source or option
MR8 (M-Register Bit 8)	A103-68	A14-36 A16-66	= MR8 FF, set-side output
$\overline{\text{MR8}}$ ("not" M-Register Bit 8)	A103-63	None	= MR8 FF, clear-side output

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
MR8 FF (M-Register Bit 8 FF)			J = $\overline{TB8}$ K = TB8 Clock = STM6-9
MR9 (M-Register Bit 9)	A103-18	A14-42 A16-68	= MR9 FF, set-side output
$\overline{MR9}$ ("not" M-Register Bit 9)	A103-19	None	= MR9 FF, clear-side output
MR9 FF (M-Register Bit 9 FF)			J = TB9 K = $\overline{TB9}$ Clock = STM6-9
MR10 (M-Register Bit 10)	A103-65	A14-46 A16-58	= MR10 FF, set-side output
$\overline{MR10}$ ("not" M-Register Bit 10)	A103-66	None	= MR10 FF, clear-side output
MR10 FF (M-Register Bit 10 FF)			J = TB10 K = $\overline{TB10}$ Clock = STM10-11 Direct Clear = RSM10-15
MR11 (M-Register Bit 11)	A103-25	A14-52 A16-60	= MR11 FF, set-side output
$\overline{MR11}$ ("not" M-Register Bit 11)	A103-24	None	= MR11 FF, clear-side output
MR11 FF (M-Register Bit 11 FF)			J = TB11 K = $\overline{TB11}$ Clock = STM10-11 Direct Clear = RSM10-15
MRD8 (M-Register Display Bit 8)	A103-11* A103-M*	A501DS41	= MR8 FF, set-side output
MRD9 (M-Register Display Bit 9)	A103-12* A103-N*	A501DS42	= MR9 FF, set-side output
MRD10 (M-Register Display Bit 10)	A103-14* A103-R*	A501DS43	= MR10 FF, set-side output
MRD11 (M-Register Display Bit 11)	A103-13* A103-P*	A501DS44	= MR11 FF, set-side output
PR8 FF (P-Register Bit 8 FF)			J = $\overline{TB8}$ K = TB8 Clock = STP0-9
PR9 FF (P-Register Bit 9 FF)			J = $\overline{TB9}$ K = TB9 Clock = STP0-9
PR10 FF (P-Register Bit 10 FF)			J = $\overline{TB10}$ K = TB10 Clock = STP10-11

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PR11 FF (P-Register Bit 11 FF)			J = TB11 K = $\overline{TB11}$ Clock = STP10-11
PRD8 (P-Register Display Bit 8)	A103-15* A103-S*	A501DS25	= PR8 FF, set-side output
PRD9 (P-Register Display Bit 9)	A103-18* A103-V*	A501DS26	= PR9 FF, set-side output
PRD10 (P-Register Display Bit 10)	A103-19* A103-W*	A501DS27	= PR10 FF, set-side output
PRD11 (P-Register Display Bit 11)	A103-17* A103-U*	A501DS28	= PR11 FF, set-side output
RARB (Read A-Register to the R Bus)	A107-19 A110-65	A103-34	See source or option
RB8 (R Bus Bit 8)	A103-37	None	= RARB · AR8 FF + RBRB · BR8 FF + RPRB · PR8 FF
RB9 (R Bus Bit 9)	A103-62	None	= RARB · AR9 FF + RBRB · BR9 FF + RPRB · PR9 FF
RB10 (R Bus Bit 10)	A103-71	None	= RARB · AR10 FF + RBRB · BR10 FF + RPRB · PR10 FF
RB11 (R Bus Bit 11)	A103-30	None	= RARB · AR11 FF + RBRB · BR11 FF + RPRB · PR11 FF
RBRB (Read B-Register to the R Bus)	A107-18 A110-58	A103-28	See source or option
$\overline{RL4}$ ("not" Rotate Left 4 Bits)	A108-28	A103-78	See source
RMSB (Read M-Register to the S Bus)	A107-68 A110-34	A103-8	See source or option
RPRB (Read P-Register to the R Bus)	A107-72 A110-4	A103-12	See source or option
RSM6-9 (Reset M-Register Bits 6 thru 9)	A107-12	A103-14	See source
RSM10-15 (Reset M-Register Bits 10 thru 15)	A107-11	A103-21	See source
RST (Reset T-Register)	A107-58	A103-7	See source
RTSB (Read T-Register to the S Bus)	A107-82 A110-19	A103-20	See source or option
SB8 (S Bus Bit 8)	A103-42	None	= IOI · IOBI 8 + RMSB · MR8 + RTSB · TR8

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
SB9 (S Bus Bit 9)	A103-59	None	= IOI · IOBI 9 + RMSB · MR9 + RTSB · TR9
SB10 (S Bus Bit 10)	A103-61	None	= IOI · IOBI 10 + RMSB · MR10 + RTSB ; TR10
SB11 (S Bus Bit 11)	A103-6	None	= IOI · IOBI 11 + RMSB · MR11 + RTSB · TR11
$\overline{\text{SLM}}$ ("not" Shift Left Magnitude)	A14-77	A103-41 A103-80 A103-82	See source
$\overline{\text{SRM}}$ ("not" Shift Right Magnitude)	A14-78	A103-74 A103-83	See source
ST8 (Set T-Register Bit 8)	A13-37	A103-49	See source
ST8 GND (Set T-Register Bit 8, Ground Return)	A13-38	A103-1	None
ST9 (Set T-Register Bit 9)	A13-43	A103-2	See source
ST9 GND (Set T-Register Bit 9, Ground Return)	A13-44	A103-2	None
ST10 (Set T-Register Bit 10)	A13-49	A103-52	See source
ST10 GND (Set T-Register Bit 10, Ground Return)	A13-50	A103-2	None
ST11 (Set T-Register Bit 11)	A13-53	A103-11	See source
ST11 GND (Set T-Register Bit 11, Ground Return)	A13-54	A103-1	None
STBA (Store T Bus in A-Register)	A107-50	A103-38	See source
STBB (Store T Bus in B-Register)	A107-51	A103-26	See source
STBT (Store T Bus in T-Register)	A107-63	A103-51	See source
STM6-9 (Store T Bus Bits 6 thru 9 in M-Register)	A107-21	A103-29	See source
STM10-11 (Store T Bus Bits 10 thru 11 in M-Register)	A107-27	A103-22	See source
STP0-9 (Store T Bus Bits 0 thru 9 in P-Register)	A107-7	A103-23	See source
STP10-11 (Store T Bus Bits 10 thru 11 in P-Register)	A107-74	A103-44	See source

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
TAN3 (T Bus Bits 8 thru 11 "anded")	A103-43	A108-60	= $\overline{RB11} \cdot \overline{TB10} \cdot \overline{TB9} \cdot \overline{TB8}$
TB7 (T Bus Bit 7)	A103-77 A104-17 A105-45	A104-17	= ADF · RB7 · SB7 · C7 + ADF · $\overline{RB7}$ · SB7 · $\overline{C7}$ + ADF · $\overline{RB7}$ · SB7 · C7 + ADF · RB7 · $\overline{SB7}$ · $\overline{C7}$ + ANF · RB7 · SB7 + CMFE · $\overline{RB7}$ + EOF · RB7 · $\overline{SB7}$ + EOF · $\overline{RB7}$ · SB7 + IOF · RB7 + IOF · SB7 + RL4 · RB4 + RL4 · SB4 + RLL · RB6 + RLL · SB6 + RSM6-9 · SRA7 + SLM · RB6 + SLM · SB6 + SRM · RB8 + SRM · SB8
TB8 (T Bus Bit 8)	A103-69 A104-81	A103-69	= ADF · RB8 · SB8 · C8 + ADF · $\overline{RB8}$ · SB8 · $\overline{C8}$ + ADF · $\overline{RB8}$ · $\overline{SB8}$ · C8 + ADF · RB8 · $\overline{SB8}$ · $\overline{C8}$ + ANF · RB8 · SB8 + CMFE · $\overline{RB8}$ + EOF · RB8 · $\overline{SB8}$ + EOF · $\overline{RB8}$ · SB8 + IOF · RB8 + IOF · SB8 + RL4 · RB5 + RL4 · SB5 + RLL · RB7 + RLL · SB7 + RSM6-9 · SRA8 + SLM · RB7 + SLM · SB7 + SRM · RB9 + SRM · SB9
TB9 (T Bus Bit 9)	A103-13 A104-75	A103-13	= ADF · RB9 · SB9 · C9 + ADF · $\overline{RB9}$ · SB9 · $\overline{C9}$ + ADF · $\overline{RB9}$ · $\overline{SB9}$ · C9 + ADF · RB9 · $\overline{SB9}$ · $\overline{C9}$ + ANF · RB9 · SB9 + CMFE · $\overline{RB9}$ + EOF · RB9 · $\overline{SB9}$ + EOF · $\overline{RB9}$ · SB9 + IOF · RB9 + IOF · SB9 + RL4 · RB5 + RL4 · SB5 + RLL · RB8 + RLL · SB8 + RSM6-9 · SRA9 + SLM · RB8 + SLM · SB8 + SRM · RB10 + SRM · SB10

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB10 (T Bus Bit 10)	A103-55 A104-84	A103-55	= ADF · RB10 · SB10 · C10 + ADF · $\overline{RB10}$ · SB10 · $\overline{C10}$ + ADF · $\overline{RB10}$ · $\overline{SB10}$ · C10 + ADF · RB10 · $\overline{SB10}$ · $\overline{C10}$ + ANF · RB10 · SB10 + CMFE · $\overline{RB10}$ + EOF · RB10 · $\overline{SB10}$ + EOF · $\overline{RB10}$ · SB10 + IOF · RB10 + IOF · SB10 + RL4 · RB6 + RL4 · SB6 + RLL · RB9 + RLL · SB9 + RSM6-9 · SRA10 + SLM · RB9 + SLM · SB9 + SRM · RB11 + SRM · SB11
TB11 (T Bus Bit 11)	A102-77 A103-17 A104-45	A103-17	= ADF · RB11 · SB11 · C11 + ADF · $\overline{RB11}$ · SB11 · $\overline{C11}$ + ADF · $\overline{RB11}$ · $\overline{SB11}$ · C11 + ADF · RB11 · $\overline{SB11}$ · $\overline{C11}$ + ANF · RB11 · SB11 + CMFE · $\overline{RB11}$ + EOF · RB11 · $\overline{SB11}$ + EOF · $\overline{RB11}$ · SB11 + IOF · RB11 + IOF · SB11 + RL4 · RB7 + RL4 · SB7 + RLL · RB10 + RLL · SB10 + RSM6-9 · SRA11 + SLM · RB10 + SLM · SB10 + SRM · RB12 + SRM · SB12
TB12 (T Bus Bit 12)	A102-69 A103-81	A102-69 A108-76	= ADF · RB12 · SB12 · C12 + ADF · $\overline{RB12}$ · SB12 · $\overline{C12}$ + ADF · $\overline{RB12}$ · $\overline{SB12}$ · C12 +ADF · RB12 · $\overline{SB12}$ · $\overline{C12}$ + ANF · RB12 · SB12 + CMFE · $\overline{RB12}$ + EOF · RB12 · $\overline{SB12}$ + EOF · $\overline{RB12}$ · SB12 + IOF · RB12 + IOF · SB12 + RL4 · RB8 + RL4 · SB8 + RLL · RB11 + RLL · SB11 + RSM6-9 · SRA12 + SLM · RB11 + SLM · SB11 + SRM · RB13 + SRM · SB13

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB13 (T Bus Bit 13)	A102-13 A103-75	A102-13 A108-73	= ADF · RB13 · SB13 · C13 + ADF · $\overline{RB13}$ · SB13 · $\overline{C13}$ + ADF · $\overline{RB13}$ · $\overline{SB13}$ · C13 + ADF · RB13 · $\overline{SB13}$ · $\overline{C13}$ + ANF · RB13 · SB13 + CMFE · $\overline{RB13}$ + EOF · RB13 · SB13 + EOF · $\overline{RB13}$ · SB13 + IOF · RB13 + IOF · SB13 + RL4 · RB9 + RL4 · SB9 + RLL · RB12 + RLL · SB12 + RSM6-9 · SRA13 + SLM · RB12 + SLM · SB12 + SRM · RB14 + SRM · SB14
TB14 (T Bus Bit 14)	A102-55 A103-84	A102-55 A108-70	= ADF · RB14 · SB14 · C14 + ADF · $\overline{RB14}$ · SB14 · $\overline{C14}$ + ADF · $\overline{RB14}$ · $\overline{SB14}$ · C14 + ADF · RB14 · $\overline{SB14}$ · $\overline{C14}$ + ANF · RB14 · SB14 + CMFE · $\overline{RB14}$ + EOF · RB14 · $\overline{SB14}$ + EOF · $\overline{RB14}$ · SB14 + IOF · RB14 + IOF · SB14 + RL4 · RB10 + RL4 · SB10 + RLL · RB13 + RLL · SB13 + RSM6-9 · SRA14 + SLM · RB13 + SLM · SB13 + SRM · RB15 + SRM · SB15
TB15 (T Bus Bit 15)	A102-17 A103-45 A105-77 A108-20 A110-80	A102-17 A108-20 A109-64 A110-80	= ADF · RB15 · SB15 · C15 + ADF · $\overline{RB15}$ · SB15 · $\overline{C15}$ + ADF · $\overline{RB15}$ · $\overline{SB15}$ · C15 + ADF · RB15 · $\overline{SB15}$ · $\overline{C15}$ + ANF · RB15 · SB15 + CMFE · $\overline{RB15}$ + EOF · RB15 · $\overline{SB15}$ + EOF · $\overline{RB15}$ · SB15 + IOF · RB15 + IOF · SB15 + RL4 · RB11 + RL4 · SB11 + RLL · RB14 + RLL · SB14 + RSM6-9 · SRA15 + SLM · RB14 + SLM · SB14 (Continued on next page)

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
TB15 (Continued)			+ SRG · T3 · $\overline{TR8}$ · $\overline{TR7}$ · RB15(B) + SRG · T5 · $\overline{TR2}$ · $\overline{TR1}$ · RB15(B) + SRG · EFF · T3 · TR8 · $\overline{TR7}$ · TR6 + SRG · EFF · T5 · TR2 · $\overline{TR1}$ · TR0 + SRM · RB0 + SRM · SB0 + EAU option signal
TR8 (T-Register Bit 8)	A103-58	A5-34 A15-32 A107-29 A108-18 A109-78	= TR8 FF, set-side output
$\overline{TR8}$ ("not" T-Register Bit 8)	A103-54	A7-75 A12-75 A15-30 A17-75 A22-75 A108-36	= TR8 FF, clear-side output
TR8 FF (T-Register Bit 8 FF)			J = TB8 K = $\overline{TB8}$ Clock = STBT Direct Set = ST8 Direct Clear = RST
TR9 (T-Register Bit 9)	A103-9	A5-43 A15-31 A108-17 A109-61	= TR9 FF, set-side output
$\overline{TR9}$ ("not" T-Register Bit 9)	A103-10	A7-76 A12-76 A15-29 A17-76 A22-76 A107-57	= TR9 FF, clear-side output
TR9 FF (T-Register Bit 9 FF)			J = TB9 K = $\overline{TB9}$ Clock = STBT Direct Set = ST9 Direct Clear = RST
TR10 (T-Register Bit 10)	A103-56	A5-46 A15-22 A107-9	= TR10 FF, set-side output
$\overline{TR10}$ ("not" T-Register Bit 10)	A103-53	A7-74 A12-74 A15-20 A17-74 A22-74	= TR10 FF, clear-side output
TR10 FF (T-Register Bit 10 FF)			J = TB10 K = $\overline{TB10}$ Clock = STBT Direct Set = ST10 Direct Clear = RST

Table 7-35. A103 Arithmetic Logic Card (Bits 11-8), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TR11 (T-Register Bit 11)	A103-16	A5-50 A15-21 A107-14 A108-43 A109-84	= TR11 FF, set-side output
$\overline{\text{TR11}}$ ("not" T-Register Bit 11)	A103-15	A7-80 A12-80 A15-19 A17-80 A22-80 A108-55 A109-70	= TR11 FF, clear-side output
TR11 FF (T-Register Bit 11 FF)	--	--	J = $\overline{\text{TB11}}$ K = $\overline{\text{TB11}}$ Clock = STBT Direct Set = ST11 Direct Clear = RST
TRD8 (T-Register Display Bit 8)	A103-21* A103-Y*	A501DS9	= TR8 FF, set-side output
TRD9 (T-Register Display Bit 9)	A103-22* A103-Z*	A501DS10	= TR9 FF, set-side output
TRD10 (T-Register Display Bit 10)	A103-20* A103=X*	A501DS11	= TR10 FF, set-side output
TRD11 (T-Register Display Bit 11)	A103-16*	A501DS12	= TR11 FF, set-side output

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A104-47 A104-48	None
+4.5V	A100E1	A104-39 A104-40	None
ADF (Add Function)	A4-82 A107-75 A110-12	A104-5	See source or option
ANF (And Function)	A107-56	A104-72	See source
AR4 FF (A-Register Bit 4 FF)			J = $\overline{TB4}$ K = $\overline{\overline{TB4}}$ Clock = STBA
AR5 FF (A-Register Bit 5 FF)			J = $\overline{TB5}$ K = $\overline{\overline{TB5}}$ Clock = STBA
AR6 FF (A-Register Bit 6 FF)			J = $\overline{TB6}$ K = $\overline{\overline{TB6}}$ Clock = STBA
AR7 FF (A-Register Bit 7 FF)			J = $\overline{TB7}$ K = $\overline{\overline{TB7}}$ Clock = STBA
ARD4 (A-Register Display Bit 4)	A104-7* A104-H*	A501DS53	= AR4 FF, set-side output
ARD5 (A-Register Display Bit 5)	A104-8* A104-J*	A501DS54	= AR4 FF, set-side output
ARD6 (A-Register Display Bit 6)	A104-9* A104-K*	A501DS55	= AR6 FF, set-side output
ARD7 (A-Register Display Bit 7)	A104-10* A104-L*	A501DS56	= AR7 FF, set-side output
BR4 FF (B-Register Bit 4 FF)			J = $\overline{TB4}$ K = $\overline{\overline{TB4}}$ Clock = STBB
BR5 FF (B-Register Bit 5 FF)			J = $\overline{TB5}$ K = $\overline{\overline{TB5}}$ Clock = STBB
BR6 FF (B-Register Bit 6 FF)			J = $\overline{TB6}$ K = $\overline{\overline{TB6}}$ Clock = STBB
BR7 FF (B-Register Bit 7 FF)			J = $\overline{TB7}$ K = $\overline{\overline{TB7}}$ Clock = STBB
BRD4 (B-Register Display Bit 4)	A104-6* A104-F*	A501DS69	= BR4 FF, set-side output
BRD5 (B-Register Display Bit 5)	A104-5* A104-E*	A501DS70	= BR5 FF, set-side output

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
BRD6 (B-Register Display Bit 6)	A104-4* A104-D*	A501DS71	= BR6 FF, set-side output
BRD7 (B-Register Display Bit 7)	A104-3* A104-C*	A501-DS72	= BR7 FF, set-side output
C4 (Carry Bit 4)	A105-36	A104-67	See source
C8 (Carry Bit 4)	A104-36	A103-67	= C7 · RB7 + C7 · SB7 + RB7 · SB7
$\overline{\text{CMF}}$ ("not" Complement Function)	A14-79	A104-64	See source
$\overline{\text{EOF}}$ ("not" Exclusive OR Function)	A14-75	A104-76	See source
GND (Ground), Card Input	A100E2	A104-1 A104-2 A104-85 A104-86	None
GND (Ground), Card Output	A104-1* A104-2* A104-A* A104-B*	A501-1 A501-2	None
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	See source or option
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	See source or option
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	See source or option

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	See source or option
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60	A1-36 A2-36 A3-63 A5-42 A16-26 A203-42 thru A218-42 A219-57	= IOCO · RB4 + DMA option signal + MP option signal
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50	A1-42 A2-42 A3-61 A5-51 A16-28 A203-51 thru A218-51 A219-59	= IOCO · RB5 + DMA option signal + MP option signal
IOBO 6 (Input/Output Bus, Output Bit 6)	A104-57	A1-52 A2-52 A5-53 A16-22 A203-53 thru A218-53 A219-61	= IOCO · RB6 + DMA option signal + MP option signal
IOBO 7 (Input/Output Bus, Output Bit 7)	A104-35	A1-50 A2-50 A5-52 A16-20 A203-52 thru A218-52 A219-63	= IOCO · RB7 + DMA option signal + MP option signal
IOCO (Input/Output Control, Output)	A108-34	A104-70	See source
$\overline{\text{IOF}}$ ("not" Inclusive OR Function)	A107-84	A104-73	See source
IOI (Input/Output, Input)	A4-81 A4-84 A108-44	A104-31	See source or option
MR4 (M-Register Bit 4)	A104-68	A14-20 A16-30	= MR4 FF, set-side output

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
$\overline{MR4}$ ("not" M-Register Bit 4)	A104-63	None	= MR4 FF, clear-side output
MR4 FF (M-Register Bit 4 FF)			J = TB4 K = $\overline{TB4}$ Clock = STM0-5
MR5 (M-Register Bit 5)	A104-18	A14-24 A16-42	= MR5 FF, set-side output
$\overline{MR5}$ ("not" M-Register Bit 5)	A104-19	None	= MR5 FF, clear-side output
MR5 FF (M-Register Bit 5 FF)			J = TB5 K = $\overline{TB5}$ Clock = STM0-5
MR6 (M-Register Bit 6)	A104-65	A14-28 A16-37	= MR6 FF, set-side output
$\overline{MR6}$ ("not" M-Register Bit 6)	A104-66	None	= MR6 FF, clear-side output
MR6 FF (M-Register Bit 6 FF)			J = TB6 K = $\overline{TB6}$ Clock = STM6-9
MR7 (M-Register Bit 7)	A104-25	A14-32 A16-32	= MR7 FF, set-side output
$\overline{MR7}$ ("not" M-Register Bit 7)	A104-24	None	= MR7 FF, clear-side output
MR7 FF (M-Register Bit 7 FF)			J = TB7 K = $\overline{TB7}$ Clock = STM6-9
MRD4 (M-Register Display Bit 4)	A104-11* A104-M*	A501DS37	= MR4 FF, set-side output
MRD5 (M-Register Display Bit 5)	A104-12* A104-N*	A501DS38	= MR5 FF, set-side output
MRD6 (M-Register Display Bit 6)	A104-14* A104-R*	A501DS39	= MR6 FF, set-side output
MRD7 (M-Register Display Bit 7)	A104-13* A104-P*	A501DS40	= MR7 FF, set-side output
PR4 FF (P-Register Bit 4 FF)			J = TB4 K = $\overline{TB4}$ Clock = STP0-9
PR5 FF (P-Register Bit 5 FF)			J = TB5 K = $\overline{TB5}$ Clock = STP0-9
PR6 FF (P-Register Bit 6 FF)			J = TB6 K = $\overline{TB6}$ Clock = STP0-9

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PR7 FF (P-Register Bit 6 FF)			J = TB7 K = $\overline{TB7}$ Clock = STP0-9
PRD4 (P-Register Display Bit 4)	A104-15* A104-S*	A501DS21	= PR4 FF, set-side output
PRD5 (P-Register Display Bit 5)	A104-18* A104-V*	A501DS22	= PR5 FF, set-side output
PRD6 (P-Register Display Bit 6)	A104-19* A104-W*	A501DS23	= PR6 FF, set-side output
PRD7 (P-Register Display Bit 7)	A104-17* A104-U*	A501DS24	= PR7 FF, set-side output
RARB (Read A-Register to the R Bus)	A107-19 A110-65	A104-34	See source or option
RB4 (R Bus Bit 4)	A104-37	None	= RARB · AR4 FF + RBRB · BR4 FF + RPRB · PR4 FF
RB5 (R Bus Bit 5)	A104-62	None	= RARB · AR5 FF + RBRB · BR5 FF + RPRB · PR5 FF
RB6 (R Bus Bit 6)	A104-71	None	= RARB · AR6 FF + RBRB · BR6 FF + RPRB · PR6 FF
RB7 (R Bus Bit 7)	A104-30	None	= RARB · AR7 FF + RBRB · BR7 FF + RPRB · PR7 FF
RBRB (Read B-Register to the R Bus)	A107-18 A110-58	A104-28	See source or option
$\overline{RL4}$ ("not" Rotate Left 4 Bits)	A108-28	A104-78	See source or option
RMSB (Read M-Register to the S Bus)	A107-68 A110-34	A104-8	See source or option
RPRB (Read P-Register to the R Bus)	A107-72 A110-4	A104-12	See source or option
RSM6-9 (Reset M-Register Bits 6 thru 9)	A107-12	A104-21	See source
RST (Reset T-Register)	A107-58	A104-7	See source
RTSB (Read T-Register to the S Bus)	A107-82 A110-19	A104-20	See source or option
SB4 (S Bus Bit 4)	A104-42	None	= IOI · IOBI 4 + RMSB · MR4 + RTSB · TR4

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SB5 (S Bus Bit 5)	A104-59	None	= IOI · IOBI 5 + RMSB · MR5 + RTSB · TR5
SB6 (S Bus Bit 6)	A104-61	None	= IOI · IOBI 6 + RMSB · MR6 + RTSB · TR6
SB7 (S Bus Bit 7)	A104-6	None	= IOI · IOBI 7 + RMSB · MR7 + RTSB · TR7
$\overline{\text{SLM}}$ ("not" Shift Left Magnitude)	A14-77	A104-41 A104-80 A104-82	See source
$\overline{\text{SRM}}$ ("not" Shift Left Magnitude)	A14-78	A104-74 A104-83	See source
ST4 (Set T-Register Bit 4)	A13-21	A104-49	See source
ST4 GND (Set T-Register Bit 4, Ground Return)	A13-22	A104-1	None
ST5 (Set T-Register Bit 5)	A13-25	A104-2	See source
ST5 GND (Set T-Register Bit 5, Ground Return)	A13-26	A104-2	None
ST6 (Set T-Register Bit 6)	A13-29	A104-52	See source
ST6 GND (Set T-Register Bit 6, Ground Return)	A13-30	A104-2	None
ST7 (Set T-Register Bit 7)	A13-33	A104-11	See source
ST7 GND (Set T-Register Bit 7, Ground Return)	A13-34	A104-1	None
STBA (Store T Bus in A-Register)	A107-50	A104-38	See source
STBB (Store T Bus in B-Register)	A107-51	A104-26	See source
STBT (Store T Bus in T-Register)	A107-63	A104-51	See source
STM0-5 (Store T Bus Bits 0 thru 5 in M-Register)	A107-20	A104-29	See source
STM6-9 (Store T Bus Bit 6 thru 9 in M-Register)	A107-21	A104-22	See source
STP0-9 (Store T Bus Bits 0 thru 9 in P-Register)	A107-7	A104-23 A104-44	See source
TAN2 (T Bus Bits 4 thru 7 "anded")	A104-43	A108-57	= $\overline{\text{TB7}} \cdot \overline{\text{TB6}} \cdot \overline{\text{TB5}} \cdot \overline{\text{TB4}}$

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB3 (T Bus Bit 3)	A102-45 A104-77 A105-17 A202-7	A105-17 A108-78	= ADF · RB3 · SB3 · C3 + ADF · RB3 · $\overline{SB3}$ · $\overline{C3}$ + $\overline{ADF}$ · $\overline{RB3}$ · $\overline{SB3}$ · C3 + ADF · $\overline{RB3}$ · SB3 · $\overline{C3}$ + ANF · RB3 · SB3 + CMFE · $\overline{RB3}$ + EOF · RB3 · $\overline{SB3}$ + EOF · $\overline{RB3}$ · SB3 + IOF · RB3 + IOF · SB3 + RL4 · RB15 + RL4 · SB15 + RLL · RB2 + RLL · SB2 + RSM6-9 · SRA3 + SLM · RB2 + SLM · SB2 + SRM · RB4 + SRM · SB4
TB4 (T Bus Bit 4)	A104-69 A105-81 A202-6	A104-69	= ADF · RB4 · SB4 · C4 + ADF · $\overline{RB4}$ · SB4 · $\overline{C4}$ + ADF · $\overline{RB4}$ · $\overline{SB4}$ · C4 + ADF · RB4 · $\overline{SB4}$ · $\overline{C4}$ + ANF · RB4 · SB4 + CMFE · $\overline{RB4}$ + EOF · RB4 · $\overline{SB4}$ + EOF · $\overline{RB4}$ · SB4 + IOF · RB4 + IOF · SB4 + RL4 · RB1 + RL4 · SB1 + RLL · RB3 + RLL · SB3 + RSM6-9 · SRA4 + SLM · RB3 + SLM · SB3 + SRM · RB5 + SRM · SB5
TB5 (T Bus Bit 5)	A104-13 A105-75 A202-5	A104-13	= ADF · RB5 · SB5 · C5 + ADF · $\overline{RB5}$ · SB5 · $\overline{C5}$ + ADF · $\overline{RB5}$ · $\overline{SB5}$ · C5 + ADF · RB5 · $\overline{SB5}$ · $\overline{C5}$ + ANF · RB5 · SB5 + CMFE · $\overline{RB5}$ + EOF · RB5 · $\overline{SB5}$ + EOF · $\overline{RB5}$ · SB5 + IOF · RB5 + IOF · SB5 + RL4 · RB2 + RL4 · SB2 + RLL · RB4 + RLL · SB4 + RSM6-9 · SRA5 + SLM · RB4 + SLM · SB4 + SRM · RB6 + SRM · SB6

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB6 (T Bus Bit 6)	A104-55 A105-84	A104-55	= ADF · RB6 · SB6 · C6 + ADF · $\overline{RB6}$ · SB6 · $\overline{C6}$ + ADF · $\overline{RB6}$ · $\overline{SB6}$ · C6 + ADF · RB6 · $\overline{SB6}$ · $\overline{C6}$ + ANF · RB6 · SB6 + CMFE · $\overline{RB6}$ + EOF · RB6 · $\overline{SB6}$ + EOF · $\overline{RB6}$ · SB6 + IOF · RB6 + IOF · SB6 + RL4 · RB3 + RL4 · SB3 + RLL · RB5 + RLL · SB5 + RSM6-9 : SRA6 + SLM · RB5 + SLM · SB6 + SRM · RB7 + SRM · SB7
TB7 (T Bus Bit 7)	A103-77 A104-17 A105-45	A104-17	= ADF · RB7 · SB7 · C7 + ADF · $\overline{RB7}$ · SB7 · $\overline{C7}$ + ADF · $\overline{RB7}$ · $\overline{SB7}$ · C7 + ADF · RB7 · $\overline{SB7}$ · $\overline{C7}$ + ANF · RB7 · SB7 + CMFE · $\overline{RB7}$ + EOF · RB7 · $\overline{SB7}$ † EOF · $\overline{RB7}$ · SB7 + IOF · RB7 + IOF · SB7 + RL4 · RB4 + RL4 · SB4 + RLL · RB6 + RLL · SB6 + RSM6-9 · SRA7 + SLM · RB6 + SLM · SB6 + SRM · RB8 + SRM · SB8
TB8 (T Bus Bit 8)	A103-69 A104-81	A103-69	= ADF · RB8 · SB8 · C8 + ADF · $\overline{RB8}$ · SB8 · $\overline{C8}$ + ADF · $\overline{RB8}$ · $\overline{SB8}$ · C8 + ADF · RB8 · $\overline{SB8}$ · $\overline{C8}$ + ANF · RB8 · SB8 + CMFE · $\overline{RB8}$ + EOF · RB8 · $\overline{SB8}$ + EOF · $\overline{RB8}$ · SB8 + IOF · RB8 + IOF · SB8 + RL4 · RB5 + RL4 · SB5 + RLL · RB7 + RLL · SB7 + RSM6-9 · SRA8 + SLM · RB7 + SLM · SB7 + SRM · RB9 + SRM · SB9

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
TB9 (T Bus Bit 9)	A103-13 A104-75	A103-13	= ADF · RB9 · SB9 · $\overline{C9}$ + ADF · $\overline{RB9}$ · SB9 · $\overline{C9}$ + ADF · $\overline{RB9}$ · $\overline{SB9}$ · C9 + ADF · RB9 · $\overline{SB9}$ · $\overline{C9}$ + ANF · RB9 · SB9 + CMFE · $\overline{RB9}$ + EOF · RB9 · $\overline{SB9}$ + EOF · $\overline{RB9}$ · SB9 + IOF · RB9 + IOF · SB9 + RL4 · RB5 + RL4 · SB5 + RLL · RB8 + RLL · SB8 + RSM6-9 · SRA9 + SLM · RB8 + SLM · SB8 + SRM · RB10 + SRM · SB10
TB10 (T Bus Bit 10)	A103-55 A104-84	A103-55	= ADF · RB10 · SB10 · C10 + ADF · $\overline{RB10}$ · SB10 · $\overline{C10}$ + ADF · $\overline{RB10}$ · $\overline{SB10}$ · C10 + ADF · RB10 · $\overline{SB10}$ · $\overline{C10}$ + ANF · RB10 · SB10 + CMFE · $\overline{RB10}$ + EOF · RB10 · $\overline{SB10}$ + EOF · $\overline{RB10}$ · SB10 + IOF · RB10 + IOF · SB10 + RL4 · RB6 + RL4 · SB6 + RLL · RB9 + RLL · SB9 + RSM6-9 · SRA10 + SLM · RB9 + SLM · SB9 + SRM · RB11 + SRM · SB11
TB11 (T Bus Bit 11)	A102-77 A103-17 A104-45	A103-17	= ADF · RB11 · SB11 · C11 + ADF · $\overline{RB11}$ · SB11 · $\overline{C11}$ + ADF · $\overline{RB11}$ · $\overline{SB11}$ · C11 + ADF · RB11 · $\overline{SB11}$ · $\overline{C11}$ + ANF · RB11 · SB11 + CMFE · $\overline{RB11}$ + EOF · RB11 · $\overline{SB11}$ + EOF · $\overline{RB11}$ · SB11 + IOF · RB11 + IOF · SB11 + RL4 · RB7 + RL4 · SB7 + RLL · RB10 + RLL · SB10 + RSM6-9 · SRA11 + SLM · RB10 + SLM · SB10 + SRM · RB12 + SRM · SB12

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
TR4 (T-Register Bit 4)	A104-58	A5-11 A15-68 A107-25 A109-72 A202-81	= TR4 FF, set-side output
$\overline{\text{TR4}}$ ("not" T-Register Bit 4)	A104-54	A7-81 A12-81 A15-66 A17-81 A22-81 A108-79 A202-78	= TR4 FF, clear-side output
TR4 FF (T-Register Bit 4 FF)			J = $\overline{\text{TB4}}$ K = $\overline{\overline{\text{TB4}}}$ Clock = STBT Direct Set = ST4 Direct Clear = RST
TR5 (T-Register Bit 5)	A104-9	A5-13 A15-67 A109-69 A202-58	= TR5 FF, set-side output
$\overline{\text{TR5}}$ ("not" T-Register Bit 5)	A104-10	A7-77 A12-77 A15-65 A17-77 A22-77 A108-6 A202-79	= TR5 FF, clear-side output
TR5 FF (T-Register Bit 5 FF)			J = $\overline{\text{TB5}}$ K = $\overline{\overline{\text{TB5}}}$ Clock = STBT Direct Set = ST5 Direct Clear = RST
TR6 (T-Register Bit 6)	A104-56	A5-15 A15-58 A108-3 A109-66	= TR6 FF, set-side output
$\overline{\text{TR6}}$ ("not" T-Register Bit 6)	A104-53	A7-79 A12-79 A15-56 A17-79 A22-79 A107-55 A108-23	= TR6 FF, clear-side output
TR6 FF (T-Register Bit 6 FF)			J = $\overline{\text{TB6}}$ K = $\overline{\overline{\text{TB6}}}$ Clock = STBT Direct Set = ST6 Direct Clear = RST

Table 7-36. A104 Arithmetic Logic Card (Bits 7-4), Sginal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TR7 (T-Register Bit 7)	A104-16	A5-17 A15-57 A108-11 A109-83	= TR7 FF, set-side output
$\overline{\text{TR7}}$ ("not" T-Register Bit 7)	A104-15	A7-73 A12-73 A15-55 A17-73 A22-73 A107-23 A108-30	= TR7 FF, clear-side output
TR7 FF (T-Register Bit 7 FF)			J = TB7 K = $\overline{\text{TB7}}$ Clock = STBT Direct Set = ST7 Direct Clear = RST
TRD4 (T-Register Display Bit 4)	A104-21* A104-Y*	A501DS5	= TR4 FF, set-side output
TRD5 (T-Register Display Bit 5)	A104-22* A104-Z*	A501DS6	= TR5 FF, set-side output
TRD6 (T-Register Display Bit 6)	A104-20* A104-X*	A501DS7	= TR6 FF, set-side output
TRD7 (T-Register Display Bit 7)	A104-16* A104-T*	A501DS8	= TR7 FF, set-side output

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A105-47 A105-48	None
+4.5V	A100E1	A105-39 A105-40	None
ADF (Add Function)	A4-82 A107-75 A110-12	A105-5	See source or option
ANF (And Function)	A107-56	A105-72	See source
AR0 FF (A-Register Bit 0 FF)			J = $\overline{TB0}$ K = $\overline{TB0}$ Clock = STBA
AR1 FF (A-Register Bit 1 FF)			J = $\overline{TB1}$ K = $\overline{TB1}$ Clock = STBA
AR2 FF (A-Register Bit 2 FF)			J = $\overline{TB2}$ K = $\overline{TB2}$ Clock = STBA
AR3 FF (A-Register Bit 3 FF)			J = $\overline{TB3}$ K = $\overline{TB3}$ Clock = STBA
ARD0 (A-Register Display Bit 0)	A105-7* A105-H*	A501DS49	= AR0 FF, set-side output
ARD1 (A-Register Display Bit 1)	A105-8* A105-J*	A501DS50	= AR1 FF, set-side output
ARD2 (A-Register Display Bit 2)	A105-9* A105-K*	A501DS51	= AR2 FF, set-side output
ARD3 (A-Register Display Bit 3)	A105-10* A105-L*	A501DS52	= AR3 FF, set-side output
BR0 FF (B-Register Bit 0 FF)			J = $\overline{TB0}$ K = $\overline{TB0}$ Clock = STBB
BR1 FF (B-Register Bit 1 FF)			J = $\overline{TB1}$ K = $\overline{TB1}$ Clock = STBB
BR2 FF (B-Register Bit 2 FF)			J = $\overline{TB2}$ K = $\overline{TB2}$ Clock = STBB
BR3 FF (B-Register Bit 3 FF)			J = $\overline{TB3}$ K = $\overline{TB3}$ Clock = STBB
BRD0 (B-Register Display Bit 0)	A105-6* A105-F*	A501DS65	= BR0 FF, set-side output
BRD1 (B-Register Display Bit 1)	A105-5* A105-E*	A501DS66	= BR1 FF, set-side output

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
BRD2 (B-Register Display Bit 2)	A105-4* A105-D*	A501DS67	= BR2 FF, set-side output
BRD3 (B-Register Display Bit 3)	A105-3* A105-C*	A501DS68	= BR3 FF, set-side output
C0 (Carry Bit 0)	A108-71	A105-67	See source
C4 (Carry Bit 4)	A105-36	A104-67	= C3 · RB3 + C3 · SB3 + RB3 · SB3
$\overline{\text{CMF}}$ ("not" Complement Function)	A14-79	A105-64	See source
$\overline{\text{EOF}}$ ("not" Exclusive OR Function)	A14-75	A105-76	See source
GND (Ground), Card Input	A100E2	A105-1 A105-2 A105-85 A105-86	None
GND (Ground), Card Output	A105-1* A105-2* A105-A* A105-B*	A501-1 A501-2	None
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	See source or option
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-70 A202-28 A203-29 thru A218-29 A220-52	A105-32	See source or option
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	See source or option

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOBI3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	See source or option
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60	A1-24 A2-24 A3-21 A5-35 A16-6 A203-35 thru A218-35 A219-49	= IOCO ; RB0 + DMA option signal + MP option signal
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50	A1-26 A2-26 A3-42 A5-38 A16-5 A203-38 thru A218-38 A219-51	= IOCO · RB1 + DMA option signal + MP option signal
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57	A1-32 A2-32 A3-65 A5-41 A16-4 A203-41 thru A218-41 A219-53	= IOCO · RB2 + DMA option signal + MP option signal
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35	A1-34 A2-34 A3-35 A5-45 A16-3 A203-45 thru A218-45 A219-55	= IOCO · RB3 + DMA option signal + MP option signal
IOCO (Input/Output Control, Output)	A108-34	A105-70	See source
$\overline{\text{IOF}}$ ("not" Inclusive OR Function)	A107-84	A105-73	See source
IOI (Input/Output, Input)	A4-81 A4-84 A108-44	A105-31	See source or option

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
MR0 (M-Register Bit 0)	A105-68	A14-4 A16-14	= MR0 FF, set-side output
$\overline{\text{MR0}}$ ("not" M-Register Bit 0)	A105-63	None	= MR0 FF, clear-side output
MR0 FF (M-Register Bit 0 FF)			J = TB0 K = $\overline{\text{TB0}}$ Clock = STM0-5
MR1 (M-Register Bit 1)	A105-18	A14-8 A16-10	= MR1 FF, set-side output
$\overline{\text{MR1}}$ ("not" M-Register Bit 1)	A105-19	None	= MR1 FF, clear-side output
MR1 FF (M-Register Bit 1 FF)			J = TB1 K = $\overline{\text{TB1}}$ Clock = STM0-5
MR2 (M-Register Bit 2)	A105-65	A14-12 A16-8	= MR2 FF, set-side output
$\overline{\text{MR2}}$ ("not" M-Register Bit 2)	A105-66	None	= MR2 FF, clear-side output
MR2 FF (M-Register Bit 2 FF)			J = TB2 K = $\overline{\text{TB2}}$ Clock = STM0-5
MR3 (M-Register Bit 3)	A105-25	A14-16 A16-18	= MR3 FF, set-side output
$\overline{\text{MR3}}$ ("not" M-Register Bit 3)	A105-24	None	= MR3 FF, clear-side output
MR3 FF (M-Register Bit 3 FF)			J = TB3 K = $\overline{\text{TB3}}$ Clock = STM0-5
MRD0 (M-Register Display Bit 0)	A105-11* A105-M*	A501DS33	= MR0 FF, set-side output
MRD1 (M-Register Display Bit 1)	A105-12* A105-N*	A501DS34	= MR1 FF, set-side output
MRD2 (M-Register Display Bit 2)	A105-14* A105-R*	A501DS35	= MR2 FF, set-side output
MRD3 (M-Register Display Bit 3)	A105-13* A105-P*	A501DS36	= MR3 FF, set-side output
PR0 FF (P-Register Bit 0 FF)			J = TB0 K = $\overline{\text{TB0}}$ Clock = STP0-9
PR1 FF (P-Register Bit 1 FF)			J = TB1 K = $\overline{\text{TB1}}$ Clock = STP0-9

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PR2 FF (P-Register Bit 2 FF)			J = TB2 K = $\overline{TB2}$ Clock = STP0-9
PR3 FF (P-Register Bit 3 FF)			J = TB3 K = $\overline{TB3}$ Clock = STP0-9
PRD0 (P-Register Display Bit 0)	A105-15* A105-S*	A501DS17	= PR0 FF, set-side output
PRD1 (P-Register Display Bit 1)	A105-18* A105-V*	A501DS18	= PR1 FF, set-side output
PRD2 (P-Register Display Bit 2)	A105-19* A105-W*	A501DS19	= PR2 FF, set-side output
PRD3 (P-Register Display Bit 3)	A105-17* A105-U*	A501DS20	= PR3 FF, set-side output
RARB (Read A-Register to the R Bus)	A107-19 A110-65	A105-34	See source or option
RB0 (R Bus Bit 0)	A105-37 A107-61 A110-43	A105-37	= ISZ · PH3 · T3T4 + RARB · AR0 FF + RBRB · BR0 FF + RPRB · PR0 FF + EAU option signal
RB1 (R Bus Bit 1)	A105-62	None	= RARB · AR1 FF + RBRB · BR1 FF + RPRB · PR1 FF
RB2 (R Bus Bit 2)	A105-71	None	= RARB · AR2 FF + RBRB · BR2 FF + RPRB · PR2 FF
RB3 (R Bus Bit 3)	A105-30	None	= RARB · AR3 FF + RBRB · BR3 FF + RPRB · PR3 FF
RBRB (Read B-Register to the R Bus)	A107-18 A110-58	A105-28	See source or option
$\overline{RL4}$ ("not" Rotate Left 4 Bits)	A108-28	A105-78	See source
RMSB (Read M-Register to the S Bus)	A107-68 A110-34	A105-8	See source or option
RPRB (Read P-Register to the R Bus)	A107-72 A110-4	A105-12	See source or option
$\overline{RRS}$ ("not" Rotate Right to Sign Bit)	A108-41	A105-83	See source
RST (Reset T-Register)	A107-58	A105-7	See source
RTSB (Read T-Register to the S Bus)	A107-32 A110-49	A105-20	See source or option

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
SB0 (S Bus Bit 0)	A105-42 A107-81 A110-44	A105-42	= ASG · T4T5 · $\overline{T6T7}$ · TR2 + ASG ; ILS · T4T5 · TR2 + JSB · PH3 · T1T2 · $\overline{T6T7}$ + JSB · ILS · PH3 · T1T2 + PH4 · T3T4 · $\overline{T6T7}$ + PH4 · $\overline{ILS}$ · T3T4 + IOI · IOBI 0 + RMSB · MR0 + RTSB · TR0 + EAU option signal
SB1 (S Bus Bit 1)	A105-59	None	= IOI · IOBI 1 + RMSB · MR1 + RTSB · TR1
SB2 (S Bus Bit 2)	A105-61	None	= IOI · IOBI 2 + RMSB · MR2 + RTSB · TR2
SB3 (S Bus Bit 3)	A105-6	None	= IOI · IOBI 3 + RMSB · MR3 + RTSB · TR3
$\overline{SLM}$ ("not" Shift Left Magnitude)	A14-77	A105-41 A105-80 A105-82	See source
$\overline{SRM}$ ("not" Shift Right Magnitude)	A14-78	A105-74	See source
ST0 (Set T-Register Bit 0)	A13-5	A105-49	See source
ST0 GND (Set T-Register Bit 0, Ground Return)	A13-6	A105-1	None
ST1 (Set T-Register Bit 1)	A13-9	A105-4	See source
ST1 GND (Set T-Register Bit 1, Ground Return)	A13-10	A105-2	None
ST2 (Set T-Register Bit 2)	A13-13	A105-52	See source
ST2 GND (Set T-Register Bit 2, Ground Return)	A13-14	A105-2	None
ST3 (Set T-Register Bit 3)	A13-17	A105-11	See source
ST3 GND (Set T-Register Bit 3, Ground Return)	A13-18	A105-1	None
STBA (Store T Bus in A-Register)	A107-50	A105-38	See source
STBB (Store T Bus in B-Register)	A107-51	A105-26	See source
STBT (Store T Bus in T-Register)	A107-63	A105-51	See source

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
STM0-5 (Store T Bus Bits 0 thru 5 in M-Register)	A107-20	A105-22 A105-29	See source
STP0-9 (Store T Bus Bit 0 thru 9 in P-Register)	A107-7	A105-23 A105-44	See source
TAN1 (T Bus Bits 0 thru 3 "anded")	A105-43	A108-58	= $\overline{TB3} \cdot \overline{TB2} \cdot \overline{TB1} \cdot \overline{TB0}$
TB0 (T Bus Bits 0)	A102-81 A105-69 A108-51 A110-79 A202-10	A105-69 A110-79	= ADF · RB0 · SB0 · C0 + ADF · RB0 · $\overline{SB0}$ · $\overline{C0}$ + ADF · $\overline{RB0}$ · SB0 · $\overline{C0}$ + ADF · $\overline{RB0}$ · $\overline{SB0}$ · C0 + ANF · RB0 · SB0 + CMF · $\overline{RB0}$ + EFF · SRG · T3 · TR8 · TR7 · $\overline{TR6}$ + EFF · SRG · T5 · TR2 · TR1 · $\overline{TR0}$ + EOF · RB0 · $\overline{SB0}$ + EOF · $\overline{RB0}$ · SB0 + IOF · RB0 + IOF · SB0 + RL4 · RB12 + RL4 · SB12 + RLL · RB15 + RLL · SB15 + RSM6-9 · SRA0 + SLM · RB15 + SLM · SB15 + SRM · RB1 + SRM · SB1 + EAU option signal
TB1 (T Bus Bit 1)	A102-75 A105-13 A202-9	A105-13 A108-75	= ADF · RB1 · SB1 · C1 + ADF · RB1 · $\overline{SB1}$ · $\overline{C1}$ + ADF · $\overline{RB1}$ · $\overline{SB1}$ · C1 + ADF · $\overline{RB1}$ · SB1 · $\overline{C1}$ + ANF · RB1 · SB1 + CMFE · $\overline{RB1}$ + EOF · RB1 · $\overline{SB1}$ + EOF · $\overline{RB1}$ · SB1 + IOF · RB1 + IOF · SB1 + RL4 · RB13 + RL4 · SB13 + RLL · RB0 + RLL · SB0 + RSM6-9 · SRA1 + SLM · RB0 + SLM · SB0 + SRM · RB2 + SRM · SB2

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB2 (T Bus Bit 2)	A102-84 A105-55 A202-8	A105-55 A108-67	= ADF · RB2 · SB2 · C2 + ADF · RB2 · $\overline{SB2}$ · $\overline{C2}$ + ADF · $\overline{RB2}$ · $\overline{SB2}$ · C2 + ADF · $\overline{RB2}$ · SB2 · $\overline{C2}$ + ANF · RB2 · SB2 + CMFE · $\overline{RB2}$ + EOF · RB2 · $\overline{SB2}$ + EOF · $\overline{RB2}$ · SB2 + IOF · RB2 + IOF · SB2 + RL4 · RB14 + RL4 · SB14 + RLL · RB1 + RLL · SB1 + RSM6-9 · SRA2 + SLM · RB1 + SLM · SB1 + SRM · RB3 + SRM · SB3
TB3 (T Bus Bit 3)	A102-45 A104-77 A105-17 A202-7	A105-17 A108-78	= ADF · RB3 · SB3 · C3 + ADF · RB3 · $\overline{SB3}$ · $\overline{C3}$ + ADF · $\overline{RB3}$ · $\overline{SB3}$ · C3 + ADF · $\overline{RB3}$ · SB3 · $\overline{C3}$ + ANF · RB3 · SB3 + CMFE · $\overline{RB3}$ + EOF · RB3 · $\overline{SB3}$ + EOF · $\overline{RB3}$ · SB3 + IOF · RB3 + IOF · SB3 + RL4 · RB15 + RL4 · SB15 + RLL · RB2 + RLL · SB2 + RSM6-9 · SRA3 + SLM · RB2 + SLM · SB2 + SRM · RB4 + SRM · SB4
TB4 (T Bus Bit 4)	A104-69 A105-81 A202-6	A104-69	= ADF · RB4 · SB4 · C4 + ADF · $\overline{RB4}$ · SB4 · $\overline{C4}$ + ADF · $\overline{RB4}$ · $\overline{SB4}$ · C4 + ADF · RB4 · SB4 · $\overline{C4}$ + ANF · RB4 · SB4 + CMFE · $\overline{RB4}$ + EOF · RB4 · $\overline{SB4}$ + EOF · $\overline{RB4}$ · SB4 + IOF · RB4 + IOF · SB4 + RL4 · RB1 + RL4 · SB1 + RLL · RB3 + RLL · SB3 + RSM6-9 · SRA4 + SLM · RB3 + SLM · SB3 + SRM · RB5 + SRM · SB5

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB5 (T Bus Bit 5)	A104-13 A105-75 A202-5	A104-13	= ADF · RB5 · SB5 · C5 + ADF · $\overline{RB5}$ · SB5 · $\overline{C5}$ + ADF · $\overline{RB5}$ · $\overline{SB5}$ · C5 + ADF · RB5 · $\overline{SB5}$ · $\overline{C5}$ + ANF · RB5 · SB5 +CMFE · $\overline{RB5}$ + EOF · RB5 · $\overline{SB5}$ + EOF · $\overline{RB5}$ · SB5 + IOF · RB5 + IOF · SB5 + RL4 · RB2 + RL4 · SB2 + RLL · RB4 + RLL · SB4 + RSM6-9 · SRA5 + SLM · RB4 + SLM · SB4 + SRM · RB6 + SRM · SB6
TB6 (T Bus Bit 6)	A104-55 A105-84	A104-55	= ADF · RB6 · SB6 · C6 + ADF · $\overline{RB6}$ · SB6 · $\overline{C6}$ + ADF · $\overline{RB6}$ · $\overline{SB6}$ · C6 + ADF · RB6 · $\overline{SB6}$ · $\overline{C6}$ + ANF · RB6 · SB6 + CMFE · $\overline{RB6}$ + EOF · RB6 · $\overline{SB6}$ + EOF · $\overline{RB6}$ · SB6 + IOF · RB6 + IOF · SB6 + RL4 · RB3 + RL4 · SB3 + RLL · RB5 + RLL · SB5 + RSM6-9 · SRA6 + SLM · RB5 + SLM · SB6 + SRM · RB7 + SRM · SB7
TB7 (T Bus Bit 7)	A103-77 A104-17 A105-45	A104-17	= ADF · RB7 · SB7 · C7 + ADF · $\overline{RB7}$ · SB7 · $\overline{C7}$ + ADF · $\overline{RB7}$ · $\overline{SB7}$ · C7 + ADF · RB7 · $\overline{SB7}$ · $\overline{C7}$ + ANF · RB7 · SB7 + CMFE · $\overline{RB7}$ + EOF · RB7 · $\overline{SB7}$ + EOF · $\overline{RB7}$ · SB7 + IOF · RB7 + IOF · SB7 + RL4 · RB4 + RL4 · SB4 + RLL · RB6 + RLL · SB6 + RSM6-9 · SRA7 + SLM · RB6 + SLM · SB6 + SRM · RB8 + SRM · SB8

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

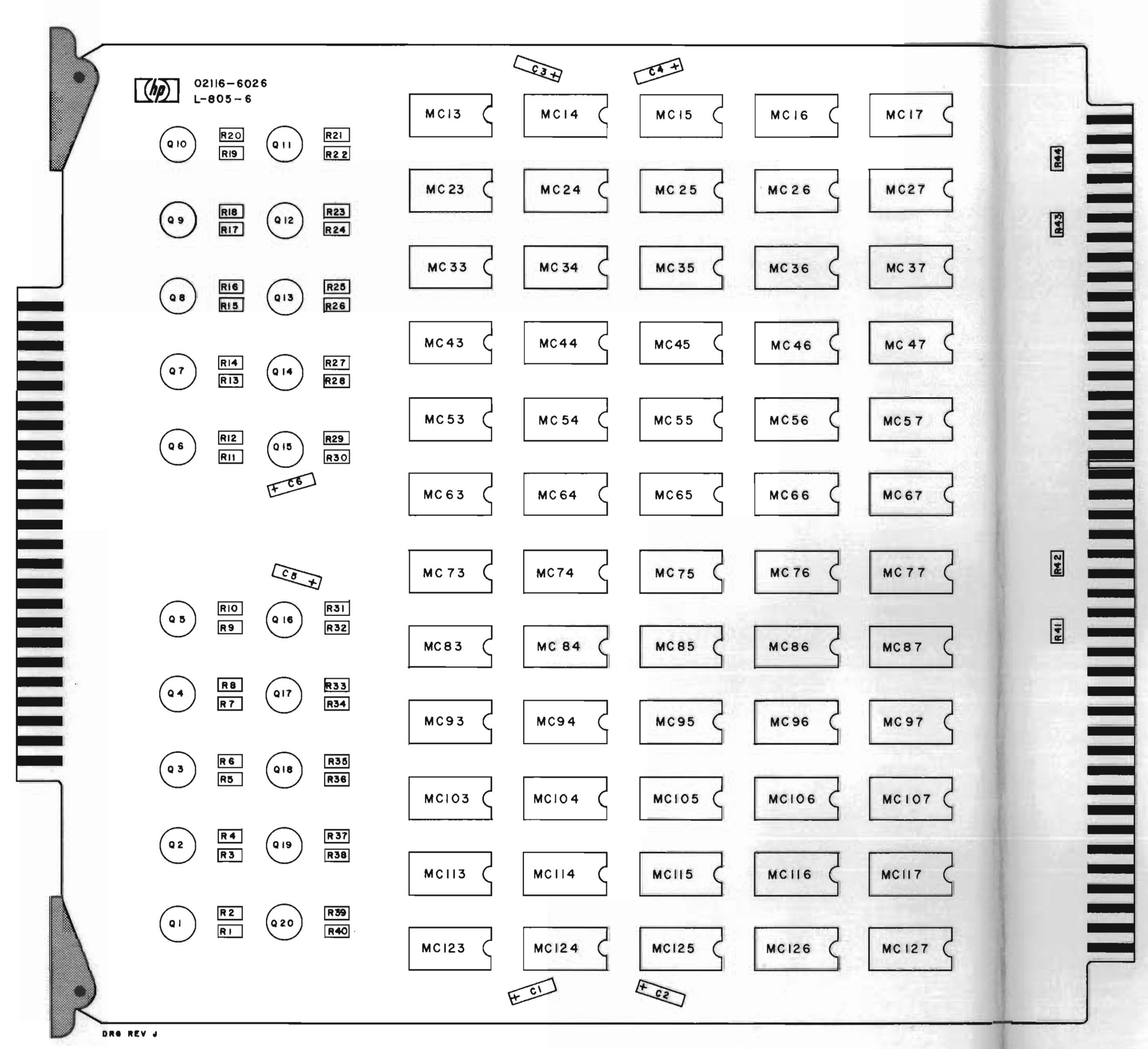
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
TB15 (T Bus Bit 15)	A102-17 A103-45 A105-77 A108-20 A110-80	A102-17 A108-20 A109-64 A110-80	= ADF · RB15 · SB15 · C15 + ADF · $\overline{RB15}$ · $\overline{SB15}$ · $\overline{C15}$ + ADF · $\overline{RB15}$ · $\overline{SB15}$; C15 + ADF · RB15 · $\overline{SB15}$ · $\overline{C15}$ + ANF · RB15 · SB15 + CMFE · $\overline{RB15}$ + EOF · RB15 · $\overline{SB15}$ + EOF · $\overline{RB15}$ · SB15 + IOF · RB15 + IOF · SB15 + RL4 · RB11 + RL4 · SB11 + RLL · RB14 + RLL · SB14 + RSM6-9 · SRA15 + SLM · RB14 + SLM · SB14 + SRG · T3 · $\overline{TR8}$ · $\overline{TR7}$ · RB15(B) + SRG · T5 ; $\overline{TR2}$ · $\overline{TR1}$; RB15(B) + SRG ; EFF · T3 · TR8 · $\overline{TR7}$ · TR6 + SRG · EFF · T5 · TR2 · $\overline{TR1}$ · TR0 + SRM · RB0 + SRM · SB0 + EAU option signal
TR0 (T-Register Bit 0)	A105-58	A5-3 A15-84 A108-12 A109-37	= TR0 FF, set-side output
$\overline{TR0}$ ("not" T-Register Bit 0)	A105-54	A7-5 A12-5 A15-82 A17-5 A22-5 A108-24 A202-82	= TR0 FF, clear-side output
TR0 FF (T-Register Bit 0 FF)			J = $\overline{TB0}$ K = TB0 Clock = STBT Direct Set = ST0 Direct Clear = RST
TR1 (T-Register Bit 1)	A105-9	A5-5 A15-83 A109-30 A202-84	= TR1 FF, set-side output
$\overline{TR1}$ ("not" T-Register Bit 1)	A105-10	A7-11 A12-11 A15-81 A17-11 A22-11 A108-27 A202-80	= TR1 FF, clear-side output
TR1 FF (T-Register Bit 1 FF)			J = $\overline{TB1}$ K = TB1 Clock = STBT Direct Set = ST1 Direct Clear = RST

Table 7-37. A105 Arithmetic Logic Card (Bits 3-0), Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TR2 (T-Register Bit 2)	A105-56	A5-7 A15-76 A107-71 A109-38	= TR2 FF, set-side output
$\overline{TR2}$ ("not" T-Register Bit 2)	A105-53	A7-13 A12-13 A15-74 A17-13 A22-13 A108-33 A202-66	= TR2 FF, clear-side output
TR2 FF (T-Register Bit 2 FF)			J = $\overline{TB2}$ K = $\overline{\overline{TB2}}$ Clock = STBT Direct Set = ST2 Direct Clear = RST
TR3 (T-Register Bit 3)	A105-16	A5-9 A15-75 A109-32 A202-60	= TR3 FF, set-side output
$\overline{TR3}$ ("not" T-Register Bit 3)	A105-15	A7-83 A12-83 A15-73 A17-83 A22-83 A108-10 A202-59	= TR3 FF, clear-side output
TR3 FF (T-Register Bit 3 FF)			J = $\overline{TB3}$ K = $\overline{\overline{TB3}}$ Clock = STBT Direct Set = ST3 Direct Clear = RST
TRD0 (T-Register Display Bit 0)	A105-21* A105-Y*	A501DS1	= TR0 FF, set-side output
TRD1 (T-Register Display Bit 1)	A105-22* A105-Z*	A501DS2	= TR1 FF, set-side output
TRD2 (T-Register Display Bit 2)	A105-20* A105-X*	A501DS3	= TR2 FF, set-side output
TRD3 (T-Register Display Bit 3)	A105-16* A105-T*	A501DS4	= TR3 FF, set-side output

Table 7-38. A102, A103, A104, A105 Arithmetic Logic Card (02116-6026), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	28480	0180-0155
MC13,14,23,24,33,43,44,53,54, 63,73,74,83,84,93,103,104, 113,114,123	1820-0967	Integrated Circuit, CTL	07263	SL3464
MC15,16,27,36,37,45,46,57,66, 67,75,76,87,96,97,105,106, 117,126,127	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC17,77,107	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC25,26,55,56,85,86,115,116	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC34,64,94,124	1820-0966	Integrated Circuit, CTL	07263	SL3463
MC35,65,95,125	1820-0971	Integrated Circuit, CTL	07263	SL3467
MC47	1820-0954	Integrated Circuit, CTL	07263	SL3457
Q1 thru Q20	1854-0246	Transistor, Si, NPN	07263	2N3643
R1,3,5,7,9,11,13,15,17,19,22, 24,26,28,30,32,34,36,38,40	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715
R2,4,6,8,10,12,14,16,18,20,21, 23,25,27,29,31,33,35,37,39	0683-6805	Resistor, Fxd, Comp, 68 ohms, 5%, 1/4W	01121	CB6805
R41 thru R44	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4W	01121	CB2215



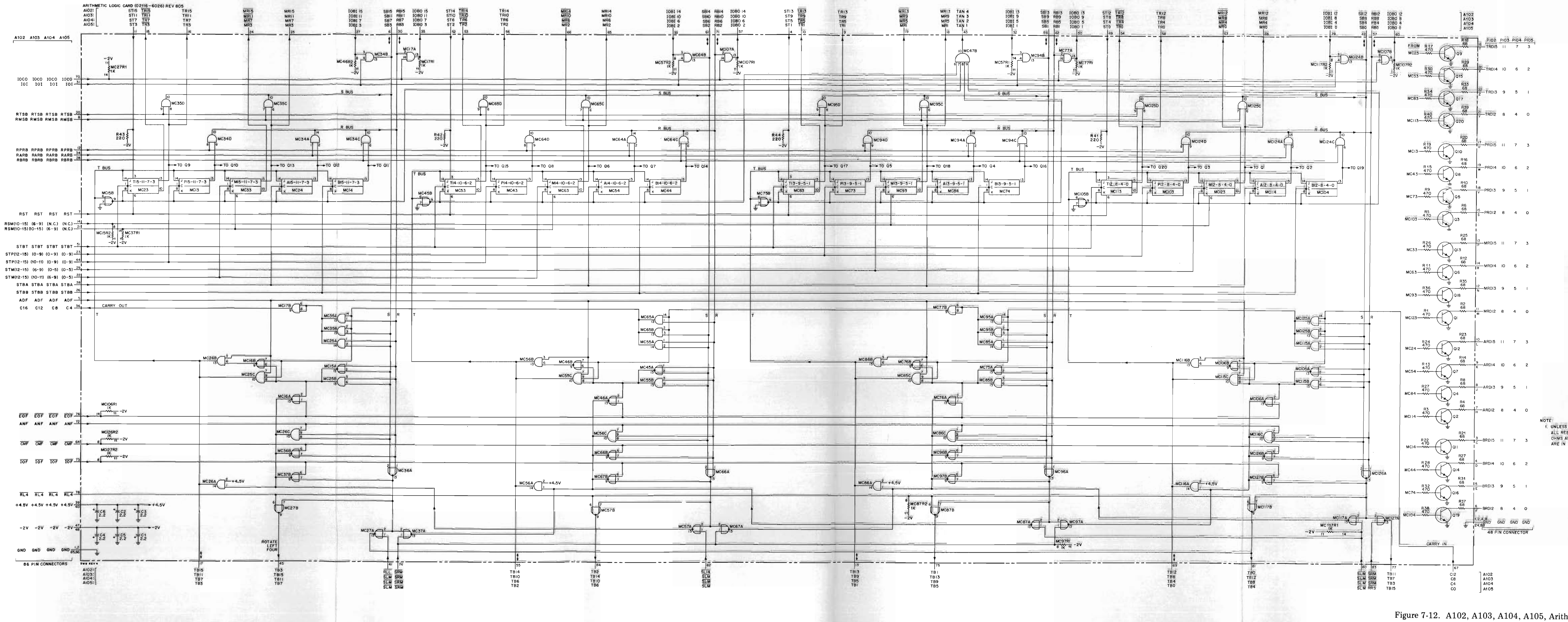


Figure 7-12. A102, A103, A104, A105, Arithmetic Logic Card (02116-6026), Parts Location and Schematic Diagram

Table 7-39. A106 Timing Generator Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A106-47 A106-48	None
+4.5V	A100E1	A106-39 A106-40	None
AAF (A-Addressable FF, set-side output)	A108-77	A106-75	See source
BAF (B-Addressable FF, set-side output)	A108-80	A106-83	See source
CF1 FF			J = +4.5V C = 10 MHz Oscillator Output K = +4.5V
CF2 FF			J = +4.5V C = CF1 FF K = +4.5V
DMS (Display Memory Switch Output, Gated)	A101-74	A106-59	See source
EIR (Enable Instruction Register)	A106-52	A107-4	= $\overline{IIR} \cdot (\overline{PH3} + \overline{DMS} \cdot \overline{LDS})$
EPH (Enable Phase)	A14-72	A106-14	See option
EXECUTE (Execute Indicator)	A106-5*	A501-5	= PH3 FF
EXT CLOCK (External Clock)	A106-3	None	= 10 MHz Oscillator Output
FETCH (Fetch Indicator)	A106-3*	A501-3	= PH1 FF, set-side output
GND (Ground), Card Input	A100E2	A106-1 A106-2 A106-85 A106-86	None
GND (Ground), Card Output	A106-1* A106-2* A106-A* A106-B*	A501-1 A501-2	None
HALT (Halt Indicator)	A106-8*	A501-8	= Run FF2, clear-side output
HALT FF			Set = HLS Clear = $\overline{HLS}$
HIN (Halt Instruction)	A15-69 A108-26	A106-66	See source or option
HLS (Halt Switch Output)	A101-54	A106-50	See source
$\overline{HLS}$ ("not" Halt Switch Output)	A101-50	A106-45	See source
IIR (Inhibit Instruction Register)	A109-77	A106-6	See option

Table 7-39. A106 Timing Generator Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
INDIRECT (Indirect Indicator)	A106-4*	A501-4	= PH2 FF, set-side output
INT (Interrupt)	A6-28 A15-79 A16-31 A202-3	A106-44	See source or option
$\overline{IR15}$ ("not" I-Register Bit 15)	A16-33 A107-42	A6-4 A106-49	See source or option
ISG (Inhibit Strobe Generator)	A4-3 A109-63	A106-4	See option
ISZ (Increment, Skip if Zero)	A107-76	A106-24	See source
JMP (Jump Instruction)	A107-79	A106-34	See source
JSB (Jump Subroutine Instruction)	A107-66	A106-82	See source
LADS (Load Address Switch Output, Gated)	A101-70	A106-68	See source
LAS (Load A Switch Output, Gated)	A101-62	A106-80	See source
LBS (Load B Switch Output, Gated)	A101-66	A106-65	See source
LMS (Load Memory Switch Output, Gated)	A101-58	A106-46	See source
MC62 (Output at "AND" gate MC62C-10)	A106	A106	= $\overline{PH3 \cdot ISZ}$ · T7T0 · T1T2 · T2T3 · T3T4 · T4T5 + T7T0 · T1T2 · T2T3 · T3T4 · T4T5 · T5T6
MIT (Memory Inhibit Time)	A106-25	A13-81	= MTE · $\overline{CF2}$ · $\overline{PH3 \cdot ISZ}$ · T4T5 + MTE · CF2 · $\overline{PH3 \cdot ISZ}$ · T3T4 + MTE · $\overline{PH3 \cdot ISZ}$ · T4 + MTE · $\overline{CF2}$ · PH3 · ISZ · $\overline{T2T3}$ · $\overline{T4T5}$ · T5T6 + MTE · CF2 · PH3 · ISZ ; $\overline{T0T1}$ · MC62 + MTE · PH3 · ISZ · $\overline{T0T1}$ · $\overline{T6T7}$ · MC62
MNS (Memory Normal Switch Output)	A101-22	A106-12	See source
MRT1 (Memory Read Time 1)	A106-29	A8-54 A8-57 A11-54 A11-57 A18-54 A18-57 A21-54 A21-57	= MTE · CF2 · T0 · DELAY · T0T1 · T1T2
MRT2 (Memory Read Time 2)	A106-26	A14-33	= MTE · T1T2
MSG (Memory Strobe Gate)	A106-19	A9-6 A10-6 A19-6 A20-6	= $\overline{MST}$; MRT1
MST (Memory Strobe Time)	A106-32	A13-83 A13-36	= MTE · $\overline{CF1}$ · $\overline{ISG}$ · $\overline{LMS}$ · $\overline{JSB}$ · $\overline{STRX}$ · $\overline{AAF}$ · $\overline{BAF}$ · $\overline{PH3}$ · T2

Table 7-39. A106 Timing Generator Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
MWL (Memory Write Level)	A106-33	A15-54 A16-34	= MTE · ISZ · PH3 + MTE · PH3 · STRX + MTE · PH3 · JSB + MTE · AAF + MTE · BAF + MTE · ISG + MTE · LMS
MWT1 (Memory Write Time 1)	A106-35	A8-50 A8-58 A11-50 A11-58 A18-50 A18-58 A21-50 A21-58	= MTE · CF2 · $\overline{\text{PH3 · ISZ}}$ · T3T4 · DLEAY + MTE · $\overline{\text{CF2}}$ · $\overline{\text{PH3 · ISZ}}$ · T4T5 + MTE · PH3 · ISZ · $\overline{\text{T0T1}}$ · MC62 + MTE · PH3 · ISZ · $\overline{\text{T2T3}}$ · $\overline{\text{T4T5}}$ · T5T6 · DELAY + MTE · PH3 · ISZ · $\overline{\text{T0T1}}$ · $\overline{\text{T6T7}}$ · MC62 · DELAY + MTE · $\overline{\text{PH3 · ISZ}}$ · T4 + MTE · PH3 · ISZ · $\overline{\text{T0T1}}$ · T6T7 · MC62
MWT2 (Memory Write Time 2)	A106-20	A14-27	= MTE · CF2 · $\overline{\text{PH3 · ISZ}}$ · T3T4 · DELAY + MTE · $\overline{\text{PH3 · ISZ}}$ · T4T5 + MTE · $\overline{\text{CF2}}$ · PH3 · ISZ · $\overline{\text{T2T3}}$ · $\overline{\text{T4T5}}$ · T5T6 · DELAY + MTE · $\overline{\text{CF2}}$ · PH3 · ISZ · $\overline{\text{T0T1}}$ · $\overline{\text{T6T7}}$ · MC62 · DELAY + MTE · PH3 · ISZ · $\overline{\text{T0T1}}$ · MC62
$\overline{\text{OPO}}$ ("not" One Phase Operation)	A107-16	A106-42	See source
P123 (Phase 1, Phase 2, or Phase 3)	A16-63 A106-23 A109-13	A14-68 A15-52 A16-63 A107-78	= PH1 + PH2 + PH3 + MP option signal + EAU option signal
$\overline{\text{P123}}$ ("not" Phase 1, Phase 2, or Phase 3)	A106-31	None	= $\overline{\text{PH1}}$ + $\overline{\text{PH2}}$ + $\overline{\text{PH3}}$
P123B (Phase 1, Phase 2, or Phase 3, Buffered)	A106-10	None	= P123
PARITY HALT (Parity Halt Indicator)	A106-6*	A501-6	= PEI
PEH (Parity Error Halt)	A15-62	A106-57	See option
PEI (Parity Error Indicator)	A15-61	A106-7	See option
PH1 FF (Phase 1 FF)			J = JMP · PH2 · $\overline{\text{SET}}$ · $\overline{\text{PH4}}$ · $\overline{\text{TR15}}$ + LPMS + PH3 · $\overline{\text{SET PH4}}$ + PH4 + PRS FF K = SET PH2 + SET PH3 + SET PH4 Clock = LNS · T7 · TS
PH1 (Phase 1, Fetch)	A106-41	A13-76 A16-21 A107-44 A109-81 A201-29	= EPH · RF2 · PH1 FF

Table 7-39. A106 Timing Generator Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
PH2 FF (Phase 2 FF)			J = PH1 · TR15 + $\overline{OPO}$ · PH1 · $\overline{SET\ PH4}$ · TR15 K = SET PH1 + SET PH3 + SET PH4 Clock = LNS · T7 · TS
PH2 (Phase 2, Indirect)	A106-37	A13-78 A16-49 A107-53	= EPH · RF2 · PH2 FF
PH3 FF (Phase 3 FF)			J = $\overline{JMP}$ · $\overline{OPO}$ · PH1 · $\overline{SET\ PH4}$ · $\overline{TR15}$ + $\overline{JMP}$ · PH2 · $\overline{SET\ PH4}$ · $\overline{TR15}$ + DMS · STEP 1 · $\overline{STEP\ 2}$ + LMS · STEP 1 · $\overline{STEP\ 2}$ K = SET PH1 + SET PH4 Clock = LNS · T7 · TS
PH3 (Phase 3, Execute)	A106-60	A1-67 A13-80 A107-60 A108-62	= EPH · RF2 · PH3 FF
PH4 FF (Phase 4 FF)			J = $\overline{JMP}$ · $\overline{JSB}$ · INT · RF1 + INT · RF1 · $\overline{IR15}$ K = SET PH1 Clock = LNS · T7 · TS
PH4 (Phase 4, Interrupt)	A106-13	A13-82 A107-83 A201-53	= EPH · RF2 · PH4 FF
PNS (Phase Normal Switch Output)	A101-18	A106-43	See source
POFP (Power On/Off Pulse)	A6-56	A106-77	See source
POPIO (Power On Pulse to I/O)	A106-61	A1-37 A15-45 A201-63	= POFP · T5
PRESET FF			Set = PRS Clear = $\overline{PRSW}$
PRS (Preset Switch Output, Gated)	A101-30	A106-78	See source
$\overline{PRSW}$ ("not" Preset Switch Output)	A101-34	A106-79	See source
$\overline{RF2}$ ("not" Run FF2)	A106-58	A6-62 A101-14 A109-54 A202-36	= Run FF2, reset-side output

Table 7-39. A106 Timing Generator Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
RNS (Run Switch FF, set-side output)	A101-44	A106-70	See source
RPB (Reset Parity Bit)	A106-27	A15-46	= P123B · T0 · TS
RPE (Reset Parity Error)	A106-74	None	= POFP
RUN (Run Indicator)	A106-7*	A501-7	= Run FF2, set-side output
RUN FF 1			J = RNS · STEP 1 FF · $\overline{\text{STEP 2 FF}}$ Clock = T1 K = HIN + PEH + LADS + PRS FF Direct Clear = HLS FF
RUN FF 2			J = STEP FF 1 · $\overline{\text{STEP FF 2}}$ Clock = T7S K = $\overline{\text{RUN FF 1}}$ Direct Clear = LADS + PRS FF
SCS (Single Cycle FF, set-side output)	A101-78	A106-56	See source
SEO (Switch Exclusive OR)	A106-72	A107-77 A108-22	= LAS + LMS + LPMS + SWSB
STEP 1 FF			L = RNS + SCS + DMS + LMS Clock = T2
STEP 2 FF			L = STEP 1 FF Clock = T1
STRX (Store Instruction, Excludable)	A13-42	A106-81	See source
SWSA (Switch Store in A-Register)	A106-84 A110-66	A107-35	= LAS · T2 + EAU option signal
SWSB (Switch Store in B-Register)	A106-71 A110-10	A107-24	= LBS · T2 + EAU option signal
SWSM (Switch Store in M-Register)	A106-73 A110-33	A107-26	= LPMS · T2 + EAU option signal
SWSP (Switch Store in P-Register)	A106-64	A107-37 A110-3	= LPMS · T2
SWST (Switch Store in T-Register)	A106-62	A4-83 A107-34 A110-20	= LMS · T2
T0 (Time Period 0)	A106-28	A1-54 A107-46 A108-68 A109-51 A110-15 A201-31	= T0T1 · T7T0
T0T1 (Time Periods 0 and 1)	A106-17	A107-80 A110-36	= T0T1 FF, set-side output
T0T1 FF (Time Periods 0 and 1 FF)			L = T7T0 Clock = CL1

Table 7-39. A106 Timing Generator Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
T1 (Time Period 1)	A106-53	A16-24 A107-62 A109-71 A110-13 A201-23	= T0T1 · T1T2
T1T2 (Time Periods 1 and 2)	A106-21	A107-52 A110-51	= T1T2 FF, set-side output
T1T2 FF (Time Periods 1 and 2 FF)			L = T0T1 Clock = CL2
T2 (Time Period 2)	A106-76	A107-59 A108-35 A109-43 A110-22 A201-83	= T1T2 · T2T3
T2T3 FF (Time Periods 2 and 3 FF)			L = T1T2 Clock = CL1
T3 (Time Period 3)	A106-63	A15-23 A16-23 A107-43 A108-45 A109-75 A110-32 A201-3	= T2T3 · T3T4
T3T4 (Time Periods 3 and 4)	A106-15	A4-30 A107-70 A108-7 A110-74	= T3T4 FF, set-side output
T3T4 FF (Time Periods 3 and 4 FF)			L = T2T3 Clock = CL2
T4 (Time Period 4)	A106-54	A107-31 A108-65 A109-55 A110-24	= T3T4 · T4T5
T4T5 (Time Periods 4 and 5)	A106-16	A3-31 A4-6 A107-54 A108-21 A110-23	= T4T5 FF, set-side output
T4T5 FF (Time Periods 4 and 5 FF)			L = T3T4 Clock = CL1
T5 (Time Period 5)	A106-69	A107-36 A108 46 A109-67 A110-54 A201-45	= T4T5 · T5T6
T5T6 FF (Time Periods 5 and 6 FF)			L = T4T5 Clock = CL2

Table 7-39. A106 Timing Generator Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
T6 (Time Period 6)	A106-11	A109-60 A110-30	= T5T6 · T6T7
T6T7 (Time Periods 6 and 7)	A106-30	A3-73 A107-69 A108-72 A109-14 A110-11	= T6T7 FF, set-side output
T6T7 FF (Time Periods 6 and 7 FF)			L = T5T6 Clock = CL1
T7 (Time Period 7)	A106-18	A1-57 A4-64 A15-26 A16-61 A107-32 A108-83 A109-73 A110-28	= T6T7 · T7T0
T7T0 FF (Time Periods 7 and 0 FF)			L = T6T7 Clock = CL2
T7S (Time Period 7 with Strobe)	A106-51	A4-10 A109-23	= T7 · TS
TR15 (T-Register Bit 15)	A102-16	A106-38	See source
$\overline{\text{TR15}}$ ("not" T-Register Bit 15)	A102-15	A106-36	See source
TS (Time Strobe)	A106-55	A107-45 A108-74 A201-27	= $\overline{\text{CF1}}$ · Delay
TSA (Time Strobe A)	A106-67	A1-59 A2-59 A3-45 A15-17 A16-27 A109-76 A110-29	= $\overline{\text{CF1}}$ · Delay

Table 7-40. A106 Timing Generator Card (02116-63220), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,3	0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192
C2	0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80-20%, 100 VDCW	28480	0160-2055
C4	0160-2588	Capacitor, Fxd, Cer, 1000 pF, 5%, 50 VDCW	28480	0160-2588
C5	0160-0363	Capacitor, Fxd, Mica, 620 pF, 5%	28480	0160-0363
C6	0140-0197	Capacitor, Fxd, Mica, 180 pF, 5%, 300 VDCW	04062	RDM15F181J3C
C7 thru C10	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	56289	150D225X0020A2-CYS
C11	0140-0225	Capacitor, Fxd, Mica, 300 pF, 1%	28480	0140-0225
C12	0160-2940	Capacitor, Fxd, Mica, 470 pF, 5%, 300 VDCW	72136	RDM15F471J3C
CR1	1910-0022	Diode, Ge, 5 WIV	14433	G401
L1	9140-0107	Coil, Fxd, RF, 27 MH, 10%	99800	1840-38
Q1 thru Q3	1854-0005	Transistor, Si, NPN	80131	2N708
Q4 thru Q9	1854-0246	Transistor, Si, NPN	80131	2N3643
R1	0683-3935	Resistor, Fxd, Comp, 39k, 5%, 1/4W	01121	CB3935
R2	0683-8215	Resistor, Fxd, Comp, 820 ohms, 5%, 1/4W	01121	CB8215
R3	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4W	01121	CB5115
R4	0683-4705	Resistor, Fxd, Comp, 47 ohms, 5%, 1/4W	01121	CB4705
R5	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R6,8,10,12,14,16	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715
R7,9,11,13,15,17	0683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4W	01121	CB3305
R18,19	0683-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/4W	01121	CB1515
R20 thru R22,24,25	0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4W	01121	CB1015
R23	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4W	01121	CB2215
MC12,23,45,46,52,55,64,65,87,97, 115,124,127	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC13,15,17,37,42,57,67,73,75,76, 83,93,103,113,114,123	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC14,24,34,44,72,74,82,84	1820-0967	Integrated Circuit, CTL	07263	SL3464
MC16,22,26,27,32,35,36,43,53,62, 76,77,104,107,117,126	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC26,54,56,85,86,95,96,105, 106,125	1820-0965	Integrated Circuit, CTL	07263	SL3462
MC47,63	1820-0954	Integrated Circuit, CTL	07263	SL3457
MC66	1820-0966	Integrated Circuit, CTL	07263	SL3463
MC92,94,102,112,122	1820-0968	Integrated Circuit, CTL	07263	SL3466
MC116	1820-0971	Integrated Circuit, CTL	07263	SL3467
XY1	1200-0199	Socket, Crystal	91506	8000-AG9
Y1	0410-0035	Crystal, Quartz, 10 mc/s, 0.005%	28480	0410-0035

Table 7-41. A107 Instruction Decoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOG (Input/Output Instruction Group)	A107-6	A6-38 A15-59 A16-16	= EIR · PH1 · IR15 · $\overline{IR14}$ · $\overline{IR13}$ · $\overline{IR12}$ · IR10
IR10 FF (I-Register Bit 10 FF)			J = TR10 Clock = PH1 · T2 · TS Direct Clear = PH1 · T1
IR11 FF (I-Register Bit 11 FF)			J = TR11 Clock = PH1 · T2 · TS Direct Clear = PH1 · T1
IR12 FF (I-Register Bit 12 FF)			J = TR12 Clock = PH1 · T2 · TS Direct Clear = PH1 · T1
IR13 FF (I-Register Bit 13 FF)			J = TR13 Clock = PH1 · T2 · T5 Direct Clear = PH1 · T1
IR14 FF (I-Register Bit 14 FF)			J = TR14 Clock = PH1 · T2 · TS Direct Clear = PH1 · T1
IR15 FF (I-Register Bit 15 FF)			J = TR15 Clock = PH1 · T2 · TS Direct Clear = PH1 · T1
$\overline{IR15}$ ("not" Instruction Register, Bit 15)	A107-42 A16-33	A6-4 A106-49	= IR15 FF, clear-side output
ISZ (Increment, Skip if Zero)	A107-76	A1-69 A15-44 A106-24 A108-61	= EIR · $\overline{IR14}$ · IR13 · IR12 · IR11
JMP (Jump Instruction)	A107-79	A16-11 A106-34	= EIR · $\overline{IR14}$ · IR13 · $\overline{IR12}$ · IR11
JSB (Jump Subroutine Instruction)	A107-66	A106-82	= EIR · $\overline{IR14}$ · $\overline{IR13}$ · IR11 · IR11
MAC (Macro Group Decoded)	A107-5	A109-62	= EIR · PH1 · IR15 · $\overline{IR14}$ · $\overline{IR13}$ · $\overline{IR12}$ · $\overline{IR10}$
$\overline{OPO}$ ("not" One Phase Operation)	A107-16	A106-42	= $\overline{EIR}$ + $\overline{PH1}$ + IR14 + IR13 + IR12
P123 (PH1, PH2 or PH3)	A106-23 A109-13	A107-78	See source or option
PH1 (Phase 1, Fetch)	A106-41	A107-44	See source
PH2 (Phase 2, Indirect)	A106-37	A107-53	See source
PH3 (Phase 3, Execute)	A106-60	A107-60	See source
PH4 (Phase 4, Interrupt)	A106-13	A107-83	See source

Table 7-41. A107 Instruction Decoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
RARB (Read A-Register to the R-Bus)	A107-19 A110-65	A102-34 A103-34 A104-34 A105-34	= AAF · $\overline{JSB}$ · P123 ; T1 + AAF · $\overline{PH3}$ · P123 · T1 + ADD · PH3 ; T3T4 + ASG · T3 · $\overline{TR8}$ + ASG · T4T5 + CPR · PH3 · T3T4 + EIR · PH3 · T3T4 · $\overline{IR14}$ · $\overline{IR11}$ + IOG · T3 · $\overline{TR6}$ + IOG · T4T5 · $\overline{TR6}$ + SRG · T3 + SRG · T4T5 + STR · PH3 · T2 + EAU option signal
RB0 (R-Bus Bit 0)	A107-61 A110-43	A106-37 A108-52	= ISZ · PH3 · T3T4 + RARB · AR0 FF + RBRB · BR0 FF + RPRB · PR0 FF + EAU option signal
RBRB (Read B-Register to the R-Bus)	A107-18 A110-58	A102-28 A103-28 A104-28 A105-28	= ADD · PH3 · T3T4 + ASG · T3 · $\overline{TR8}$ + ASG · T4T5 + BAF · $\overline{JSB}$ · P123 · T1 + BAF · $\overline{PH3}$ · P123 · T1 + CPR · PH3 · T3T4 + EIR ; PH3 · T3T4 · $\overline{IR14}$ · $\overline{IR11}$ + IOG ; T3 · $\overline{TR6}$ + IOG · T4T5 · $\overline{TR6}$ + SRG · T3 + SRG · T4T5 + STR · PH3 · T2 + EAU option signal
RMSB (Read M-Register to the S-Bus)	A107-68 A110-34	A102-8 A103-8 A104-8 A105-8	= JSB · PH3 · T3T4 + P123 · T0 + EAU option signal
RPRB (Read P-Register to the R Bus)	A107-72 A110-4	A102-12 A103-12 A104-12 A105-12	= JSB · PH3 · T1T2 + OPO · T6T7 + PH3 · T6T7 + PH4 · T1T2 + PH4 · T3T4 + PH4 · T5 + EAU option signal
RSM 6-9 (Reset M-Register Bits 6 thru 9)	A107-12	A103-14 A104-21 A202-11	= PH4 · T7
RSM 10-15 (Reset M-Register Bits 10 thru 15)	A107-11	A102-14 A102-21 A103-21	= OPO · PH1 · TS · IR10
RST (Reset T-Register)	A107-58	A102-7 A103-7 A104-7 A105-7	= P123 · T0 · TS

Table 7-41. A107 Instruction Decoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
RTSB (Read T-Register to the S-Bus)	A107-82 A110-19	A1-60 A102-20 A103-20 A104-20 A105-20	= $\overline{CPR}$ · PH3 · T5 · IR12 + EIR · $\overline{JSB}$ · PH3 · T3T4 + OPO · PH1 · T6T7 + PH2 · T6T7 + EAU option signal
SBO (S Bus Bit 0)	A107-81 A110-44 A105-42	A105-42	= ASG · T4T5 · $\overline{T6T7}$ · TR2 + ASG · $\overline{TLS}$ · T4T5 · TR2 + JSB · PH3 · T1T2 · $\overline{T6T7}$ + JSB · $\overline{TLS}$ · PH3 · T1T2 + PH4 · T3T4 · $\overline{T6T7}$ + PH4 · $\overline{TLS}$ · T3T4 + IOI · IOBI 0 + RMSB · MR0 + RTSB · TR0 + EAU option signal
SEO (Switch Exclusive OR)	A106-72	A107-77	See source
SRG (Shift-Rotate Group Decoded)	A107-38	A108-49	= EIR · PH1 · $\overline{IR15}$ · $\overline{IR14}$ · $\overline{IR13}$ · $\overline{IR12}$ · $\overline{IR10}$
STBA (Store T-Bus in A-Register)	A107-50	A102-38 A103-38 A104-38 A105-38	= SWSA · TS + EIR · PH3 · T4 · TS · IR14 · $\overline{IR12}$ · $\overline{IR11}$ + EIR · PH3 · T4 · TS · $\overline{IR14}$ · $\overline{IR11}$ + CPR · AAF · PH3 · T5 · TS · IR12 + ASG · T3 · TS · $\overline{IR11}$ + ASG · T5 · TS · TR2 + SRG · T3 · TS · TR9 · $\overline{IR11}$ + SRG · T5 · TS · TR4 · $\overline{IR11}$ + IOG · TS · TR8 · TR7 · $\overline{IR11}$
STBB (Store T-Bus in B-Register)	A107-51	A102-26 A103-26 A104-26 A105-26	= SWSB · TS + EIR · PH3 · T4 · TS · IR14 · $\overline{IR12}$ · IR11 + CPR · BAF · PH3 · T5 · TS · IR12 + ASG · T3 · TS · IR11 + ASG · T5 · TS · IR11 + SRG · T3 · TS · TR9 · IR11 + SRG · T5 · TS · TR4 · IR11 + IOG · TS · TR8 · TR7 · IR11
STBT (Store T-Bus in T-Register)	A107-63	A102-51 A103-51 A104-51 A105-51	= SWST · TS + AAF · P123 · T1 · TS + BAF · P123 · T1 · TS + ISZ · PH3 · T4 · TS + JSB · PH3 · T2 · TS + STR · PH3 · T2 · TS
STM 0-5 (Store T-Bus Bits 0 thru 5 in M-Register)	A107-20	A104-29 A105-22 A105-29	= SWSM · TS + EIR · $\overline{OPO}$ · PH1 · T7 · TS + OPO · T7 · TS + PH2 · T7 · TS + PH3 · T7 · TS + PH4 · T7 · TS
STM 6-9 (Store T-Bus Bits 6 thru 9 in M-Register)	A107-21	A103-29 A104-22	= SWSM · TS + EIR · $\overline{OPO}$ · PH1 · T7 · TS + OPO · T7 · TS + PH2 · T7 · TS + PH3 · T7 · TS

Table 7-41. A107 Instruction Decoder Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
STM 10-11 (Store T-Bus Bits 10 thru 11 in M-Register)	A107-27	A103-22	= SWSM · TS + OPO · T7 · TS + PH2 · T7 · TS + PH3 · T7 · TS
STM 12-15 (Store T-Bus Bits 12 thru 15 in M-Register)	A107-28	A102-22 A102-29 A201-79	= SWSM · TS + OPO · T7 · TS + PH2 · T7 · TS + PH3 · T7 · TS
STP 0-9 (Store T-Bus Bits 0 thru 9 in P-Register)	A107-7	A103-23 A104-23 A104-44 A105-23 A105-44	= SWSP · TS + JMP · PH1 · T5 · TS · $\overline{IR10}$ + JMP · PH1 · T7 · TS · $\overline{TR15}$ + JMP · PH2 · T7 · TS · $\overline{TR15}$ + JSB · PH3 · T4 · TS + OPO · T7 · TS + PH3 · T7 · TS + PH4 · T2 · TS + PH4 · T4T5 · TS
STP 10-11 (Store T-Bus Bits 10 thru 11 in P-Register)	A107-74	A103-44	= SWSP · TS + JMP · PH1 · T5 · TS · $\overline{IR10}$ + JMP · PH2 · T7 · TS · $\overline{TR15}$ + JSB · PH3 · T4 · TS + OPO · T7 · TS + PH3 · T7 · TS + PH4 · T2 · TS + PH4 · T4T5 · TS
STP 12-15 (Store T-Bus Bits 12 thru 15 in P-Register)	A107-8	A102-23 A102-44	= SWSP · TS + JMP · PH1 · T5 · TS · $\overline{IR10}$ + JMP · PH2 · T7 · TS · $\overline{TR15}$ + JSB · PH3 · T4 · TS + OPO · T7 · TS + PH3 · T7 · TS + PH4 · T2 · TS + PH4 · T4T5 · TS
STR (Store Instruction)	A107-64	A13-46	= EIR · IR14 · IR13 · IR12
SWSA (Switch Store in A-Register)	A106-84 A110-66	A107-35	See source or option
SWSB (Switch Store in B-Register)	A106-71 A110-10	A107-24	See source or option
SWSM (Switch Store in M-Register)	A106-73 A110-33	A107-26	See source or option
SWSP (Switch Store in P-Register)	A106-64	A107-37	See source
SWST (Switch Store in T-Register)	A106-62 A4-83	A107-34	See source or option
T0 (Time Period 0)	A106-28	A107-46	See source
T0T1 (Time Periods 0 and 1)	A106-17	A107-80	See source
T1 (Time Period 1)	A106-53	A107-62	See source
T1T2 (Time Periods 1 and 2)	A106-21	A107-52	See source

Table 7-41. A107 Instruction Decoder Card, Signal List (Continued)

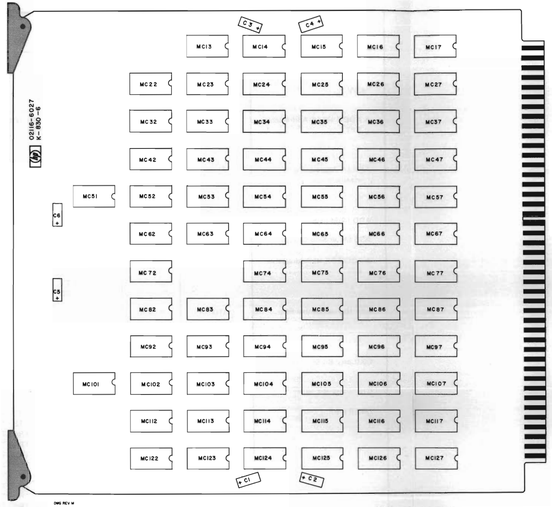
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
T2 (Time Period 2)	A106-76	A107-59	See source
T3 (Time Period 3)	A106-63	A107-43	See source
T3T4 (Time Periods 3 and 4)	A106-15	A107-70	See source
T4 (Time Period 4)	A106-54	A107-31	See source
T4T5 (Time Periods 4 and 5)	A106-16	A107-54	See source
T5 (Time Period 5)	A106-69	A107-36	See source
T6T7 (Time Periods 6 and 7)	A106-30	A107-69	See source
T7 (Time Period 7)	A106-18	A107-32	See source
TR2 (T-Register Bit 2)	A105-56	A107-71	See source
TR4 (T-Register Bit 4)	A104-58	A107-25	See source
$\overline{TR6}$ ("not" T-Register Bit 6)	A104-53	A107-55	See source
$\overline{TR7}$ ("not" T-Register Bit 7)	A104-15	A107-23	See source
TR8 (T-Register Bit 8)	A103-58	A107-29	See source
$\overline{TR9}$ ("not" T-Register Bit 9)	A103-10	A107-57	See source
TR10 (T-Register Bit 10)	A103-56	A107-9	See source
TR11 (T-Register Bit 11)	A103-16	A107-14	See source
TR12 (T-Register Bit 12)	A102-58	A107-17	See source
TR13 (T-Register Bit 13)	A102-9	A107-30	See source
TR14 (T-Register Bit 14)	A102-56	A107-33	See source
TR15 (T-Register Bit 15)	A102-16	A107-41	See source
TS (Time Strobe)	A106-55	A107-45	See source

Table 7-42. A107 Instruction Decoder Card (02116-6027), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	56289	150D225X0020A2
MC13,16,23,26,33,36,46,51,54, 56,66,77,87,92,97,107,114, 123	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC14,22,24,25,43,45,49,52,64, 74,84	1820-0954	Integrated Circuit, CTL	07263	SL3457
MC15,53,62,75,83,85,94,101,102, 106,113,125,127	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC17,27,37,47,57,67	1820-0967	Integrated Circuit, CTL	07263	SL3464
MC32,35,72,76,86,93,95,103,104, 105,122,124,126	1820-0971	Integrated Circuit, CTL	07263	SL3467
MC34,55,63,116,117	1820-0965	Integrated Circuit, CTL	07263	SL3462
MC42,65,82,96,112,115	1820-0952	Integrated Circuit, CTL	07263	SL3455

Table 7-43. A108 Shift Logic Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A108-47 A108-48	None
+4.5V	A100E1	A108-39 A108-40	None
A ADDR FF (A-Addressable FF)			J = P123G · T0 · TAN1 · TAN2 · TAN3 · $\overline{TB14}$ · $\overline{TB13}$ · $\overline{TB12}$ K = T7 Clock = TS
AAF (A Addressable FF, set-side output)	A108-77	A15-49 A16-17 A106-75 A107-49	= AA FF, set-side output
ADD (Add Instruction)	A107-3	A108-29	See source
ASG (Alter-Skip Group)	A107-10	A108-82	See source
B ADDR FF (B-Addressable FF)			J = P123G · T0 · TAN2 · TAN3 · $\overline{TB14}$ · $\overline{TB13}$ · $\overline{TB12}$ · $\overline{TB3}$ · $\overline{TB2}$ · $\overline{TB1}$ · TB0 K = T7 Clock = TS
BAF (B Addressable FF, set-side output)	A108-80	A15-50 A16-13 A106-83 A107-13	= BA FF, set-side output
C0 (Carry Bit 0)	A108-71	A1-43 A105-67	= Carry FF ; T6T7
C16 (Carry Bit 16)	A102-36	A108-64	See source
CARRY FF			J = ASG · EFF · T3 · TR6 · TR0(B) + ASG · $\overline{EFF}$ · T3 · TR5 · TR0 + ASG · T4 · TR4 · $\overline{TR0}$ · RB15 + ASG · T4 · TR4 · $\overline{TR3}$ · TR0(B) + ASG · T4 · TR4 · TR0(B) ; RB15 + ASG · T4 · $\overline{TR4}$ · TR0(B) · RB0 + ASG · T4 · $\overline{TR4}$ · TR3 · TR0(B) + ASG · T4 · TR3 · TR0(B)· RB15 + ASG · T4 · TR3 · TR0(B) · RB0 + ASG · T4 · TR3 · $\overline{TR0}$ · $\overline{RB0}$ + ASG · T5 · TR1 · ($\overline{TAN4}$ + $\overline{TAN3}$ + $\overline{TAN2}$ + $\overline{TAN1}$) + ASG · T5 · $\overline{TR4}$ · $\overline{TR3}$ · $\overline{TR1}$ · ($\overline{TAN4}$ · $\overline{TAN3}$ · $\overline{TAN2}$ · $\overline{TAN1}$) + ASG · T5 · TR1 · $\overline{TR0}$ · TAN4 · TAN3 · TAN2 · TAN1 + CPR · PH3 · T4 · ($\overline{TAN4}$ + $\overline{TAN3}$ + $\overline{TAN2}$ + $\overline{TAN1}$) + ISZ · PH3 · T4 · C16 + SKF · T4 + SRG · T4 · TR3 · $\overline{RB0}$ K = T0 Clock = TS
CLC (Clear Control)	A108-53 A4-60	A1-18 A2-18 A6-21 A201-75 A203-21 thru A220-21	= IOG · T4 · TR11 · TR8 · TR7 · TR6 + DMA option signal



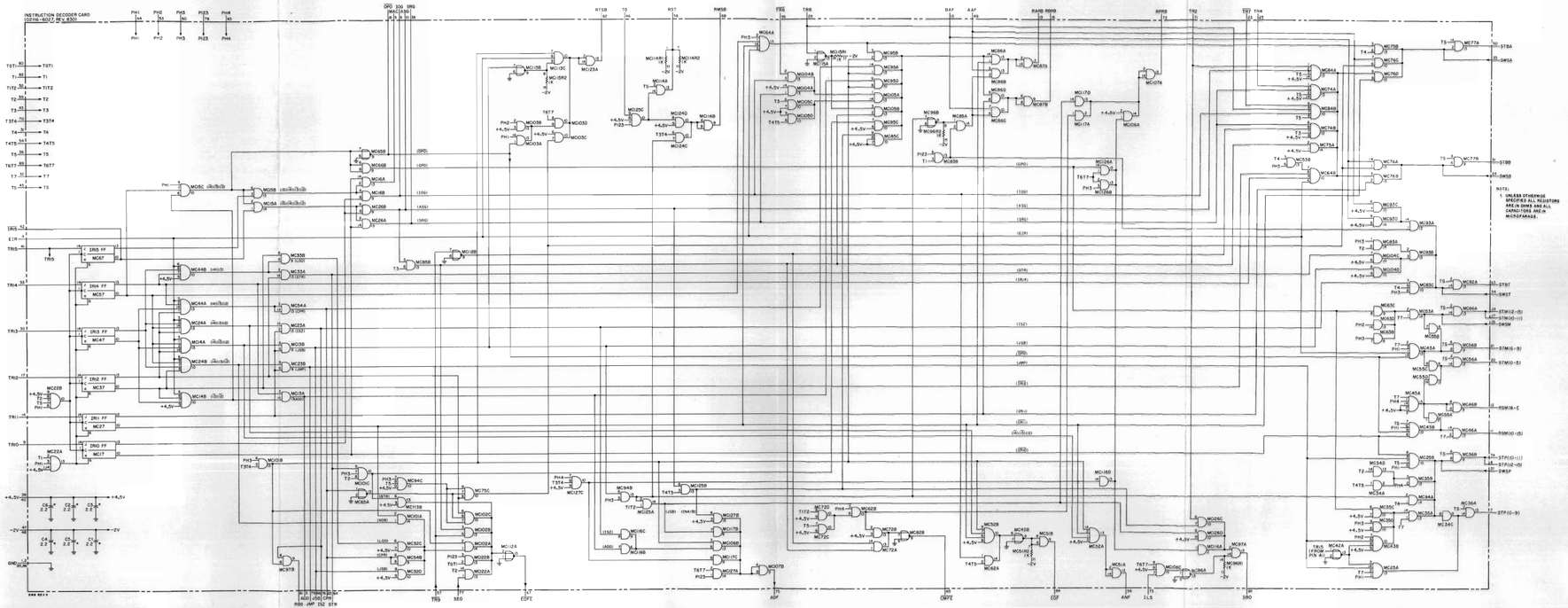


Figure 7-14. A107 Instruction Decoder Card (02116-6027), Parts Location and Schematic Diagram

Table 7-43. A108 Shift Logic Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
CLF (Clear Flag)	A108-19 A4-14	A1-51 A6-7 A15-51 A109-24 A201-51 A203-7 thru A220-7	= IOG · T4 · TR9 + DMA option signal
CPR (Compare Instruction)	A107-22	A108-63	See source
EXTEND FF			J = ADD · PH3 · T4 · C16 + ASG · T3 · TR7 + ASG · T5 · TR2(B) · C16 + SRG · T3 · TR8 · TR7 · $\overline{TR6}$ · RB15(B) + SRG · T3 · TR8 · $\overline{TR7}$ · TR6 · RB0(B) + SRG · T5 · TR2 · TR1 · $\overline{TR0}$ · RB15(B) + SRG · T5 · TR2 · $\overline{TR1}$ · TR0 · RB0(B) K = ASG · T3 · TR7 · $\overline{TR6}$ + ASG · T+ · TR7 · TR6 + SRG · T3 · TR8 · TR7 · $\overline{TR6}$ · $\overline{RB15}$ + SRG · T3 · TR8 · $\overline{TR7}$ · TR6 · RB0 + SRG · T4 · TR5 + SRG · T5 · TR2 · TR1 · $\overline{TR0}$ · $\overline{RB15}$ + SRG · T5 · TR2 · $\overline{TR1}$ · TR0 · $\overline{RB0}$ Clock = TS
EXTEND IND (Extend Indicator)	A108-37	A101-83	= EXTEND FF
GND (Ground)	A100E2	A108-1 A108-2 A108-85 A108-86	None
HIN (Halt Instruction)	A108-26 A15-69	A106-66 A16-55	= IOG · $\overline{TR8}$ · $\overline{TR7}$ · $\overline{TR6}$ + PE option signal + MP option signal
IOCO (Input/Output Control, Output)	A108-34	A102-70 A103-70 A104-70 A105-70	= IOG · T4T5 · TR8 · TR7 · $\overline{TR6}$
IOGE (Input/Output Instruction Group, Buffered)	A6-59	A108-16	See source or option
IOI (Input/Output, Input)	A108-44 A4-81 A4-84	A1-22 A2-22 A3-11 A3-43 A15-15 A16-59 A102-31 A103-31 A104-31 A105-31 A202-24 thru A220-24	= IOG · T4T5 · TR8 · $\overline{TR7}$ + SEO · T2 + DMA option

Table 7-43. A108 Shift Logic Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOO (Input/Output, Output)	A108-13 A4-56	A1-8 A2-8 A3-30 A16-57 A203-20 thru A220-20	= IOG · T3T4 · TR8 · TR7 · $\overline{TR6}$ + SRG · T3 · TR8 · TR7 · $\overline{TR6}$ + DMA option signal
IOS (Input/Output Switch Address)	A201-6 A109-29	A108-81	See source or option
ISR (Input Switch Register)	A108-84	A101-6	= IOG · IOS · TR8 · $\overline{TR7}$ + SEO
ISZ (Increment, Skip if Zero)	A107-76	A108-61	See source
OVERFLOW FF			J = ADD ; PH3 ; T4 · $\overline{TB15}$ · RB15 · SB15 + ADD · PH3 · T4 · $\overline{TB15}$ · RB15 · SB15 + ASG · T5 · TR2(B) · TB15 · RB15 · SB15 + ASG · T5 · TR2(B) · $\overline{TB15}$ · RB15 · SB15 + IOS · STF K = IOS · CLF Clock = TS
OVERFLOW IND (Overflow Indicator)	A108-9	A101-4	= OVERFLOW FF
P123G (Phase 1, Phase 2, or Phase 3, with "not" Phase 5)	A14-65	A108-69	See source
PH3 (Phase 3, Execute)	A106-60	A108-62	See source
RB0 (R bus, Bit 0)	A107-61 A110-43	A108-52	See source
RB15 (R bus, Bit 15)	A102-30	A108-66	See source
$\overline{RL4}$ ("not" Rotate Left 4 Bits)	A108-28	A102-78 A103-78 A104-78 A105-78	= SRG · T3 · TR8 TR7 · TR6 + SRG · T5 · TR2 · TR1 · TR0(B)
$\overline{RLL}$ ("not" Rotate Left to Least Significant Bit)	A108-42	A102-41	= SRG ; T3 · $\overline{TR8}$; TR7 · TR6 = SRG ; T5 · $\overline{TR2}$ · TR1 · TR0(B)
$\overline{RRS}$ ("not" Rotate Right to Sign Bit)	A108-41	A105-83	= SRG · T3 · $\overline{TR8}$ · TR7 · TR6 + SRG · T5 · $\overline{TR2}$ · TR1 · TR0
SB15 (S bus, Bit 15)	A102-6	A108-50	See source
SEO (Switch Exclusive OR)	A106-72	A108-22	See source

Table 7-43. A108 Shift Logic Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
SFC (Skip if Flag Clear)	A108-14	A4-24 A6-5 A201-71 A203-5 thru A220-5	= IOG · $\overline{TR8}$ · TR7 · $\overline{TR6}$
SFS (Skip if Flag Set)	A108-54	A1-31 A4-20 A201-68 A203-25 thru A220-25	= IOG · $\overline{TR8}$ · TR7 · TR6
SKF (Skip on Flag Signal)	A201-73 A203-12 thru A220-12 A4-29	A108-31	See source or option
$\overline{SL14E}$ ("not" Shift Left, Bit 14)	A108-38	A14-67	= SRG · T3 · $\overline{TR6}$ + SRG · T5 · $\overline{TR0}$
$\overline{SLME}$ ("not" Shift Left Magnitude)	A108-8	A14-70	= SRG · T3 · $\overline{TR6}$ + SRG · T5 · $\overline{TR0}$
SRG (Shift Rotate Group)	A107-38	A108-49	See source
$\overline{SRME}$ ("not" Shift Right Magnitude)	A108-32	A14-76	= SRG · T3 · $\overline{TR7}$ · TR6 + SRG · T3 · $\overline{TR8}$ · TR6 + SRG · T5 · $\overline{TR1}$; TR2 + SRG · T5 · $\overline{TR2}$; TR0
STC (Set Control)	A108-56 A4-58	A1-20 A2-20 A3-17 A6-22 A16-41 A201-61 A203-22 thru A219-22	= IOG · T4 · $\overline{TR11}$ · TR8 · TR7 · TR6 + DMA option signal
STF (Set Flag)	A108-5	A4-16 A15-18 A109-15 A201-41 A203-9 thru A220-9	= IOG · T3 · $\overline{TR8}$ · $\overline{TR7}$ · TR6 + SRG · T3 · $\overline{TR8}$ · $\overline{TR7}$ · TR6
T0 (Time Period 0)	A106-28	A108-68	See source
T2 (Time Period 2)	A106-76	A108-35	See source
T3 (Time Period 3)	A106-63	A108-45	See source
T3T4 (Time Periods 3 and 4)	A106-15	A108-7	See source
T4 (Time Period 4)	A106-54	A108-65	See source

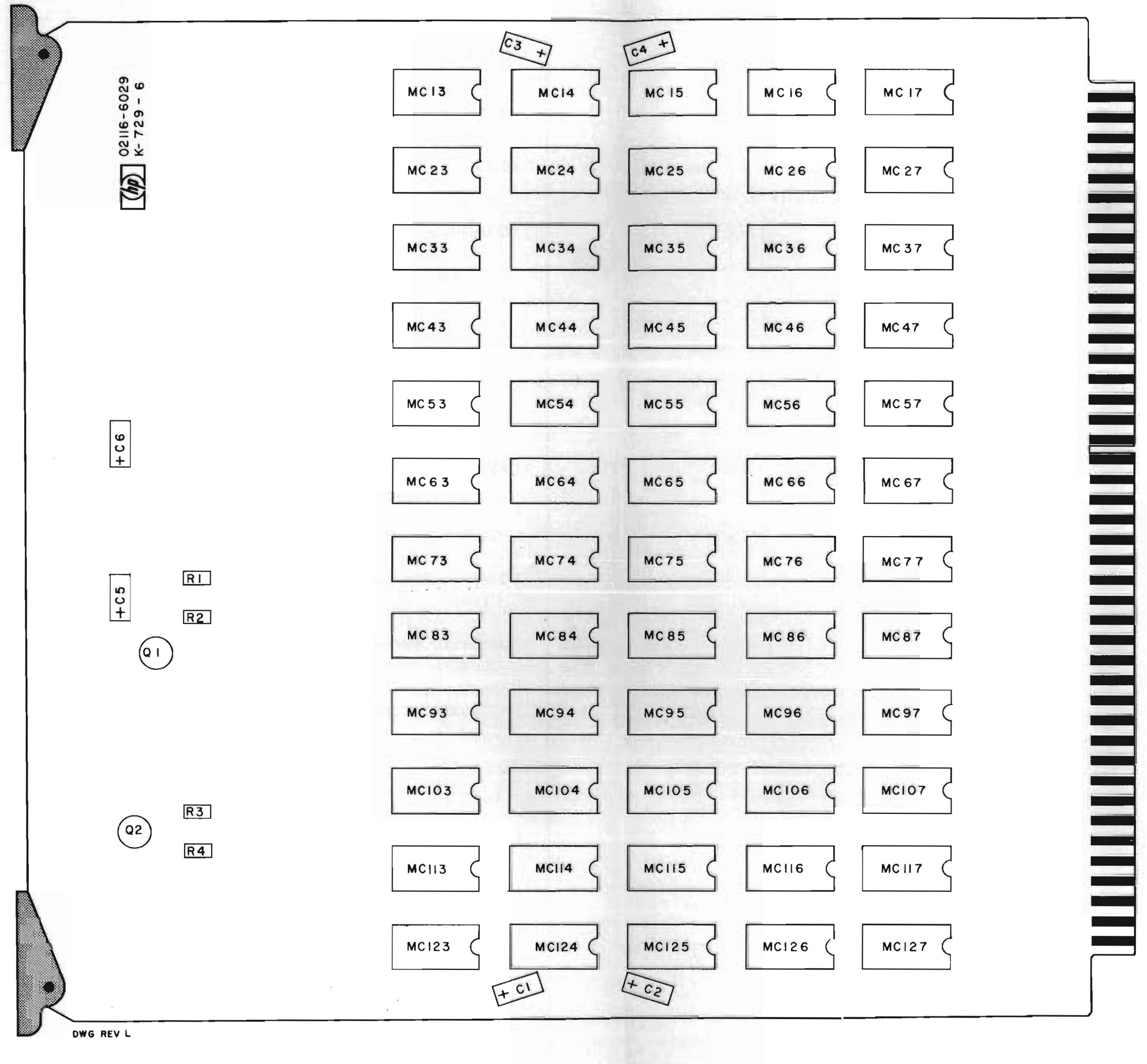
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
T4T5 (Time Periods 4 and 5)	A106-16	A108-21	See source
T5 (Time Period 5)	A106-69	A108-46	See source
T6T7 (Time Periods 6 and 7)	A106-30	A108-72	See source
T7 (Time Period 7)	A106-18	A108-83	See source
TAN1 (T-Bus Bits 0 thru 3 "anded")	A105-43	A108-58	See source
TAN2 (T-Bus Bits 4 thru 7 "anded")	A104-43	A108-57	See source
TAN3 (T-Bus Bits 8 thru 11 "anded")	A103-43	A108-60	See source
TAN4 (T-Bus Bits 12 thru 15 "anded")	A102-43	A108-59	See source
TB0 (T-Bus Bit 0)	A105-69 A110-79	A108-51	See source or option
TB1 (T-Bus Bit 1)	A105-13	A108-75	See source
TB2 (T-Bus Bit 2)	A105-55	A108-67	See source
TB3 (T-Bus Bit 3)	A105-17	A108-78	See source
TB12 (T-Bus Bit 12)	A102-69	A108-76	See source
TB13 (T-Bus Bit 13)	A102-13	A108-73	See source
TB14 (T-Bus Bit 14)	A102-55	A108-70	See source
TB15 (T-Bus Bit 15)	A102-17 A110-80	A108-20	See source or option
TR0 (T-Register Bit 0)	A105-58	A108-12	See source
$\overline{\text{TR0}}$ ("not" T-Register Bit 0)	A105-54	A108-24	See source
TR0(B) (T-Register Bit 0, Buffered)	A108-4	A202-83	= TR0
$\overline{\text{TR1}}$ ("not" T-Register Bit 1)	A105-10	A108-27	See source
$\overline{\text{TR2}}$ ("not" T-Register Bit 2)	A105-53	A108-33	See source
TR2(B) (T-Register Bit 2, Buffered)	A108-15	A202-53	= TR2
$\overline{\text{TR3}}$ ("not" T-Register Bit 3)	A105-15	A108-10	See source
$\overline{\text{TR4}}$ ("not" T-Register Bit 4)	A104-54	A108-79	See source

Table 7-43. A108 Shift Logic Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
$\overline{TR5}$ ("not" T-Register Bit 5)	A104-10	A108-6	See source
TR6 (T-Register Bit 6)	A104-56	A108-3	See source
$\overline{TR6}$ ("not" T-Register Bit 6)	A104-53	A108-23	See source
TR7 (T-Register Bit 7)	A104-16	A108-11	See source
$\overline{TR7}$ ("not" T-Register Bit 7)	A104-15	A108-30	See source
TR8 (T-Register Bit 8)	A103-58	A108-18	See source
$\overline{TR8}$ ("not" T-Register Bit 8)	A103-54	A108-36	See source
TR9 (T-Register Bit 9)	A103-9	A108-17	See source
TR11 (T-Register Bit 11)	A103-16	A108-43	See source
$\overline{TR11}$ ("not" T-Register Bit 11)	A103-15	A108-55	See source
TS (Time Strobe)	A106-55	A108-74	See source

Table 7-44. A108 Shift Logic Card (02116-6029), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	56289	150D225X0020A2
MC13,15,17,23,25,27,33,35,37,43, 44,46,47,53,54,64,65,67,77, 83,84,96,97,104,106,123	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC14,36,55,65,74,85,103,107,113, 117,124	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC16,26,34,45,56,64,75,76,94, 127	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC24,63,86,87,93,105,114,126	1820-0954	Integrated Circuit, CTL	07263	SL3457
MC73,95,115,116,123	1820-0967	Integrated Circuit, CTL	07263	SL3464
Q1,2	1854-0246	Transistor, Si, NPN	07263	2N3643
R1,3	0683-3305	Resistor, Fxd, Comp, 33 ohms, 5%, 1/4W	01121	CB3305
R2,4	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715



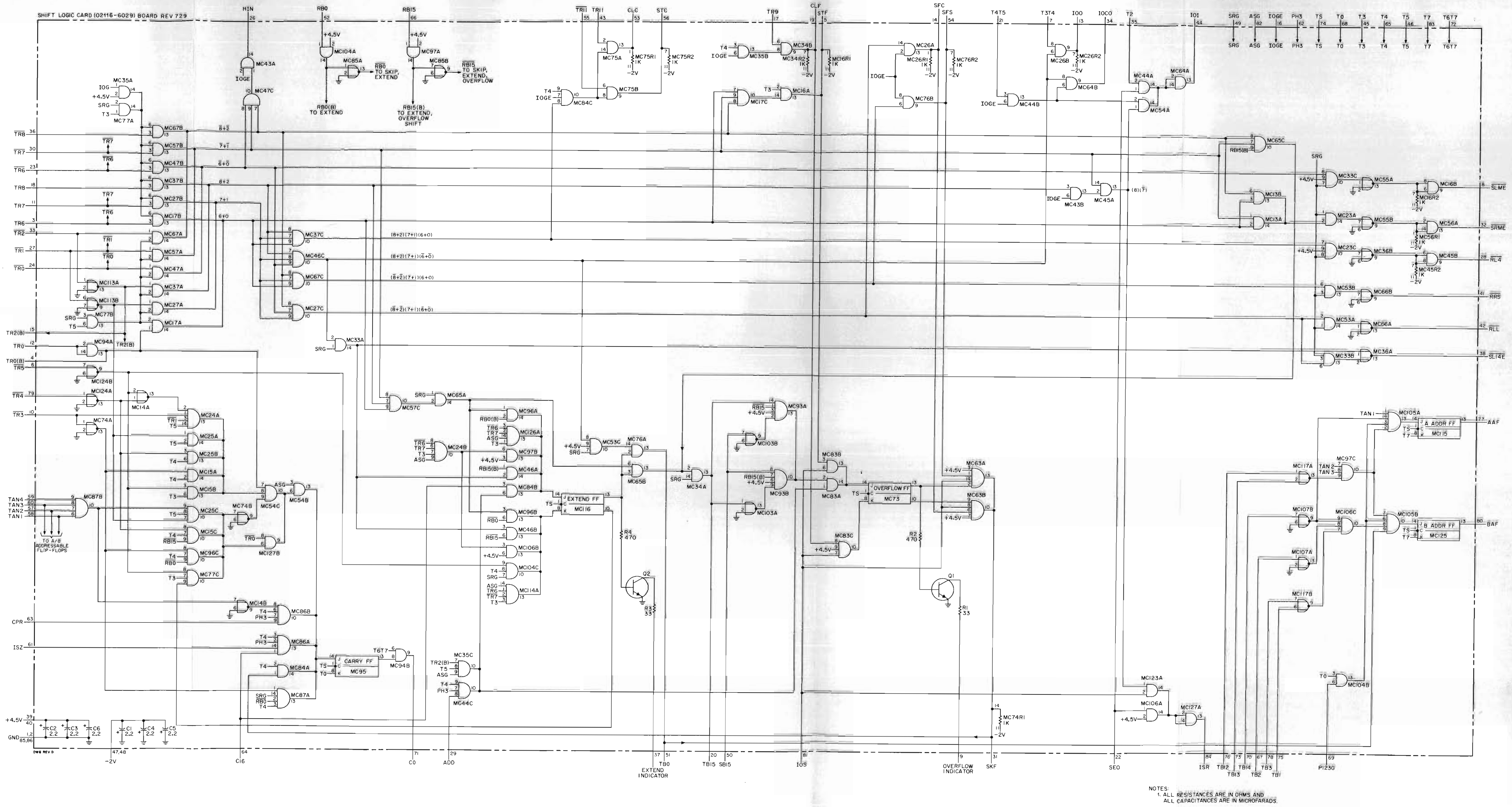


Figure 7-15. A108 Shift Logic Card (02116-6029), Parts Location and Schematic Diagram

Table 7-45. A109 Extended Arithmetic Timing Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A109-47 A109-48	None
+4.5V	A100E1	A109-39 A109-40	None
AS (Arithmetic Shift, EAU)	A109-50	A110-84	See option
CLF (Clear Flag)	A108-19 A4-14 A109-24	A1-51 A4-14 A6-7 A15-51 A201-51 A203-7 thru A220-7	See source or option
CRS (Control Reset to I/O)	A201-65	A109-68	See source
D1 (Divide Operation Cycle 1)	A109-34	A110-62	See option
D2 (Divide Operation Cycle 2)	A109-33	A110-60	See option
D3 (Divide Operation Cycle 3)	A109-26	A110-27	See option
D4 (Divide Operation Cycle 4)	A109-25	A110-6	See option
D5 (Divide Operation Cycle 5)	A109-17	A110-73	See option
D5L8 (Divide Operation Cycle 5, Loop 8)	A109-27	A110-71	See option
D6 (Divide Operation Cycle 6)	A109-18	A110-8	See option
DL3 (Double Load Operation Cycle 3)	A109-57	A110-70	See option
DL4 (Double Load Operation Cycle 4)	A109-36	A110-18	See option
DS3 (Double Store Operation Cycle 3)	A109-28	A110-67	See option
DS34 (Double Store Operation Cycles 3 and 4)	A109-6	A110-14	See option
DS4 (Double Store Operation Cycle 4)	A109-9	A110-52	See option
EXIT (Exit MAC Operation Sequence)	A109-74	A110-17	See option
GATE (Gate FF, set-side output)	A109-59	A110-76	See option

Table 7-45. A109 Extended Arithmetic Timing Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
GND (Ground)	A100E2	A109-1 A109-2 A109-85 A109-86	None
IIR (Inhibit Instruction Register)	A109-77	A14-71 A16-69 A106-6	See option
IOS (Input/Output Switch Address)	A201-6 A109-29	A108-81	See source or option
ISG (Inhibit Strobe Generator)	A109-63	A4-3 A106-4	See option
MAC (Macro Group)	A107-5	A109-62	See source
MD2 (Multiply/Divide Operation Cycle 2)	A109-79	A110-16	See option
MP1 (Multiply Operation Cycle 1)	A109-12	A110-59	See option
MP2 (Multiply Operation Cycle 2)	A109-11	A110-5	See option
MP3 (Multiply Operation Cycle 3)	A109-4	A110-69	See option
MP4 (Multiply Operation Cycle 4)	A109-3	A110-46	See option
MP5 (Multiply Operation Cycle 5)	A109-8	A110-9	See option
OASL (Overflow Due to Arithmetic Shift Left)	A110-31	A109-5	See option
OVD (Overflow Due to Divide Operation)	A110-56	A109-80	See option
OVR (Overflow Register)	A110-35	A109-22	See option
$\overline{\text{OVR}}$ ("not" Overflow Register)	A110-64	A109-16	See option
P123 (Phase 1, Phase 2, or Phase 3)	A109-13	A14-68 A15-52 A16-63 A107-78	See option
PH1 (Phase 1, Fetch)	A106-41	A109-81	See source
PH5 (Phase 5, DMA)	A4-8	A109-53	See option
$\overline{\text{RF2}}$ ("not" Run FF 2)	A106-58	A109-54	See source
RO (Rotate)	A109-46	A110-75	See option

Table 7-45. A109 Extended Arithmetic Timing Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
ROT5 (Rotate at Time Period 5)	A109-82	A110-68	See option
RSDS (Reset, Double Store Operation)	A16-15	A109-65	See source
RSET (Reset CARX FF)	A109-42	A110-63	See option
RT (Right Shift or Rotate)	A109-52	A110-57	See option
$\overline{\text{RT}}$ ("not" Right Shift or Rotate)	A109-58	A110-78	See option
SRCS (Shift-Rotate Count Started)	A109-31	A110-83	See option
SL14B (Shift Left Bit 14, Buffered)	A109-49	A14-84	See option
SLMB (Shift Left Magni-tude, Buffered)	A109-44	A14-73	See option
SRMB (Shift Right Magni-tude, Buffered)	A109-41	A14-61	See option
STF (Set Flag)	A108-5 A109-15	A4-16 A15-18 A201-41 A203-9 thru A220-9	See source or option
T0 (Time Period 0)	A106-28	A109-51	See source
T1 (Time Period 1)	A106-53	A109-71	See source
T2 (Time Period 2)	A106-76	A109-43	See source
T2T3(B) (Time Periods 2 and 3, Buffered)	A110-21	A109-35	See option
T3 (Time Period 3)	A106-63	A109-75	See source
T4 (Time Period 4)	A106-54	A109-55	See source
T5 (Time Period 5)	A106-69	A109-67	See source
T6 (Time Period 6)	A106-11	A109-60	See source
T6T7 (Time Periods 6 and 7)	A106-30	A109-14	See source
T7 (Time Period 7)	A106-18	A109-73	See source
T7S (Time Period 7 with Strobe)	A106-51	A109-23	See source
TB15 (T-Bus Bit 15)	A102-17	A109-64	See source
TEV (Time Bits, Even Numbered)	A109-56	A110-81	See option

Table 7-45. A109 Extended Arithmetic Timing Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TOD (Time Bits, Odd Numbered)	A109-45	A110-82	See option
TR0 (T-Register Bit 0)	A105-58	A109-37	See source
TR1 (T-Register Bit 1)	A105-9	A109-30	See source
TR2 (T-Register Bit 2)	A105-56	A109-38	See source
TR3 (T-Register Bit 3)	A105-16	A109-32	See source
TR4 (T-Register Bit 4)	A104-58	A109-72	See source
TR5 (T-Register Bit 5)	A104-9	A109-69	See source
TR6 (T-Register Bit 6)	A104-56	A109-66	See source
TR7 (T-Register Bit 7)	A104-16	A109-83	See source
TR8 (T-Register Bit 8)	A103-58	A109-78	See source
TR9 (T-Register Bit 9)	A103-9	A109-61	See source
TR11 (T-Register Bit 11)	A103-16	A109-84	See source
$\overline{\text{TR11}}$ ("not" T-Register Bit 11)	A103-15	A109-70	See source
TSA (Time Strobe A)	A106-67	A109-76	See source

Table 7-46. A110 Extended Arithmetic Logic Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A110-47 A110-48	None
+4.5V	A100E1	A110-39 A110-40	None
ADF (Add Function)	A110-12	A102-5 A103-5 A104-5 A105-5	See option
AS (Arithmetic Shift)	A109-50	A110-84	See option
C16 (Carry Bit 16)	A102-36	A110-50	See source
CMFB (Complement Function, Buffered)	A110-72	A14-80	See option
D1 (Divide Operation Cycle 1)	A109-34	A110-62	See option
D2 (Divide Operation Cycle 2)	A109-33	A110-60	See option
D3 (Divide Operation Cycle 3)	A109-26	A110-27	See option
D4 (Divide Operation Cycle 4)	A109-25	A110-6	See option
D5 (Divide Operation Cycle 5)	A109-17	A110-73	See option
D5L8 (Divide Operation Cycle 5, Loop 8)	A109-27	A110-71	See option
D6 (Divide Operation Cycle 6)	A109-18	A110-8	See option
DL3 (Double Load Operation Cycle 3)	A109-57	A110-70	See option
DL4 (Double Load Operation Cycle 4)	A109-36	A110-18	See option
DS3 (Double Store Operation Cycle 3)	A109-28	A110-67	See option
DS34 (Double Store Operation Cycles 3 and 4)	A109-6	A110-14	See option
DS4 (Double Store Operation Cycle 4)	A109-9	A110-52	See option
EOFB (Exclusive OR Function, Buffered)	A110-26	A14-82	See option
EXIT (Exit MAC Operation Sequence)	A109-74	A110-17	See option
GATE (Gate FF, Set-side output)	A109-59	A110-76	See option

Table 7-46. A110 Extended Arithmetic Logic Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
GND (Ground)	A100E2	A110-1 A110-2 A110-85 A110-86	None
MD2 (Multiply/Divide Operation Cycle 2)	A109-79	A110-16	See option
MP1 (Multiple Operation Cycle 1)	A109-12	A110-59	See option
MP2 (Multiply Operation Cycle 2)	A109-11	A110-5	See option
MP3 (Multiply Operation Cycle 3)	A109-4	A110-69	See option
MP4 (Multiply Operation Cycle 4)	A109-3	A110-46	See option
MP5 (Multiply Operation Cycle 5)	A109-8	A110-9	See option
OASL (Overflow Due to Arithmetic Shift Left)	A110-31	A109-5	See option
OVD (Overflow Due to Divide Operation)	A110-56	A109-80	See option
OVR (Overflow Register)	A110-35	A109-22	See option
$\overline{\text{OVR}}$ ("not" Overflow Register)	A110-64	A109-16	See option
RARB (Read A-Register to the R bus)	A110-65	A102-34 A103-34 A104-34 A105-34	See option
RB0 (R bus Bit 0)	A110-43	A105-37 A108-52	See option
RB14 (R bus Bit 14)	A102-71	A110-25	See source
RB15 (R bus Bit 15)	A102-30	A110-77	See source
RBRB (Read B-Register to the R bus)	A110-58	A102-28 A103-28 A104-28 A105-28	See option
RMSB (Read M-Register to the S bus)	A110-34	A102-8 A103-8 A104-8 A105-8	See option
RO (Rotate)	A109-46	A110-75	See option
ROT5 (Rotate at Time Period 5)	A109-82	A110-68	See option

Table 7-46. A110 Extended Arithmetic Logic Card, Signal List (Continued)

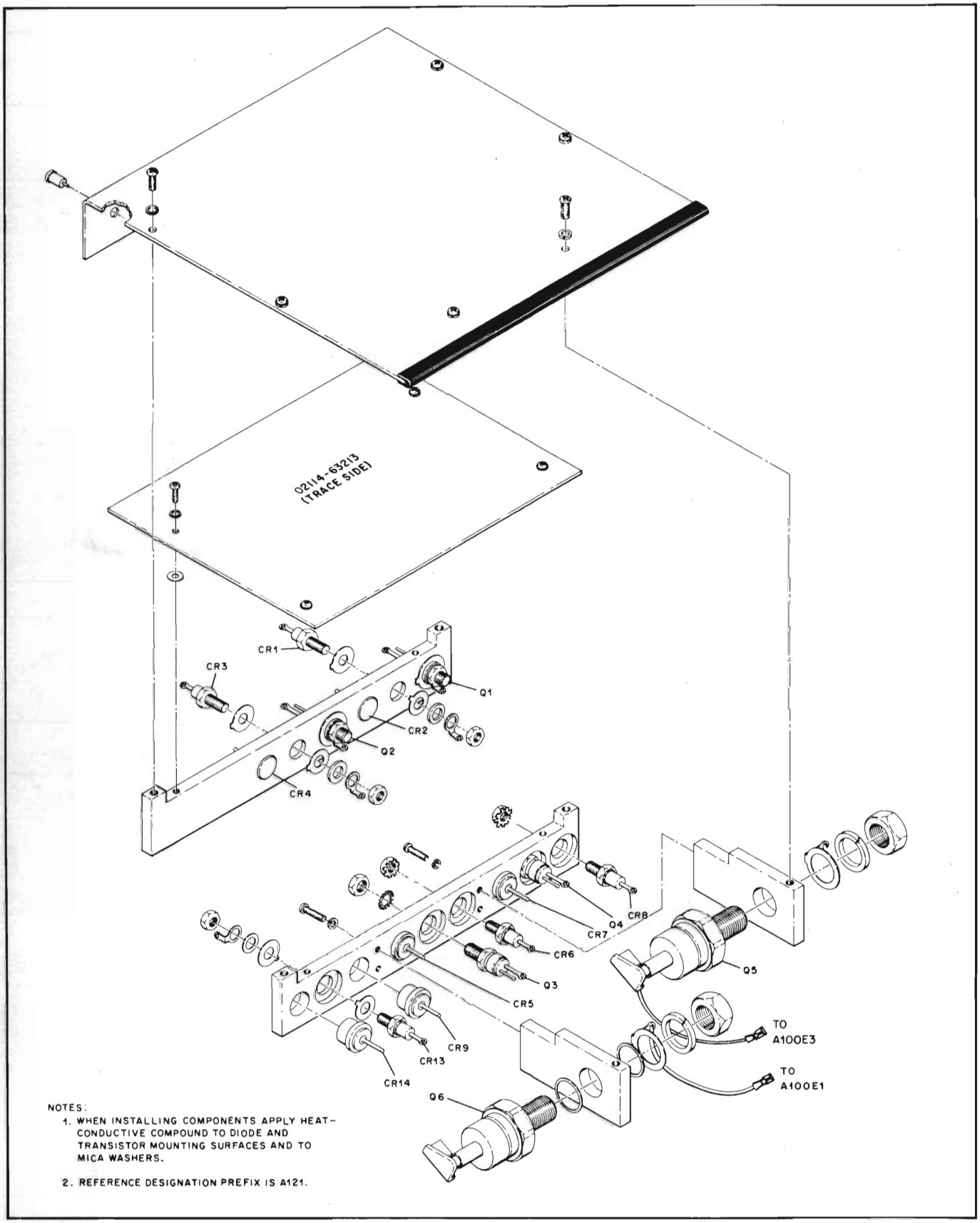
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
RPRB (Read P-Register to the R bus)	A110-4	A102-12 A103-12 A104-12 A105-12	See option
RSET (Reset CARX FF)	A109-42	A110-63	See option
RT (Right Shift or Rotate)	A109-52	A110-57	See option
$\overline{RT}$ ("not" Right Shift or Rotate)	A109-58	A110-78	See option
RTSB (Read T-Register to the S bus)	A110-19	A1-60 A102-20 A103-20 A104-20 A105-20	See option
SB0 (S bus Bit 0)	A110-44	A105-42	See option
SRCS (Shift Rotate Count Started)	A109-31	A110-83	See option
SWSA (Switch Store in A-Register)	A106-84 A110-66	A107-35	See source or option
SWSB (Switch Store in B-Register)	A110-10	A107-24	See option
SWSM (Switch Store in M-Register)	A110-33	A107-26	See option
SWSP (Switch Store in P-Register)	A106-64 A110-3	A107-37	See source or option
SWST (Switch Store in T-Register)	A106-62 A4-83 A110-20	A107-34	See source or option
T0 (Time Period 0)	A106-28	A110-15	See source
T0T1 (Time Periods 0 and 1)	A106-17	A110-36	See source
T1 (Time.Period 1)	A106-53	A110-13	See source
T1T2 (Time Periods 1 and 2)	A106-21	A110-51	See source
T2 (Time Period 2)	A106-76	A110-22	See source
T2T3(B) (Time Periods 2 and 3, Buffered)	A110-21	A109-35	See option
T3 (Time Period 3)	A106-63	A110-32	See source
T3T4 (Time Periods 3 and 4)	A106-15	A110-74	See source
T4 (Time Period 4)	A106-54	A110-24	See source

Table 7-46. A110 Extended Arithmetic Logic Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
T4T5 (Time Periods 4 and 5)	A106-16	A110-23	See source
T5 (Time Period 5)	A106-69	A110-54	See source
T6 (Time Period 6)	A106-11	A110-30	See source
T6T7 (Times Periods 6 and 7)	A106-30	A110-11	See source
T7 (Time Period 7)	A106-18	A110-28	See source
TB0 (T bus Bit 0)	A105-69 A110-79	A102-81 A108-51 A202-10	See source or option
TB15 (T bus Bit 15)	A102-17 A110-80	A103-45 A105-77 A108-20 A109-64	See source or option
TEV (Time Bits, Even Numbered)	A109-56	A110-81	See option
TOD (Time Bits, Odd Numbered)	A109-45	A110-82	See option
TSA (Time Strobe A)	A106-67	A110-29	See source

Table 7-47. A121 Overvoltage Protection Assembly (02116-63218) Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
A121A1	02116-63213	Overvoltage Component Board Assembly (see table 7-48)	28480	02116-63213
CR1,6	1902-1205	Diode, Breakdown, 15V, +2%	04713	1N2979R8
CR2,4,14	1901-0343	Diode, Si, 50 PIV, 18A	04713	1N3491R
CR3,8	1902-1228	Diode, Breakdown, 27V, 10%, 10W	28480	1902-1228
CR5,7,9	1901-0406	Diode, Si, PIV, 18A	04713	1N3491/MR-322
CR13	1902-1217	Diode, Breakdown, 39V, 2%	04713	SZ11747
Q1 thru Q4	1884-0046	Thyristor, SCR, 50V, 25A	28480	1884-0046
Q5,6	1884-0047	Thyristor, SCR, 25V, 55A	01002	C45UX123



2107-27B

Figure 7-16. A121 Overvoltage Protection Assembly, (02116-63218), Parts Location Diagram

Table 7-48. A121A1 Overvoltage Component Board Assembly (02116-63213), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW	56289	C023F101F103Z-E12CDH
CR10 thru CR12	1901-0191	Diode, Si, 0.75A, 100 PIV	04713	SR1358-2
R1,5,13,18	0686-2205	Resistor, Fxd, Comp, 22 ohms, 5%, 1/2W	01121	EB2205
R2,6,12,17	0686-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/2W	01121	EB4715
R3,4,7,8,10,11,15,16	0813-0038	Resistor, Fxd, ww, 0.5 ohms, 5%, 10W	28480	0813-0038
R9,14	0811-1857	Resistor, Fxd, ww, 400 ohms, 5%, 5W	28480	0811-1857
R19,22	0689-3315	Resistor, Fxd, Comp, 220 ohms, 5%, 1/2W	01121	EB2215
R20,21	0689-1505	Resistor, Fxd, Comp, 15 ohms, 5%, 1W	01121	GB1505

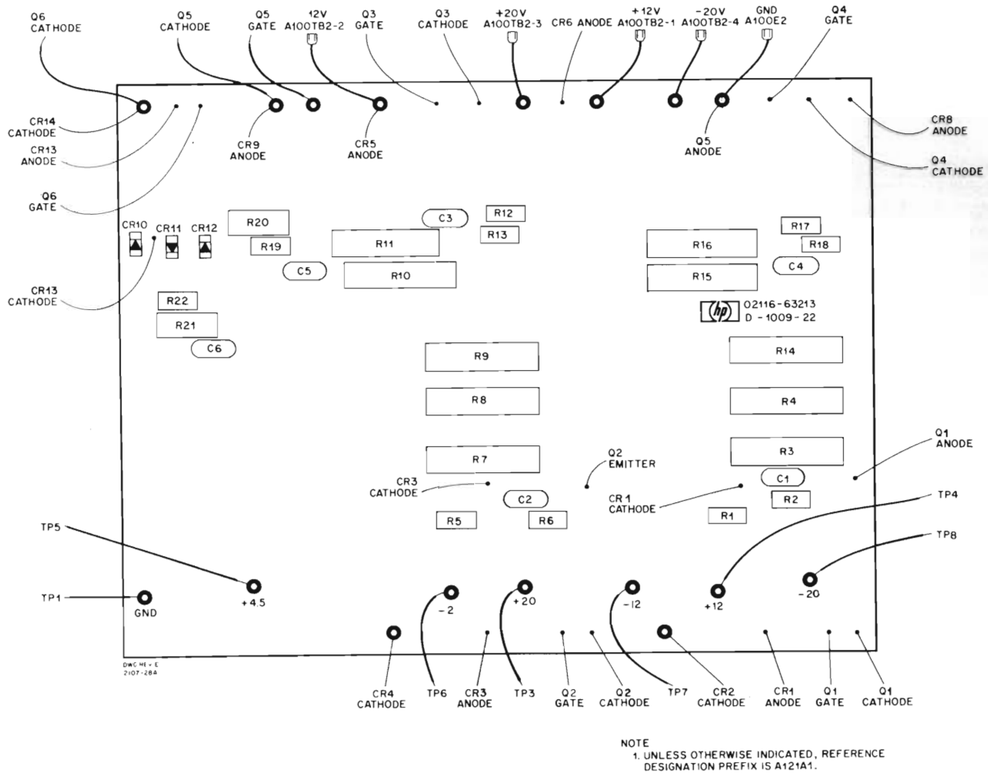


Figure 7-17. A121A1 Overvoltage Component Board (02116-63213), Parts Location and Connection Diagram

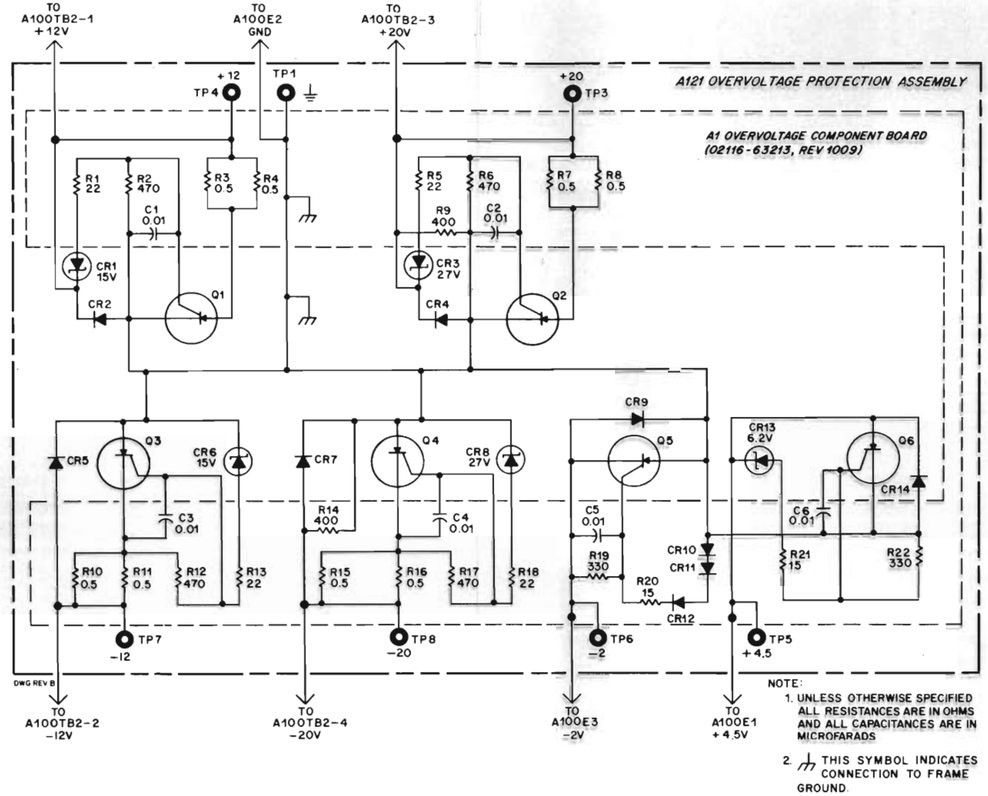


Figure 7-18. A121 Overvoltage Protection Assembly (02116-63218), Schematic Diagram

Table 7-49. A201 I/O Control Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
-2V	A100E3	A201-47 A201-48	None
+4.5V	A100E1	A201-39 A201-40	None
+12V	A100TB2-1	A201-43 A201-44	None
-12V	A100TB2-2	A201-69 A201-70	None
CLC (Clear Control)	A108-53	A201-75	See source
CLF (Clear Flag)	A4-14 A108-19 A109-24	A201-51	See source
CRS (Control Reset to I/O)	A201-65	A1-9 A2-9 A3-74 A4-32 A109-68 A203-13 thru A220-13	= POPIO
ENF (Enable Flag)	A201-67	A3-49 A4-37 A6-46 A15-71 A203-46 thru A220-46	= T2
ESR (Enable Service Request)	A201-21	A202-12	= $\overline{\text{HIS}}$ + Interrupt Control FF + Interrupt System Enable FF + $\overline{\text{POPIO}}$
GND (Ground)	A100E2	A201-1 A201-2 A201-85 A201-86	None
HIS (Hold Interrupt System)	A3-83	A201-4	See option
IAK (Interrupt Acknowledge)	A201-77	A1-44 A4-27 A6-10 A15-38 A16-56 A203-10 thru A220-10	= PH1 · T1 · Interrupt Control FF
IEN6 (Interrupt Enable 6)	A201-10	A1-35 A4-7 A16-53 A201-5	= Interrupt System Enable FF

Table 7-49. A201 I/O Control Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IEN10 (Interrupt Enable 10)	A201-8	A203-8 thru A210-8	= Interrupt System Enable FF · PRH10
IEN20 (Interrupt Enable 20)	A201-7	A211-8 A211-23 A212-8 thru A218-8 A220-4	= PRH10 · PRL17 · IEN6
INTERRUPT CONTROL FF	– –	– –	Set = $\overline{\text{Interrupt Timing FF}}$ Direct Clear = CRS + PH4 · T3(B) + IOGE(B) · $\overline{\text{PH5}}$ · TS · STC + IOGE(B) · $\overline{\text{PH5}}$ · TS · STF + IOGE(B) · $\overline{\text{PH5}}$ · TS · CLC + IOGE(B) · $\overline{\text{PH5}}$ · TS · CLF
INTERRUPT SYSTEM ENABLE FF	– –	– –	Set = IOGE(B) · SCM0 · SCL0 · STF Clear = IOGE(B) · SCM0 · SCL0 · CLF
INTERRUPT TIMING FF	– –	– –	Set = STM12-15 Clear = T0 · TS
IOGE (Input/Output Instruction Group, Buffered)	A6-59 A16-19	A201-33	See source or option
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A1-11 A2-11 A3-84 A4-22 A6-15 A202-34 A203-15 thru A220-15	= IOGE delayed
IOS (Input/Output Switch Address)	A109-29 A201-6	A108-81	= IOGE(B) · SCL1 · SCM0 + EAU option signal
PH1 (Phase 1, Fetch)	A106-41	A201-29	See source
PH4 (Phase 4, Interrupt)	A106-13	A201-53	See source
PH4/5 SYNC 1 FF (Phase 4 or 5, Synchronization 1 FF)	– –	– –	Direct Set = T3(B) · PH4 + PH5 · PH4/5 SYNC 1 · PH4/5 SYNC 2 J = – – K = +4.5V Clock = $\overline{\text{IAK}}$ Direct Clear = POPIO(B)
PH4/5 SYNC 2 FF (Phase 4 or 5, Synchronization 2 FF)	– –	– –	Set = $\overline{\text{T5}}$ Direct Clear = T0
PH5 (Phase 5)	A4-8	A201-17	See option
$\overline{\text{PH5}}$ ("not" Phase 5)	A201-9	A202-4	= PH5 inverted
POPIO (Power On Pulse to I/O)	A106-61	A201-63	See source

Table 7-49. A201 I/O Control Card, Signal List (Continued)

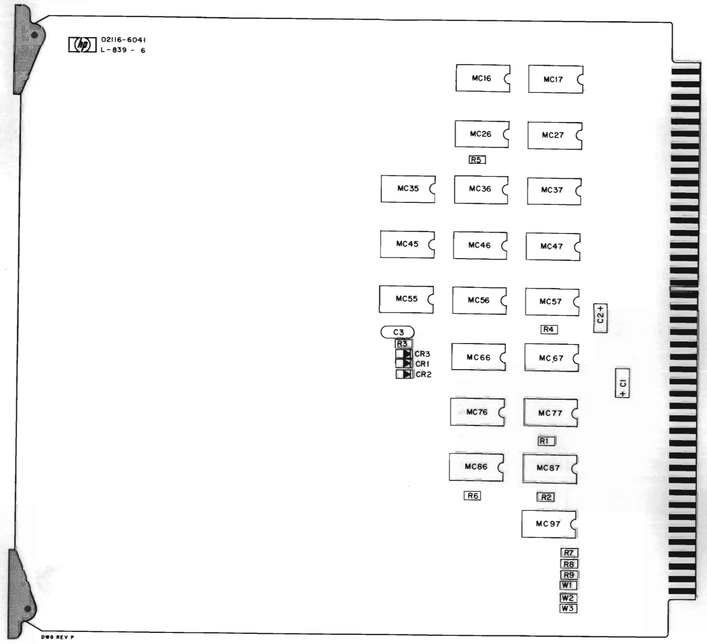
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
POPIO(B) (Power On Pulse to I/O, Buffered)	A201-72	A4-35 A16-29 A203-17 thru A220-17	= POPIO
PRH5/PRL4 (Priority High Select Code 5/Priority Low Select Code 4)	A6-3	A201-84	See source
RPH6/PRL5 (Priority High Select Code 6/Priority Low Select Code 5)	A15-27 A16-51	A1-33 A201-76 A201-82	See option
PRH10/PRL7 (Priority High Select Code 10/Priority Low Select Code 7)	A4-9 A201-80	A201-12 A201-14 A203-23	See option
PRH20/PRL17 (Priority High Select Code 20/Priority Low Select Code 17)	A210-3	A201-16	See option
PRL6 (Priority Low Select Code 6)	A201-78	A1-23 A4-31	= PRH6/PRL5
SCL0 (Select Code Least Significant Digit, Octal 0)	A202-65	A201-38	See source
SCL1 (Select Code Least Significant Digit, Octal 1)	A202-67	A201-42	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A201-36	See source
SFC (Skip if Flag Clear)	A108-14	A201-71	See source
SFS (Skip if Flag Set)	A108-54	A201-68	See source
SIR (Service Interrupt Request)	A201-35	A1-53 A2-53 A3-70 A4-34 A6-32 A15-37 A16-36 A203-32 thru A220-32	= T5
SKF (Skip On Flag)	A201-73 A203-12 thru A220-12	A1-15 A4-29 A6-12 A108-31	= IOGE(B) · SCM0 ; SCL0 · SFS · Interrupt System Enable FF + IOGE(B) · SCM0 · SCL0 · SFC · Interrupt System Enable FF + I/O Interface option signal
STC (Set Control)	A108-56	A201-61	See source

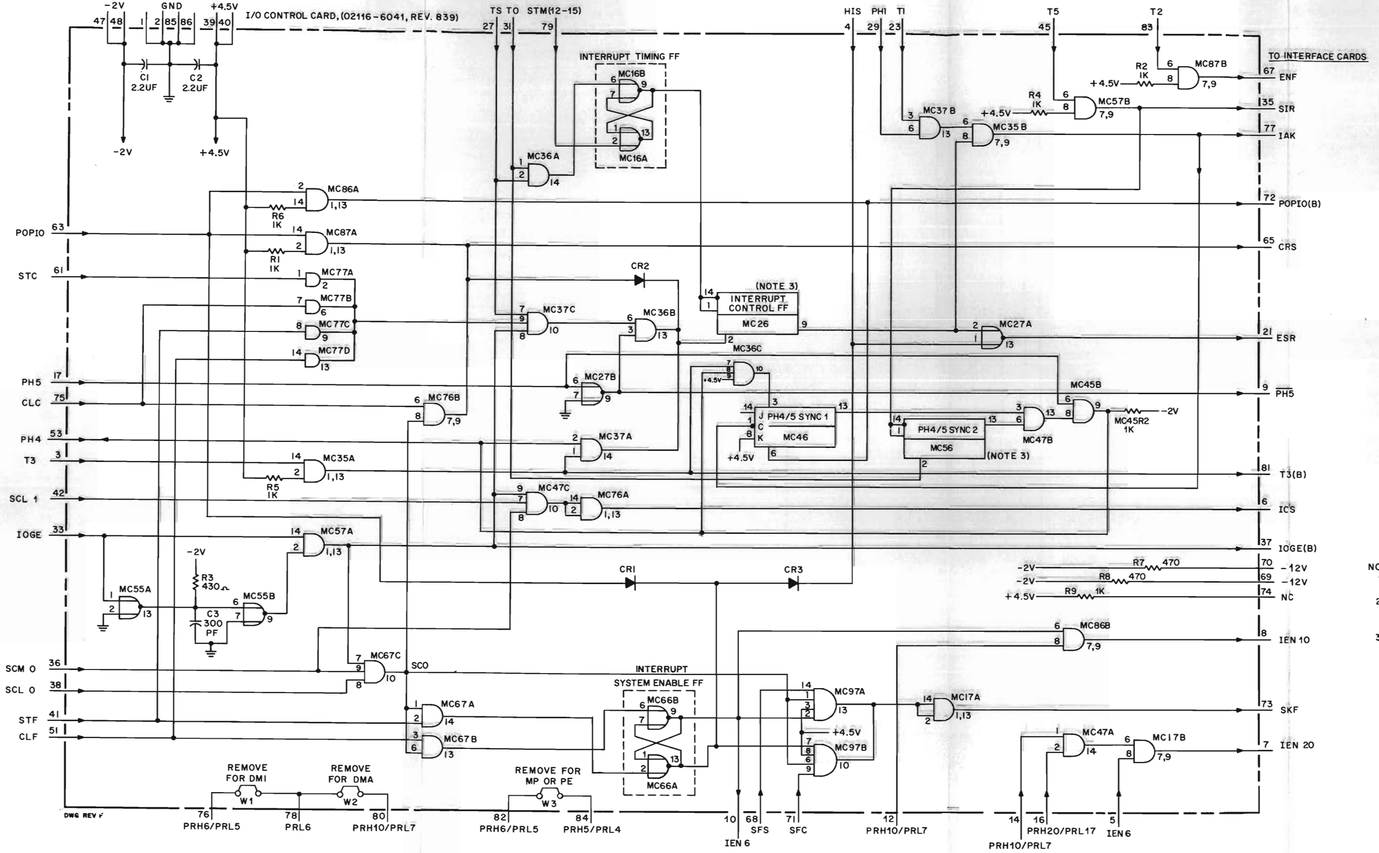
Table 7-49. A201 I/O Control Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
STF (Set Flag)	A108-5 A109-15	A201-41	See source or option
STM12-15 (Store T Bus Bits 12 thru 15 in M-Register)	A107-28	A201-79	See source
T0 (Time Period 0)	A106-28	A201-31	See source
T1 (Time Period 1)	A106-53	A201-23	See source
T2 (Time Period 2)	A106-76	A201-83	See source
T3 (Time Period 3)	A106-63	A201-3	See source
T3(B) (Time Period 3, Buffered)	A201-81	A1-5 A2-5 A203-11 thru A220-11	= T3
T5 (Time Period 5)	A106-69	A201-45	See source
TS (Time Strobe)	A106-55	A201-27	See source

Table 7-50. A201 I/O Control Card (02116-6041), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	56289	150D225X0020A2-DYS
C3	0140-0225	Capacitor, Fxd, Mica, 300 pF, 1%	28480	0140-0225
CR1 thru CR3	1910-0022	Diode, Ge, 5 WIV	28480	1910-0022
MC16,27,55,66	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC17,35,45,57,76,86,87	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC26,56	1820-0957	Integrated Circuit, CTL	07263	SL3460
MC36,37,47,67	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC46	1820-0967	Integrated Circuit, CTL	07263	SL3464
MC77	1820-0965	Integrated Circuit, CTL	07263	SL3462
MC97	1820-0954	Integrated Circuit, CTL	07263	SL3457
R1,2,4,5,6,9	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R3	0757-0915	Resistor, Fxd, Flm, 430 ohms, 2%, 1/8W	28480	0757-0915
R7,8	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715
W1 thru W3	8159-0005	Jumper Wire	28480	8159-0005





NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.
2. THE TIMING CHART DOES NOT RELATE SIGNALS TO THE MACHINE PHASE IN WHICH THEY OCCUR.
3. THE FOLLOWING IS A MICROCIRCUIT PACKAGE DIAGRAM OF MC26 AND MC56:

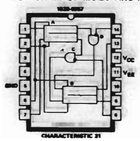


Figure 7-19. A201 I/O Control Card (02116-6041), Parts Location and Schematic Diagram

Table 7-51. A202 I/O Address Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A202-47 A202-48	None
+4.5V	A100E1	A202-39 A202-40	None
-12V	A100TB2-2	A202-69 A202-70	None
+12V	A100TB2-1	A202-43 A202-44	None
CIF 0 (Central Interrupt FF 0)	--	--	L = SRA0 C = RSM6-9
CIF 1 (Central Interrupt FF 1)	--	--	L = SRA1 C = RSM6-9
CIF 2 (Central Interrupt FF 2)	--	--	L = SRA2 C = RSM6-9
CIF 3 (Central Interrupt FF 3)	--	--	L = SRA3 C = RSM6-9
CIF 4 (Central Interrupt FF 4)	--	--	L = SRA4 C = RSM6-9
CIF 5 (Central Interrupt FF 5)	--	--	L = SRA5 C = RSM6-9
ESR (Enable Service Request)	A201-21	A202-12	See source
FLG 0 (Flag from Group 0)	A203-4 thru A210-4 A203-49 thru A209-49	A202-14	See option
FLG 1 (Flag From Group 1)	A210-49 thru A218-49 A211-4 thru A218-4 A219-26	A202-16	See option
FLG2 (Flag From Group 2)	A219-28	A202-13	See option
FLG3 (Flag From Group 3)	A219-30	A202-15	See option
GND (Ground)	A100E2	A202-1 A202-2 A202-85 A202-86	None
INT (Interrupt)	A6-28 A15-79 A16-31	A106-44 A202-3	= ESR · FLG0 + FLG1 + FLG2 + FLG3

Table 7-51. A202 I/O Address Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 : ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI0 FF + IOGE · IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI1 FF + IOGE · IOI · SC · DATA BIT 1
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	= DMA option signal + MP option signal + SWR2 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI2 FF + IOGE · IOI · SC · DATA BIT 2
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 : ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI3 FF + IOGE · IOI · SC · DATA BIT 3
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI4 FF + IOGE · IOI · SC · DATA BIT 4

Table 7-51. A202 I/O Address Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI5 FF + IOGE · IOI · SC · DATA BIT 5
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A202-34	See source
IOI (Input/Output, Input)	A4-81 A4-84 A108-44	A202-24	See source or option
IRQ1 (Interrupt Request 1)	A211-33 A212-6 A219-50	A202-17	See option
IRQ2 (Interrupt Request 2)	A212-33 A213-6 A219-52	A202-21	See option
IRQ3 (Interrupt Request 3)	A213-33 A214-6 A219-54	A202-23	See option
IRQ4 (Interrupt Request 4)	A214-33 A215-6 A219-56	A202-27	See option
IRQ5 (Interrupt Request 5)	A16-35 A215-33 A216-6 A219-58	A202-29	See option
IRQ6 (Interrupt Request 6)	A4-28 A216-33 A217-6 A219-60	A202-25	See option
IRQ7 (Interrupt Request 7)	A4-26 A217-33 A218-6 A219-62	A202-19	See option
IRQ10 (Interrupt Request 10)	A203-6 A218-33 A219-64	A202-33	See option
IRQ11 (Interrupt Request 11)	A203-33 A204-6 A219-66	A202-35	See option
IRQ12 (Interrupt Request 12)	A204-33 A205-6 A219-68	A202-37	See option

Table 7-51. A202 I/O Address Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IRQ13 (Interrupt Request 13)	A205-33 A206-6 A219-72	A202-18	See option
IRQ14 (Interrupt Request 14)	A206-33 A207-6 A219-74	A202-31	See option
IRQ15 (Interrupt Request 15)	A207-33 A208-6 A219-76	A202-20	See option
IRQ16 (Interrupt Request 16)	A208-33 A209-6 A219-78	A202-38	See option
IRQ17 (Interrupt Request 17)	A210-6	A202-22	See option
$\overline{PH5}$ ("not" Phase 5)	A201-9	A202-4	See source
$\overline{RF2}$ ("not" Run FF 2)	A106-58	A202-36	See source
RSM6-9 (Reset M-Register Bits 6 thru 9)	A107-12	A202-11	See source
RUN	A202-32	A203-50 thru A218-50 A220-41	= RF2
SCL0 (Select Code Least Significant Digit, Octal 0)	A3-32 A202-65	A201-38 A203-16 A210-34 A211-16 A218-34 A220-67	= $\overline{PH5} \cdot \overline{TR0} \cdot \overline{TR1} \cdot \overline{TR2}$ + DMA option signal
SCL1 (Select Code Least Significant Digit, Octal 1)	A3-80 A202-67	A16-71 A201-42 A203-34 A204-16 A211-34 A212-16 A220-71	= $\overline{PH5} \cdot TR0 \cdot \overline{TR1} \cdot \overline{TR2}$ + DMA option signal
SCL2 (Select Code Least Significant Digit, Octal 2)	A3-18 A202-61	A1-13 A204-34 A205-16 A212-34 A213-16 A220-73	= $\overline{PH5} \cdot \overline{TR0} \cdot TR1 \cdot \overline{TR2}$ + DMA option signal
SCL3 (Select Code Least Significant Digit, Octal 3)	A3-82 A202-63	A2-13 A205-34 A206-16 A213-34 A214-16 A220-75	= $\overline{PH5} \cdot TR0$; $TR1 \cdot \overline{TR2}$ +DMA option signal

Table 7-51. A202 I/O Address Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
SCL4 (Select Code Least Significant Digit, Octal 4)	A3-38 A202-51	A6-16 A206-34 A207-16 A214-34 A215-16 A220-77	= $\overline{PH5} \cdot \overline{TR0} \cdot \overline{TR1} \cdot TR2$ +DMA option signal
SCL5 (Select Code Least Significant Digit, Octal 5)	A3-79 A202-52	A15-9 A16-12 A207-34 A208-16 A215-34 A216-16 A220-79	= $\overline{PH5} \cdot TR0 \cdot \overline{TR1} \cdot TR2$ + DMA option signal
SCL6 (Select Code Least Significant Digit, Octal 6)	A3-46 A202-49	A4-36 A208-34 A209-16 A216-34 A217-16 A220-81	= $\overline{PH5} \cdot \overline{TR0} \cdot TR1 \cdot TR2$ + DMA option signal
SCL7 (Select Code Least Significant Digit, Octal 7)	A3-50 A202-50	A4-38 A209-34 A210-16 A217-34 A218-16 A220-83	= $\overline{PH5} \cdot TR0 \cdot TR1 \cdot TR2$ + DMA option signal
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A1-14 A2-14 A3-51 A4-18 A6-14 A15-7 A16-9 A201-36 A220-55	= $PH5 \cdot \overline{TR3} \cdot \overline{TR4} \cdot \overline{TR5}$
SCM1 (Select Code Most Significant Digit, Octal 1)	A3-67 A202-77	A203-14 thru A210-14 A203-37 thru A209-37	= $\overline{PH5} \cdot TR3 \cdot \overline{TR4} \cdot \overline{TR5}$ + DMA option signal
SCM2 (Select Code Most Significant Digit, Octal 2)	A3-69 A202-71	A210-37 thru A217-37 A211-14 thru A218-14	= $\overline{PH5} \cdot \overline{TR3} \cdot TR4 \cdot \overline{TR5}$ + DMA option signal
SCM3 (Select Code Most Significant Digit, Octal 3)	A202-73	A218-37 A220-57	= $\overline{PH5} \cdot TR3 \cdot TR4 \cdot \overline{TR5}$

Table 7-51. A202 I/O Address Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SCM4 (Select Code Most Significant Digit, Octal 4)	A202-56	A220-59	= $\overline{PH5} \cdot \overline{TR3} \cdot \overline{TR4} \cdot TR5$
SCM5 (Select Code Most Significant Digit, Octal 5)	A202-57	A220-61	= $\overline{PH5} \cdot TR3 \cdot \overline{TR4} \cdot TR5$
SCM6 (Select Code Most Significant Digit, Octal 6)	A202-54	A220-63	= $\overline{PH5} \cdot \overline{TR3} \cdot TR4 \cdot TR5$
SCM7 (Select Code Most Significant Digit, Octal 7)	A202-55	A220-65	= $\overline{PH5} \cdot TR3 \cdot TR4 \cdot TR5$
SRA0 (Service Request Address 0)	– –	– –	= IRQ1 + IRQ3 + IRQ5 + IRQ7 + IRQ11 + IRQ13 + IRQ15 + IRQ17
SRA1 (Service Request Address 1)	– –	– –	= IRQ2 + IRQ3 + IRQ6 + IRQ7 + IRQ12 + IRQ13 + IRQ16 + IRQ17
SRA2 (Service Request Address 2)	– –	– –	= IRQ4 + IRQ5 + IRQ6 + IRQ7 + IRQ14 + IRQ15 + IRQ16 + IRQ17
SRA3 (Service Request Address 3)	– –	– –	= IRQ10 + IRQ 11 + IRQ 12 + IRQ13 + IRQ14 + IRQ15 + IRQ16 + IRQ17
SRA4 (Service Request Address 4)	– –	– –	= FLG 1 + FLG 3
SRA5 (Service Request Address 5)	– –	– –	= FLG 2 + FLG 3

Table 7-51. A202 I/O Address Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB0 (T Bus Bit 0)	A102-81 A105-69 A108-51 A110-79 A202-10	A105-69 A110-79	= ADF · RB0 · SB0 · C0 + ADF · RB0 · $\overline{SB0}$ · $\overline{C0}$ + ADF · $\overline{RB0}$ · SB0 · $\overline{C0}$ + ADF · $\overline{RB0}$ · $\overline{SB0}$ · C0 + ANF · RB0 · SB0 + CMF · $\overline{RB0}$ + EFF · SRG · T3 · TR8 · TR7 · $\overline{TR6}$ + EFF · SRG · T5 · TR2 · TR1 · $\overline{TR0}$ + EOF · RB0 · $\overline{SB0}$ + EOF · $\overline{RB0}$ · SB0 + IOF · RB0 + IOF · SB0 + RL4 · RB12 + RL4 · SB12 + RLL · RB15 + RLL · SB15 + RSM6-9 · SRA0 + SLM · RB15 + SLM · SB15 + SRM · RB1 + SRM · SB1 + EAU option signal
TB1 (T Bus Bit 1)	A102-75 A105-13 A202-9	A105-13 A108-75	= ADF · RB1 · SB1 · C1 + ADF · RB1 · $\overline{SB1}$ · $\overline{C1}$ + ADF · $\overline{RB1}$ · $\overline{SB1}$ · C1 + ADF · $\overline{RB1}$ · SB1 · $\overline{C1}$ + ANF · RB1 · SB1 + CMFE · $\overline{RB1}$ + EOF · RB1 · $\overline{SB1}$ + EOF · $\overline{RB1}$ · SB1 + IOF · RB1 + IOF · SB1 + RL4 · SB13 + RL4 · SB13 + RLL · RB0 + RLL · SB0 + RSM6-9 · SRA1 + SLM · RB0 + SLM · SB0 + SRM · RB2 + SRM · SB2
TB2 (T Bus Bit 2)	A102-84 A105-55 A202-8	A105-55 A108-67	= ADF · RB2 · SB2 · C2 + ADF · RB2 · $\overline{SB2}$ · $\overline{C2}$ + ADF · $\overline{RB2}$ · $\overline{SB2}$ · C2 + ADF · $\overline{RB2}$ · SB2 · $\overline{C2}$ + ANF · RB2 · SB2 + CMFE · $\overline{RB2}$ + EOF · RB2 · $\overline{SB2}$ + EOF · $\overline{RB2}$ · SB2 + IOF · RB2 + IOF · SB2 + RL4 · RB14 + RL4 · SB14 + RLL · RB1 + RLL · SB1 + RSM6-9 · SRA2 + SLM · RB1 + SLM · SB1 + SRM · RB3 + SRM · SB3

Table 7-51. A202 I/O Address Card, Signal List (Continued)

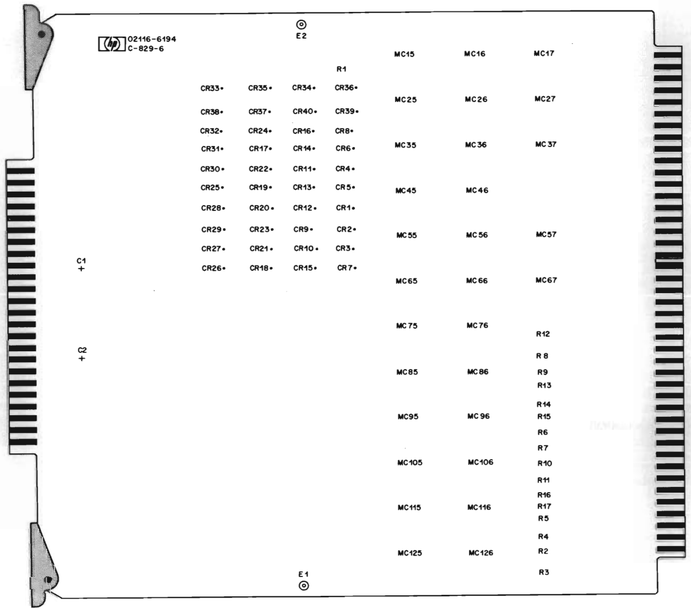
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
TB3 (T Bus Bit 3)	A102-45 A104-77 A105-17 A202-7	A105-17 A108-78	= ADF · RB3 · SB3 · C3 + ADF · RB3 · $\overline{SB3}$ · $\overline{C3}$ + ADF · $\overline{RB3}$ · $\overline{SB3}$ · C3 + ADF · $\overline{RB3}$ · SB3 · $\overline{C3}$ + ANF · RB3 · SB3 + CMFE · $\overline{RB3}$ + EOF · RB3 · $\overline{SB3}$ + EOF · $\overline{RB3}$ · SB3 + IOF · RB3 + IOF · SB3 + RL4 · RB15 + RL4 · SB15 + RLL · RB2 + RLL · SB2 + RSM6-9 · SRA3 + SLM · RB2 + SLM · SB2 + SRM · RB4 + SRM · SB4
TB4 (T Bus Bit 4)	A104-69 A105-81 A202-6	A104-69	= ADF · RB4 · SB4 · C4 + ADF · $\overline{RB4}$ · SB4 · $\overline{C4}$ + ADF · $\overline{RB4}$ · $\overline{SB4}$ · C4 + ADF · RB4 · $\overline{SB4}$ · $\overline{C4}$ + ANF · RB4 · SB4 + CMFE · $\overline{RB4}$ + EOF · RB4 · $\overline{SB4}$ + EOF · $\overline{RB4}$ · SB4 + IOF · RB4 + IOF · SB4 + RL4 · RB1 + RL4 · SB1 + RLL · RB3 + RLL · SB3 + RSM6-9 · SRA4 + SLM · RB3 + SLM · SB3 + SRM · RB5 + SRM · SB5
TB5 (T Bus Bit 5)	A104-13 A105-75 A202-5	A104-13	= ADF · RB5 · SB5 · C5 + ADF · $\overline{RB5}$ · SB5 · $\overline{C5}$ + ADF · $\overline{RB5}$ · $\overline{SB5}$ · C5 + ADF · RB5 · $\overline{SB5}$ · $\overline{C5}$ + ANF · RB5 · SB5 + CMFE · $\overline{RB5}$ + EOF · RB5 · $\overline{SB5}$ + EOF · $\overline{RB5}$ · SB5 + IOF · RB5 + IOF · SB5 + RL4 · RB2 + RL4 · SB2 + RLL · RB4 + RLL · SB4 + RSM6-9 · SRA5 + SLM · RB4 + SLM · SB4 + SRM · RB6 + SRM · SB6

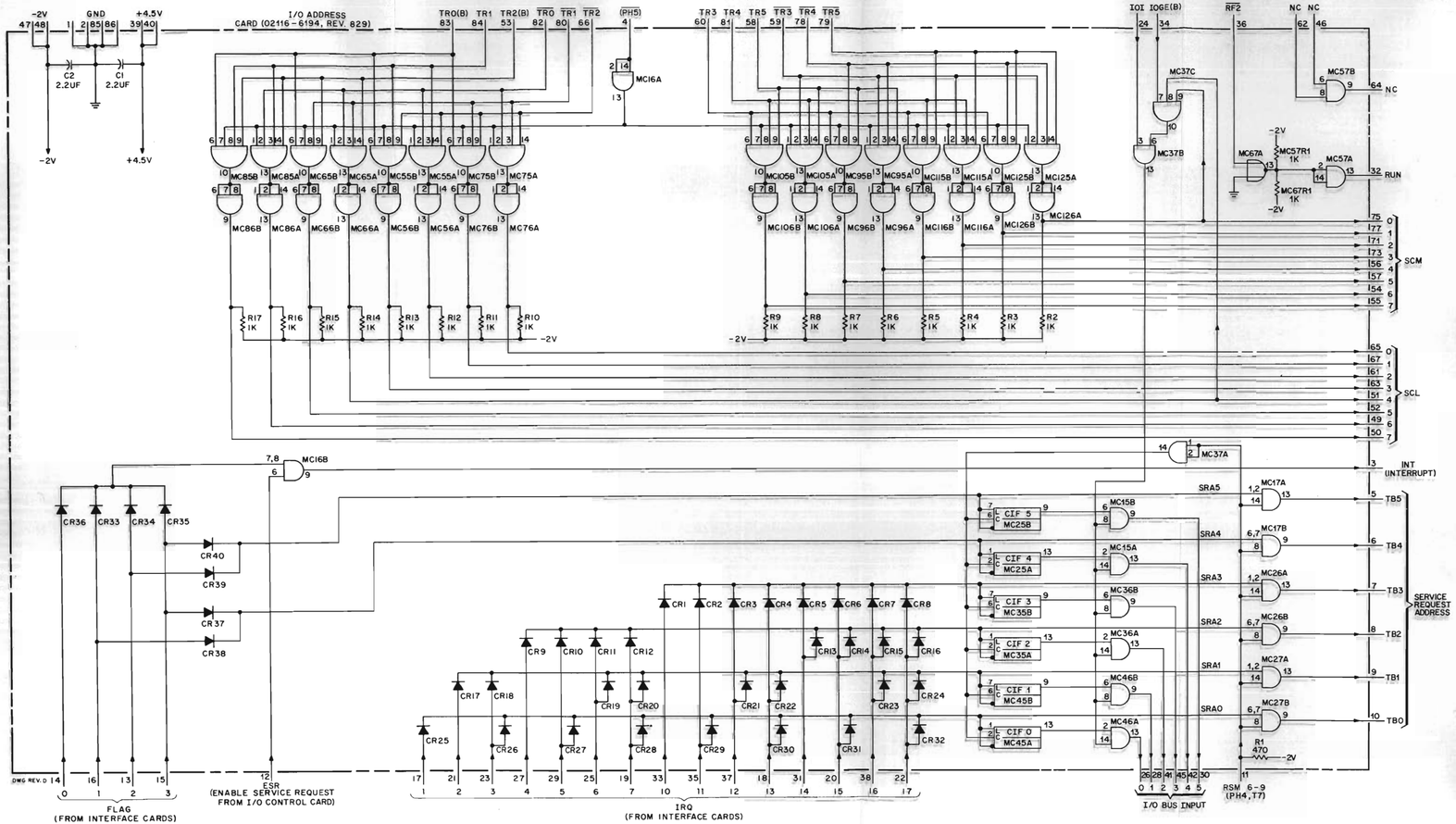
Table 7-51. A202 I/O Address Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
$\overline{TR0}$ ("not" T-Register Bit 0)	A105-54	A202-82	See source
TR0(B) (T-Register Bit 0, Buffered)	A108-4	A202-83	See source
TR1 (T-Register Bit 1)	A105-9	A202-84	See source
$\overline{TR1}$ ("not" T-Register Bit 1)	A105-10	A202-80	See source
$\overline{TR2}$ ("not" T-Register Bit 2)	A105-53	A202-66	See source
TR2(B) (T-Register Bit 2, Buffered)	A108-15	A202-53	See source
TR3 (T-Register Bit 3)	A105-16	A202-60	See source
$\overline{TR3}$ ("not" T-Register Bit 3)	A105-15	A202-59	See source
TR4 (T-Register Bit 4)	A104-58	A202-81	See source
$\overline{TR4}$ ("not" T-Register Bit 4)	A104-54	A202-78	See source
TR5 (T-Register Bit 5)	A104-9	A202-58	See source
$\overline{TR5}$ ("not" T-Register Bit 5)	A104-10	A202-79	See source

Table 7-52. A202 I/O Address Card (02116-6194), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2	0180-0155	Capacitor, Fxd, Elect, 2.2 uF, 20%, 20 VDCW	56289	150D225X0020A2-DYS
CR1 thru CR40	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088
MC15,16,17,26,27,36,46,56,57, 66,76,86,96,106,116,126	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC25,35,45	1820-0968	Integrated Circuit, CTL	07263	SL3466
MC37	1820-0953	Integrated Circuit, CTL	07263	SL3456
MC55,65,75,85,95,105,115,125	1820-0954	Integrated Circuit, CTL	07263	SL3457
MC67	1820-0952	Integrated Circuit, CTL	07263	SL3455
R1	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4W	01121	CB4715
R2 thru R17	0683-1015	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025





NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCES ARE IN OHMS.
2. PINS 8 AND 14 OF MC25, MC35, AND MC45 ARE CONNECTED TO +4.5V UNLESS OTHERWISE INDICATED ON A LOGIC DIAGRAM USING THE MICROCIRCUIT PACKAGE.

Figure 7-20. A202 I/O Address Card (02116-6194), Parts Location and Schematic Diagram

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A203-47 thru A218-47 A203-48 thru A218-48	None
+4.5V	A100E1	A203-39 thru A218-39 A203-40 thru A218-40	None
+12V	A100TB2-1	A203-43 thru A218-43 A203-44 thru A218-44	None
-12V	A100TB2-2	A203-69 thru A218-69 A203-70 thru A218-70	None
+35V	A100TB2-8	A203-36 thru A218-36	None
CLC (Clear Control)	A108-53	A203-21 thru A218-21	See source
CLF (Clear Flag)	A4-14 A108-19 A109-24	A203-7 thru A218-7	See source or option
CRS (Control Reset to I/O)	A201-65	A203-13 thru A218-13	See source
EDT (End of Data Transfer)	A4-42	A203-62 thru A218-62	See option
ENF (Enable Flag)	A201-67	A203-46 thru A218-46	See source
FLG0 (Flag from Group 0)	A203-4 thru A210-4 A203-49 thru A209-49	A1-30 A4-25 A202-14	See option

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
FLG1 (Flag from Group 1)	A210-49 thru A218-49 A211-4 thru A218-4 A219-26	A202-16	See option
GND (Ground)	A100E2	A203-1 thru A218-1 A203-2 thru A218-2 A203-85 thru A218-85 A203-86 thru A218-86	None
IAK (Interrupt Acknowledge)	A201-77	A203-10 thru A218-10	See source
IEN10 (Interrupt Enable 10)	A201-8	A203-8 thru A210-8	See source
IEN20 (Interrupt Enable 20)	A201-7	A211-8 A211-23 A212-8′ thru A218-8	See source
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · CI0 FF + IOGE · IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 ; ISR + IOGE(B) · IOI · SCM0 · SCL4 · C11 FF + IOGE · IOI · SC · DATA BIT 1

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	= DMA option signal + MP option signal + SWR2 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C12 FF + IOGE · IOI · SC · DATA BIT 2
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C13 FF + IOGE · IOI · SC · DATA BIT 3
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 ; ISR + IOGE(B) · IOI · SCM0 · SCL4 · C14 FF + IOGE · IOI · SC · DATA BIT 4
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C15FF + IOGE · IOI · SC · DATA BIT 15
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	= DMA option signal + MP option signal + SWR6 ; ISR + IOGE · IOI · SC · DATA BIT 6
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	= DMA option signal + MP option signal + SWR7 · ISR + IOGE · IOI · SC · DATA BIT 7

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	= DMA option signal + MP option signal + SWR8 · ISR + IOGE · IOI · SC · DATA BIT 8
IOBI 9 (Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	= DMA option signal + MP option signal + SWR9 · ISR + IOGE · IOI · SC · DATA BIT 9
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	= DMA option signal + MP option signal + SWR10 · ISR + IOGE · IOI · SC · DATA BIT 10
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	= DMA option signal + MP option signal + SWR11 · ISR + IOGE · IOI · SC · DATA BIT 11
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	= DMA option signal + MP option signal + SWR12 · ISR + IOGE · IOI · SC · DATA BIT 12
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	= DMA option signal + MP option signal + SWR13 · ISR + IOGE · IOI · SC · DATA BIT 13

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 14 (Input/Output Bus, Input Bit 14)	A1-73 A5-82 A16-76 A101-63 A203-82 thru A218-82 A220-80	A102-33	= DMA option signal + MP option signal + SWR14 · ISR + IOGE · IOI · SC · DATA BIT 14
IOBI 15 (Input/Output Bus, Input Bit 15)	A5-83 A15-28 A101-67 A203-83 thru A218-83 A220-82	A102-27	= DMA option signal + PE option signal + SWR15 · ISR + IOGE · IOI · SC · DATA BIT 15
IOBI 16 (Input/Output Bus, Input Bit 16)	A220-30	A203-18 thru A218-18	See option
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60	A203-35 thru A218-35	See source
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50	A203-38 thru A218-38	See source
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57	A203-41 thru A218-41	See source
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35	A203-45 thru A218-45	See source
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60	A203-42 thru A218-42	See source
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50	A203-51 thru A218-51	See source
IOBO 6 (Input/Output Bus, Output Bit 6)	A104-57	A203-53 thru A218-53	See source
IOBO 7 (Input/Output Bus, Output Bit 7)	A104-35	A203-52 thru A218-52	See source
IOBO 8 (Input/Output Bus, Output Bit 8)	A103-60	A203-54 thru A218-54	See source
IOBO 9 (Input/Output Bus, Output Bit 9)	A103-50	A203-56 thru A218-56	See source

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBO 10 (Input/Output Bus, Output Bit 10)	A103-57	A203-58 thru A218-58	See source
IOBO 11 (Input/Output Bus, Output Bit 11)	A103-35	A203-55 thru A218-55	See source
IOBO 12 (Input/Output Bus, Output Bit 12)	A102-60	A203-57 thru A218-57	See source
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-50	A203-61 thru A218-61	See source
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57	A203-65 thru A218-65	See source
IOBO 15 (Input/Output Bus, Output Bit 15)	A102-35	A203-74 thru A218-74	See source
IOBO 16 (Input/Output Bus, Output Bit 16)	A203-73 thru A218-73	A219-83	See option
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A203-15 thru A218-15	See source
IOI (Input/Output, Input)	A108-44	A203-24 thru A218-24	See source
IOO (Input/Output, Output)	A108-13	A203-20 thru A218-20	See source
IRQ1 (Interrupt Request 1)	A211-33 A212-6 A219-50	A202-17	See option
IRQ2 (Interrupt Request 2)	A212-33 A213-6 A219-52	A202-21	See option
IRQ3 (Interrupt Request 3)	A213-33 A214-6 A219-54	A202-23	See option
IRQ4 (Interrupt Request 4)	A214-33 A215-6 A219-56	A6-6 A202-27	See option
IRQ5 (Interrupt Request 5)	A16-35 A215-33 A216-6 A219-58	A15-77 A202-29	See option

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IRQ6 (Interrupt Request 6)	A216-33 A217-6 A219-60	A1-29 A4-28 A202-25	See option
IRQ7 (Interrupt Request 7)	A217-33 A218-6 A219-62	A4-26 A202-19	See option
IRQ10 (Interrupt Request 10)	A203-33 A204-6	A202-35	See option
IRQ11 (Interrupt Request 11)	A203-33 A204-6 A219-66	A202-35	See option
IRQ12 (Interrupt Request 12)	A204-33 A205-6 A219-68	A202-37	See option
IRQ13 (Interrupt Request 13)	A205-33 A206-6 A219-72	A202-18	See option
IRQ14 (Interrupt Request 14)	A206-33 A207-6 A219-74	A202-31	See option
IRQ15 (Interrupt Request 15)	A207-33 A208-6 A219-76	A202-20	See option
IRQ16 (Interrupt Request 16)	A208-33 A209-6 A219-78	A202-38	See option
IRQ17 (Interrupt Request 17)	A210-6	A202-22 A209-33 A219-80	See option
LMS (Load Memory FF, set-side output)	A101-58	A203-59 thru A218-59	See source
PON (Power On Normal)	A6-58	A203-66 thru A218-66	See source
POPIO(B) (Power On Pulse to I/O, Buffered)	A201-72	A203-17 thru A218-17	See source
PRH10/PRL7 (Priority High Select Code 10/Priority Low Select Code 7)	A4-9 A201-80	A203-23	See option
PRH11/PRL10 (Priority High Select Code 11/Priority Low Select Code 10)	A203-3	A204-23	See option

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
PRH12/PRL11 (Priority High Select Code 12/Priority Low Select Code 11)	A204-3	A205-23	See option
PRH13/PRL12 (Priority High Select Code 13/Priority Low Select Code 12)	A205-3	A206-23	See option
PRH14/PRL13 (Priority High Select Code 14/Priority Low Select Code 13)	A206-3	A207-23	See option
PRH15/PRL14 (Priority High Select Code 15/Priority Low Select Code 14)	A207-3	A208-23	See option
PRH16/PRL15 (Priority High Select Code 16/Priority Low Select Code 15)	A208-3	A209-23	See option
PRH17/PRL16 (Priority High Select Code 17/Priority Low Select Code 16)	A209-3	A210-23	See option
PRH20/PRL17 (Priority High Select Code 20/Priority Low Select Code 17)	A210-3	A201-16	See option
PRH21/PRL20 (Priority High Select Code 21/Priority Low Select Code 20)	A211-3	A212-23	See option
PRH22/PRL21 (Priority High Select Code 22/Priority Low Select Code 21)	A212-3	A213-23	See option
PRH23/PRL22 (Priority High Select Code 23, Priority Low Select Code 22)	A213-3	A214-23	See option
PRH24/PRL23 (Priority High Select Code 24/Priority Low Select Code 23)	A214-3	A215-23	See option
PRH25/PRL24 (Priority High Select Code 25/Priority Low Select Code 24)	A215-3	A216-23	See option
PRH26/PRL25 (Priority High Select Code 26/Priority Low Select Code 25)	A216-3	A217-23	See option
PRH27/PRL26 (Priority High Select Code 27/Priority Low Select Code 26)	A217-3	A218-23	See option
PRH30/PRL27 (Priority High Select Code 30/Priority Low Select Code 27)	A218-3	A220-3	See option

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
RUN (Run Signal)	A202-32	A203-50 thru A218-50	See source
SCL0 (Select Code Least Significant Digit, Octal 0)	A202-65	A203-16 A210-34 A211-16 A218-34	See source
SCL1 (Select Code Least Significant Digit, Octal 1)	A202-67	A203-34 A204-16 A211-34 A212-16	See source
SCL2 (Select Code Least Significant Digit, Octal 2)	A202-61	A204-34 A205-16 A212-34 A213-16	See source
SCL3 (Select Code Least Significant Digit, Octal 3)	A202-63	A205-34 A206-16 A213-34 A214-16	See source
SCL4 (Select Code Least Significant Digit, Octal 4)	A202-51	A206-34 A207-16 A214-34 A215-16	See source
SCL5 (Select Code Least Significant Digit, Octal 5)	A202-52	A207-34 A208-16 A215-34 A216-16	See source
SCL6 (Select Code Least Significant Digit, Octal 6)	A202-49	A208-34 A209-16 A216-34 A217-16	See source
SCL7 (Select Code Least Significant Digit, Octal 7)	A202-50	A209-34 A210-16 A217-34 A218-16	See source
SCM1 (Select Code Most Significant Digit, Octal 1)	A202-77	A203-14 thru A210-14 A203-37 thru A209-37	See source
SCM2 (Select Code Most Significant Digit, Octal 2)	A202-71	A210-37 thru A217-37 A211-14 thru A218-14	See source
SCM3 (Select Code Most Significant Digit, Octal 3)	A202-73	A218-37	See source

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

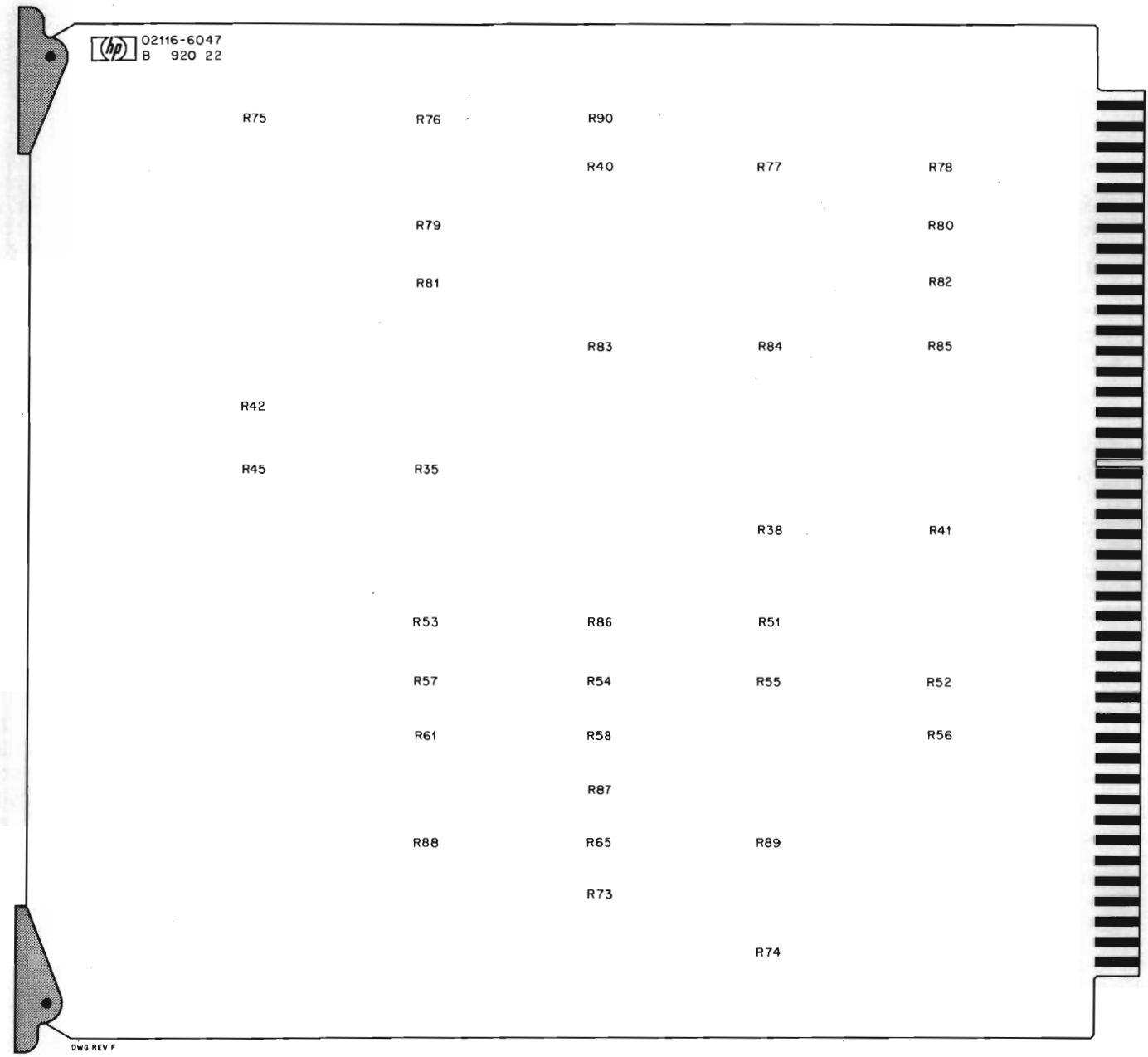
SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SIR (Service Interrupt Request)	A201-35	A203-32 thru A218-32	See source
SFC (Skip If Flag Clear)	A108-14	A203-5 thru A218-5	See source
SFS (Skip If Flag Set)	A108-54	A203-25 thru A218-25	See source
SKF (Skip On Flag)	A201-73 A203-12 thru A220-12	A1-15 A4-29 A6-12 A108-31	See source or option
SRQ10 (Service Request, Select Code 10)	A203-19	A3-22	See option
SRQ11 (Service Request, Select Code 11)	A204-19	A3-28	See option
SRQ12 (Service Request, Select Code 12)	A205-19	A3-20	See option
SRQ13 (Service Request Select Code 13)	A206-19	A3-26	See option
SRQ14 (Service Request, Select Code 14)	A207-19	A3-33	See option
SRQ15 (Service Request, Select Code 15)	A208-19	A3-44	See option
SRQ16 (Service Request, Select Code 16)	A209-19	A3-29	See option
SRQ17 (Service Request, Select Code 17)	A210-19	A3-37	See option
SRQ20 (Service Request, Select Code 20)	A211-19	A3-71	See option
SRQ21 (Service Request, Select Code 21)	A212-19	A3-66	See option
SRQ22 (Service Request, Select Code 22)	A213-19	A3-68	See option
SRQ23 (Service Request, Select Code 23)	A214-19	A3-64	See option
SRQ24 (Service Request, Select Code 24)	A215-19	A3-58	See option
SRQ25 (Service Request, Select Code 25)	A216-19	A3-54	See option

Table 7-53. A203 thru A218 I/O Interface Cards and Resistance Load Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SRQ26 (Service Request, Select Code 26)	A217-19	A3-56	See option
SRQ27 (Service Request, Select Code 27)	A218-19	A3-52	See option
STC (Set Control)	A108-56	A203-22 thru A218-22	See source
STF (Set Flag)	A108-5 A109-15	A203-9 thru A218-9	See source or option
T3(B) (Time Period 3, Buffered)	A201-81	A203-11 thru A218-11	See source

Table 7-54. A218 Resistance Load Card (02116-6047), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R35,38,40,41,43,45,R51 thru R58,61,65,73,R74 thru R90	0683-1515	Resistor, Fxd, Comp, 150 ohms, 5%, 1/4W	01121	CB1515



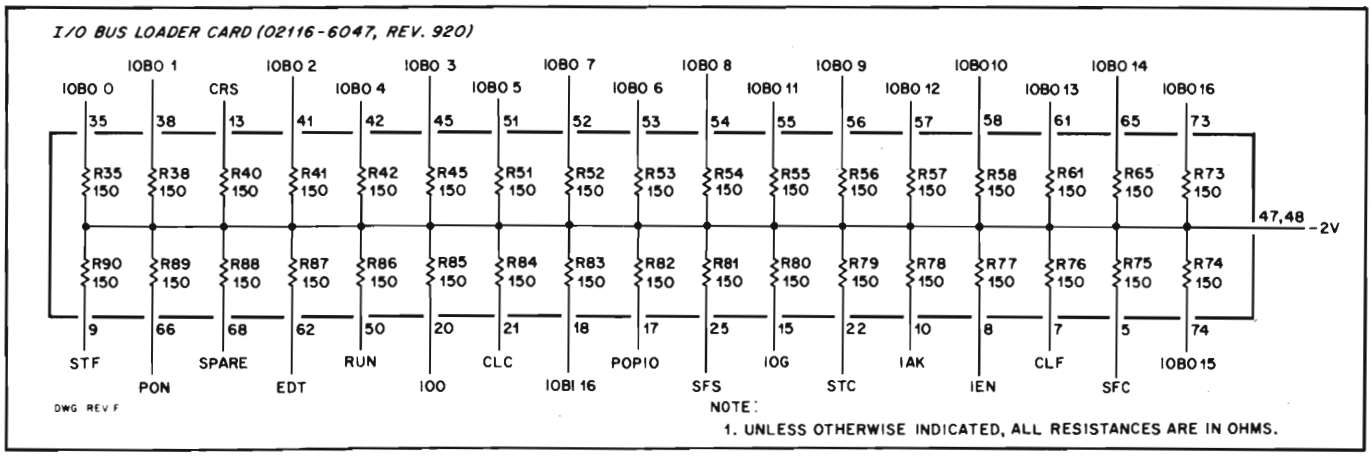


Figure 7-21. A218 Resistance Load Card, (02116-6047), Parts Location and Schematic Diagram

Table 7-55. A219 I/O-1 Extender Driver Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A219-47 A219-48	None
+4.5V	A100E1	A219-39 A219-40	None
+12V	A100TB2-1	A219-43 A219-44	None
-12V	A100TB2-2	A219-69 A219-70	None
+35V	A100TB2-8	A219-36	None
CLC (Clear Control)	A108-53	A219-21	See source
CLF (Clear Flag)	A4-14 A108-19 A109-24	A219-7	See source or option
CRS (Control Reset to I/O)	A201-65	A219-13	See source
EDT (End of Data Transfer)	A4-42	A219-3	See option
ENF (Enable Flag)	A201-67	A219-46	See source
FLG1 (Flag From Group 1)	A210-49 thru A218-49 A211-4 thru A218-4 A219-26	A202-16	See option
FLG2 (Flag From Group 2)	A219-28	A202-13	See option
FLG3 (Flag From Group 3)	A219-30	A202-15	See option
GND (Ground)	A100E2	A219-1 A219-2 A219-85 A219-86	None
IAK (Interrupt Acknowledge)	A201-77	A219-10	See source
IOBO 0 (Input/Output Bus, Output Bit 0)	A105-60	A219-49	See source
IOBO 1 (Input/Output Bus, Output Bit 1)	A105-50	A219-51	See source
IOBO 2 (Input/Output Bus, Output Bit 2)	A105-57	A219-53	See source
IOBO 3 (Input/Output Bus, Output Bit 3)	A105-35	A219-55	See source

Table 7-55. A219 I/O-1 Extender Driver Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBO 4 (Input/Output Bus, Output Bit 4)	A104-60	A219-57	See source
IOBO 5 (Input/Output Bus, Output Bit 5)	A104-50	A219-59	See source
IOBO 6 (Input/Output Bus, Output Bit 6)	A104-57	A219-61	See source
IOBO 7 (Input/Output Bus, Output Bit 7)	A104-35	A219-63	See source
IOBO 8 (Input/Output Bus, Output Bit 8)	A103-60	A219-65	See source
IOBO 9 (Input/Output Bus, Output Bit 9)	A103-50	A219-67	See source
IOBO 10 (Input/Output Bus, Output Bit 10)	A103-57	A219-71	See source
IOBO 11 (Input/Output Bus, Output Bit 11)	A103-35	A219-73	See source
IOBO 12 (Input/Output Bus, Output Bit 12)	A102-60	A219-75	See source
IOBO 13 (Input/Output Bus, Output Bit 13)	A102-50	A219-77	See source
IOBO 14 (Input/Output Bus, Output Bit 14)	A102-57	A219-79	See source
IOBO 15 (Input/Output Bus, Output Bit 15)	A102-35	A219-81	See source
IOBO 16 (Input/Output Bus, Output Bit 16)	A203-73 thru A218-73	A219-83	See option
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A219-15	See source
IOI (Input/Output, Input)	A108-44	A219-24	See source
IOO (Input/Output, Output)	A108-13	A219-20	See source
IRQ1 (Interrupt Request 1)	A211-33 A212-6 A219-50	A202-17	See option
IRQ2 (Interrupt Request 2)	A212-33 A213-6 A219-52	A202-21	See option
IRQ3 (Interrupt Request 3)	A213-33 A214-6 A219-54	A202-23	See option

Table 7-55. A219 I/O-1 Extender Driver Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IRQ4 (Interrupt Request 4)	A214-33 A215-6 A219-56	A6-6 A202-27	See option
IRQ5 (Interrupt Request 5)	A16-35 A215-33 A216-6 A219-58	A15-77 A202-29	See option
IRQ6 (Interrupt Request 6)	A216-33 A217-6 A219-60	A1-29 A4-28 A202-25	See option
IRQ7 (Interrupt Request 7)	A217-33 A218-6 A219-62	A4-26 A202-19	See option
IRQ10 (Interrupt Request 10)	A203-6 A218-33 A219-64	A202-33	See option
IRQ11 (Interrupt Request 11)	A203-33 A204-6 A219-66	A202-35	See option
IRQ12 (Interrupt Request 12)	A204-33 A205-6 A219-68	A202-37	See option
IRQ13 (Interrupt Request 13)	A205-33 A206-6 A219-72	A202-18	See option
IRQ14 (Interrupt Request 14)	A206-33 A207-6 A219-74	A202-31	See option
IRQ15 (Interrupt Request 15)	A207-33 A208-6 A219-76	A202-20	See option
IRQ16 (Interrupt Request 16)	A208-33 A209-6 A219-78	A202-38	See option
IRQ17 (Interrupt Request 17)	A210-6	A219-80	See option
PON (Power On Normal)	A6-58	A219-41	See source
POPIO(B) (Power On Pulse to I/O, Buffered)	A201-72	A219-17	See source
SFC (Skip If Flag Clear)	A108-14	A219-5	See source
SFS (Skip If Flag Set)	A108-54	A219-25	See source
SIR (Service Interrupt Request)	A201-35	A219-32	See source

Table 7-55. A219 I/O-1 Extender Driver Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SKF (Skip On Flag)	A201-73 A203-12 thru A220-12	A1-15 A4-29 A6-12 A108-31	See source or option
STC (Set Control)	A108-56	A219-22	See source
STF (Set Flag)	A108-5 A109-15	A4-16 A15-18 A201-41 A203-9 thru A220-9	See source or option
T3(B) (Time Period 3, Buffered)	A201-81	A219-11	See source

Table 7-56. A220 I/O-2 Extender Driver Card, Signal List

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTINATION	LOGIC EQUATION
-2V	A100E3	A220-47 A220-48	None
+4.5V	A100E1	A220-39 A220-40	None
+12V	A100TB2-1	A220-43 A220-44	None
-12V	A100TB2-2	A220-69 A220-70	None
+35V	A100TB2-8	A220-36	None
CLC (Clear Control)	A108-53	A220-21	See source
CLF (Clear Flag)	A4-14 A108-19 A109-24	A220-7	See source or option
CRS (Control Reset to I/O)	A201-65	A220-13	See source
ENF (Enable Flag)	A201-67	A220-46	See source
GND (Ground)	A100E2	A220-1 A220-2 A220-85 A220-86	None
IAK (Interrupt Acknowledge)	A201-77	A220-10	See source
IEN20 (Interrupt Enable 20)	A201-7	A220-4	See source
IOBI 0 (Input/Output Bus, Input Bit 0)	A1-17 A2-17 A5-26 A16-79 A101-3 A202-26 A203-26 thru A218-26 A220-50	A105-79	= DMA option signal + MP option signal + SWR0 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C10 FF + IOGE · IOI · SC · DATA BIT 0
IOBI 1 (Input/Output Bus, Input Bit 1)	A1-25 A2-25 A5-29 A16-80 A101-7 A202-28 A203-29 thru A218-29 A220-52	A105-32	= DMA option signal + MP option signal + SWR1 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C11 FF + IOGE · IOI · SC · DATA BIT 1

Table 7-56. A220 I/O-2 Extender Driver Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 2 (Input/Output Bus, Input Bit 2)	A1-28 A2-28 A5-30 A16-78 A101-11 A202-41 A203-30 thru A218-30 A220-54	A105-33	= DMA option signal + MP option signal + SWR2 · ISR + IOGE(B) · IOI ; SCM0 · SCL4 · C12 FF + IOGE · IOI · SC · DATA BIT 2
IOBI 3 (Input/Output Bus, Input Bit 3)	A1-58 A2-58 A5-64 A16-75 A101-15 A202-45 A203-64 thru A218-64 A220-56	A105-27	= DMA option signal + MP option signal + SWR3 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C13 FF + IOGE · IOI · SC · DATA BIT 3
IOBI 4 (Input/Output Bus, Input Bit 4)	A1-27 A2-77 A5-77 A16-81 A101-19 A202-42 A203-77 thru A218-77 A220-58	A104-79	= DMA option signal + MP option signal + SWR4 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C14 FF + IOGE · IOI · SC · DATA BIT 4
IOBI 5 (Input/Output Bus, Input Bit 5)	A1-80 A2-80 A5-80 A16-82 A101-23 A202-30 A203-80 thru A218-80 A220-60	A104-32	= DMA option signal + MP option signal + SWR5 · ISR + IOGE(B) · IOI · SCM0 · SCL4 · C15 FF + IOGE · IOI · SC · DATA BIT 5
IOBI 6 (Input/Output Bus, Input Bit 6)	A1-79 A2-79 A5-81 A16-84 A101-27 A203-81 thru A218-81 A220-62	A104-33	= DMA option signal + MP option signal + SWR6 · ISR + IOGE · IOI · SC · DATA BIT 6
IOBI 7 (Input/Output Bus, Input Bit 7)	A1-81 A2-81 A5-84 A16-83 A101-31 A203-84 thru A218-84 A220-64	A104-27	= DMA option signal + MP option signal + SWR7 · ISR + IOGE · IOI · SC · DATA BIT 7

Table 7-56. A220 I/O-2 Extender Driver Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 8 (Input/Output Bus, Input Bit 8)	A1-21 A2-21 A5-27 A16-64 A101-35 A203-27 thru A218-27 A220-66	A103-79	= DMA option signal + MP option signal + SWR8 · ISR + IOGE · IOI · SC · DATA BIT 8
IOBI 9(Input/Output Bus, Input Bit 9)	A1-19 A2-19 A5-28 A16-65 A101-41 A203-28 thru A218-28 A220-68	A103-32	= DMA option signal + MP option signal + SWR9 ; ISR + IOGE · IOI · SC · DATA BIT 9
IOBI 10 (Input/Output Bus, Input Bit 10)	A1-27 A2-27 A5-31 A16-67 A101-45 A203-31 thru A218-31 A220-72	A103-33	= DMA option signal + MP option signal + SWR10 · ISR + IOGE · IOI · SC · DATA BIT 10
IOBI 11 (Input/Output Bus, Input Bit 11)	A1-49 A2-49 A5-60 A16-62 A101-51 A203-60 thru A218-60 A220-74	A103-27	= DMA option signal + MP option signal + SWR11 · ISR + IOGE · IOI · SC · DATA BIT 11
IOBI 12 (Input/Output Bus, Input Bit 12)	A1-61 A2-61 A5-78 A16-70 A101-55 A203-78 thru A218-78 A220-76	A102-79	= DMA option signal + MP option signal + SWR12 · ISR + IOGE · IOI · SC · DATA BIT 12
IOBI 13 (Input/Output Bus, Input Bit 13)	A1-75 A2-75 A5-79 A16-73 A101-59 A203-79 thru A218-79 A220-78	A102-32	= DMA option signal + MP option signal + SWR13 · ISR + IOGE · IOI · SC · DATA BIT 13

Table 7-56. A220 I/O-2 Extender Driver Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
IOBI 14 (Input/Output Bus, Input Bit 14)	A1-73 A5-82 A16-76 A101-63 A203-82 thru A218-82 A220-80	A102-33	= DMA option signal + MP option signal + SWR14 · ISR + IOGE · IOI · SC · DATA BIT 14
IOBI 15 (Input/Output Bus, Input Bit 15)	A5-83 A15-28 A101-67 A203-83 thru A218-83 A220-82	A102-27	= DMA option signal + PE option signal + SWR15 · ISR + IOGE · IOI · SC · DATA BIT 15
IOBI 16 (Input/Output Bus, Input Bit 16)	A220-30	A203-18 thru A218-18	See option
IOGE(B) (Input/Output Instruction Group, I/O Buffered)	A201-37	A220-15	See source
IOI (Input/Output, Input)	A108-44	A220-24	See source
IOO (Input/Output, Output)	A108-13	A220-20	See source
POPIO(B) (Power On Pulse to I/O, Buffered)	A201-72	A220-17	See source
PRH30/PRL27 (Priority High Select Code 30/Priority Low Select Code 27)	A220-3	A218-3	See option
RUN (Run Signal)	A202-32	A220-41	See source
SCL0 (Select Code Least Significant Digit, Octal 0)	A202-65	A220-67	See source
SCL1 (Select Code Least Significant Digit, Octal 1)	A202-67	A220-71	See source
SCL2 (Select Code Least Significant Digit, Octal 2)	A202-61	A220-73	See source
SCL3 (Select Code Least Significant Digit, Octal 3)	A202-63	A220-75	See source
SCL4 (Select Code Least Significant Digit, Octal 4)	A202-51	A220-77	See source
SCL5 (Select Code Least Significant Digit, Octal 5)	A202-52	A220-79	See source

Table 7-56. A220 I/O-2 Extender Driver Card, Signal List (Continued)

SIGNAL OR FLIP-FLOP	SIGNAL SOURCE	SIGNAL DESTI-NATION	LOGIC EQUATION
SCL6 (Select Code Least Significant Digit, Octal 6)	A202-49	A220-81	See source
SCL7 (Select Code Least Significant Digit, Octal 7)	A202-50	A220-83	See source
SCM0 (Select Code Most Significant Digit, Octal 0)	A202-75	A220-55	See source
SCM3 (Select Code Most Significant Digit, Octal 3)	A202-73	A220-57	See source
SCM4 (Select Code Most Significant Digit, Octal 4)	A202-56	A220-59	See source
SCM5 (Select Code Most Significant Digit, Octal 5)	A202-57	A220-61	See source
SCM6 (Select Code Most Significant Digit, Octal 6)	A202-54	A220-63	See source
SCM7 (Select Code Most Significant Digit, Octal 7)	A202-55	A220-65	See source
SFS (Skip If Flag Clear)	A108-14	A220-5	See source
SFS (Skip If Flag Set)	A108-54	A220-25	See source
SIR (Service Interrupt Request)	A201-35	A220-32	See source
SKF (Skip on Flag)	A201-73 A203-12 thru A220-12	A1-15 A4-29 A6-12 A108-31	See source or option
STF (Set Flag)	A108-5 A109-15	A220-9	See source or option
T3(B) (Time Period 3, Buffered)	A201-81	A220-11	See source

Table 7-57. A300 Power Supply Assembly (02116-63217), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
A301	02116-6014	Logic Supply Regulator Card (see figure 7-22)	28480	02116-6014
A302 (3)	02116-63214 or 02116-63267	Memory Supply Regulator Card (see figure 7-23)	28480	02116-63214 or 02116-63267
A303	02116-63215	Capacitor Board Assembly (see figure 7-24)	28480	02116-63215
A304	02116-63237	Large Heat Sink Assembly (see figure 7-25)	28480	02116-63237
A305	02116-63238	Small Heat Sink Assembly (see figure 7-26)	28480	02116-63238
A306	02116-63229	Component Board Assembly (see figure 7-27)	28480	02116-63229
A307	02116-63242	Component Board Assembly (see figure 7-28)	28480	02116-63242
A308	02116-63235	Component Board Assembly (see figure 7-29)	28480	02116-63235
A309	02116-63240	Component Board Assembly (see figure 7-30)	28480	02116-63240
A310	02116-63241	Component Board Assembly (see figure 7-31)	28480	02116-63241
A311	02116-63225	Transformer Assembly (see figure 7-32)	28480	02116-63225
A312	02116-63228	AC Input Section (see figure 7-33)	28480	02116-63228
B1 (1)	3160-0072	Fan, Tubeaxial, 115V, 60 Hz	28480	3160-0072
B1 (2)	3160-0224	Fan Assembly, 115V, 60 Hz	28480	3160-0224
C1A, 1B	0160-3043	Capacitor, Fxd, Cer, 2x0.005 uF, 20%, 250 VDCW (see figure 7-33)	56289	29C147-CDH
J1 (1)	1251-2660	Connector, Male, 250V, 10A (see figure 7-33)	28480	1251-2660
J1 (2)	1251-0315	Connector, Male, 250V, 10A (see figure 7-33)	83315	7556-G
J2	1251-0143	Connector, Female, 14 contact (see figure 7-31)	28480	1251-0143
R1	0811-2140	Resistor, Fxd, ww, 2 ohms, 5%, 5W (see figure 7-33)	28480	0811-2140

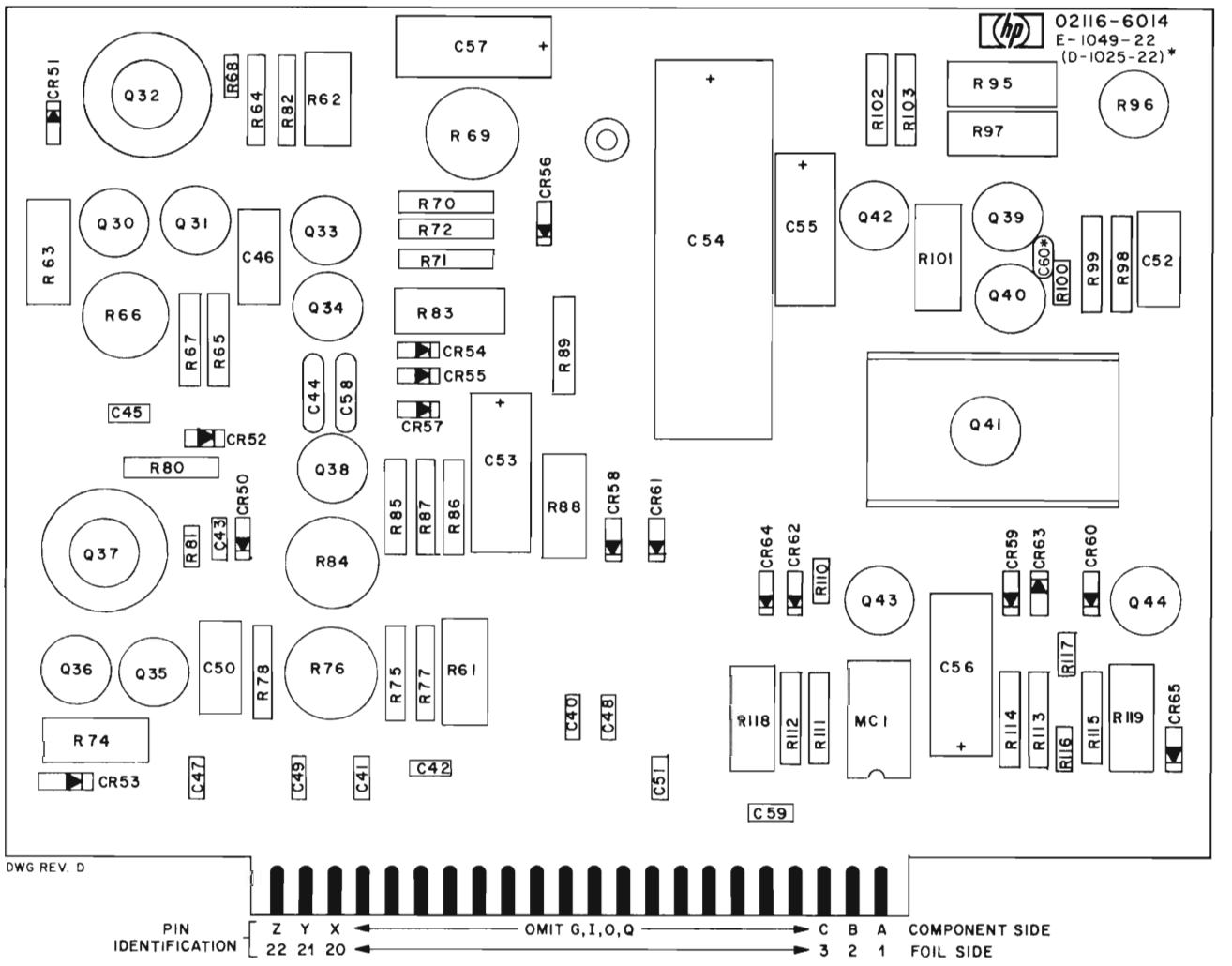
(1) For use on computers with serial number prefix below 1108A.

(2) First used on computers with serial number prefix 1108A.

(3) Memory Supply Regulator Cards with part number 02116-63267 are used on computers with serial number prefix 1127A and above. **Cards with part numbers 02116-63214 and 02116-63267 are not interchangeable.**

Table 7-58. A301 Logic Supply Regulator Card (02116-6014), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C40,41,42,43,45,48,49,59	0150-0121	Capacitor, Fxd, Cer, 0.1 uF, +80 -20%, 50 VDCW	56289	5C50BIS-CML
C44,58	0150-0050	Capacitor, Fxd, Cer, 1000 pF, +80 -20%, 1000 VDCW	56289	C067B102E102-ZE19CDH
C46,50,52	0160-0163	Capacitor, Fxd, My, 0.033 uF, 10%, 200 VDCW	56289	192P33392-PTS
C53,55,57	0180-0064	Capacitor, Fxd, Elect, 35 uF, -10 +100%, 6 VDCW	56289	30D156G006BB4
C54	0180-1867	Capacitor, Fxd, Elect, 1600 uF, +75 -10%, 10 VDCW	28480	0180-1867
C56	0180-1714	Capacitor, Fxd, Elect, 330 uF, 10%, 6 VDCW	28480	0180-1714
C60	0160-0153	Capacitor, Fxd, My, 0.001 uF, 10%, 200 VDCW	56289	192P10292-PTS
CR50	1902-0071	Diode, Breakdown, 9.0V, 5%	28480	1902-0071
CR51,53,54,55,56,57,59,61, 62,63	1901-0025	Diode, Silicon, 100 mA, 1V	07263	FD2387
CR52	1902-0556	Diode, Breakdown, 20.0V, 5%, 1W	28480	1902-0556
CR58	1902-3079	Diode, Breakdown, 4.53V, 5%	04713	SZ10939-83
CR60	1902-0184	Diode, Breakdown, Si, 16.2V, 5%	28480	1902-0184
CR64	1902-3224	Diode, Breakdown, 17.8V, 5%, 400 mW	28480	1902-3224
CR65	1902-0017	Diode, Breakdown, 6.81, 10%	04713	SZ10939-133
MC1	1820-0954	Integrated Circuit, CTL	07263	SL3457
Q30,31,32,35,36,37	1853-0001	Transistor, Si, PNP	28480	1853-0001
Q33,34,38,43	1850-0062	Transistor, Ge, Alloy Junction	01295	GA287
Q39,40	1854-0003	Transistor, Si, NPN	28480	1854-0003
Q41	1854-0265	Transistor, Si, NPN	28480	1854-0265
Q42,44	1851-0017	Transistor, Ge, NPN	01295	2N1304
R61	0757-0808	Resistor, Fxd, Flm, 301 ohms, 1%, 1/4W	28480	0757-0808
R62	0761-0008	Resistor, Fxd, Met Ox, 510 ohms, 5%, 1W	28480	0761-0008
R63,74	0751-0821	Resistor, Fxd, Flm, 1.21k, 1%, 1/2W	28480	0757-0821
R64,78,98	0757-0730	Resistor, Fxd, Flm, 750 ohms, 1%, 1/4W	28480	0757-0730
R65,67	0757-0071	Resistor, Fxd, Flm, 247.5 ohms, 1%, 1/4W	28480	0757-0071
R66,76,96	2100-1770	Resistor, Var, ww, 100 ohms, 5%	28480	2100-1770
R68,81,100	0757-0924	Resistor, Fxd, Flm, 1k, 2%, 1/8W	28480	0757-0924
R69,84	2100-1772	Resistor, Var, ww, 500 ohms, 5%	28480	2100-1772
R70	0757-0728	Resistor, Fxd, Flm, 619 ohms, 1%, 1/4W	28480	0757-0728
R71,86	0757-0715	Resistor, Fxd, Flm, 150 ohms, 1%, 1/4W	28480	0757-0715
R72,87,119	0757-0244	Resistor, Fxd, Flm, 499 ohms, 1%, 1/4W	28480	0757-0244
R75,102	0757-0711	Resistor, Fxd, Flm, 82.5 ohms, 1%, 1/4W	28480	0757-0711
R77	0757-0727	Resistor, Fxd, Flm, 562 ohms, 1%, 1/4W	28480	0757-0727
R82,90,99	0757-0743	Resistor, Fxd, Flm, 3.32k, 1%, 1/4W	28480	0757-0743
R83	0757-0198	Resistor, Fxd, Flm, 100 ohms, 1%, 1/2W	28480	0757-0198
R85	0757-0732	Resistor, Fxd, Flm, 909 ohms, 1%, 1/4W	28480	0757-0732
R88	0761-0026	Resistor, Fxd, Met Ox, 220 ohms, 5%, 1W	28480	0761-0026
R89	0757-0739	Resistor, Fxd, Flm, 2.00k, 1%, 1/4W	28480	0757-0739
R95	0757-0814	Resistor, Fxd, Flm, 511 ohms, 1%, 1/2W	28480	0757-0814
R97	0757-0158	Resistor, Fxd, Flm, 619 ohms, 1%, 1/2W	28480	0757-0158
R101	0761-0011	Resistor, Fxd, Met Ox, 3300 ohms, 5%, 1W	28480	0761-0011
R103	0698-3134	Resistor, Fxd, Flm, 1.33k, 1%, 1/4W	28480	0698-3134
R110	0757-0912	Resistor, Fxd, Flm, 330, 2%, 1/8W	28480	0757-0912
R111,113	0757-0338	Resistor, Fxd, Flm, 1.00k, 1%, 1/4W	28480	0757-0338
R112	0757-0759	Resistor, Fxd, Flm, 18.2k, 1%, 1/4W	28480	0757-0759
R114	0757-0705	Resistor, Fxd, Flm, 47.5 ohms, 1%, 1/4W	28480	0757-0705
R115	0757-0340	Resistor, Fxd, Flm, 10.0k, 1%, 1/4W	28480	0757-0340
R116	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R117	0683-5115	Resistor, Fxd, Comp, 510 ohms, 5%, 1/4W	01121	CB5115
R118	0757-0197	Resistor, Fxd, Flm, 1500 ohms, 1%, 1/2W	28480	0757-0197



PIN	TO/FROM
A	– –
B	XA301-2, XA302-T
C	– –
D	A307R40
E	-2V Bus
F	A100TB2-7, XA302-13
H	A307R47
J	A307R45
K	A303C10(-)
L	Ground Bus
M	– –
N	A303C15(+)
P	A303C15(+)
R	-2V Bus
S	A303C23(-)
T	– –
U	– –
V	– –
W	– –
X	A308R19
Y	Ground Bus
Z	A303C19(-)

PIN	TO/FROM
1	– –
2	A303C9(+)
3	XA302-19
4	– –
5	XA301-E
6	– –
7	A303C11(-)
8	Ground Bus
9	A306R16
10	XA301-L
11	A100TB1-1
12	XA301-N
13	A310-R11
14	A310R11
15	A310R15
16	– –
17	– –
18	– –
19	– –
20	XA301-X
21	A307R46
22	A307R45

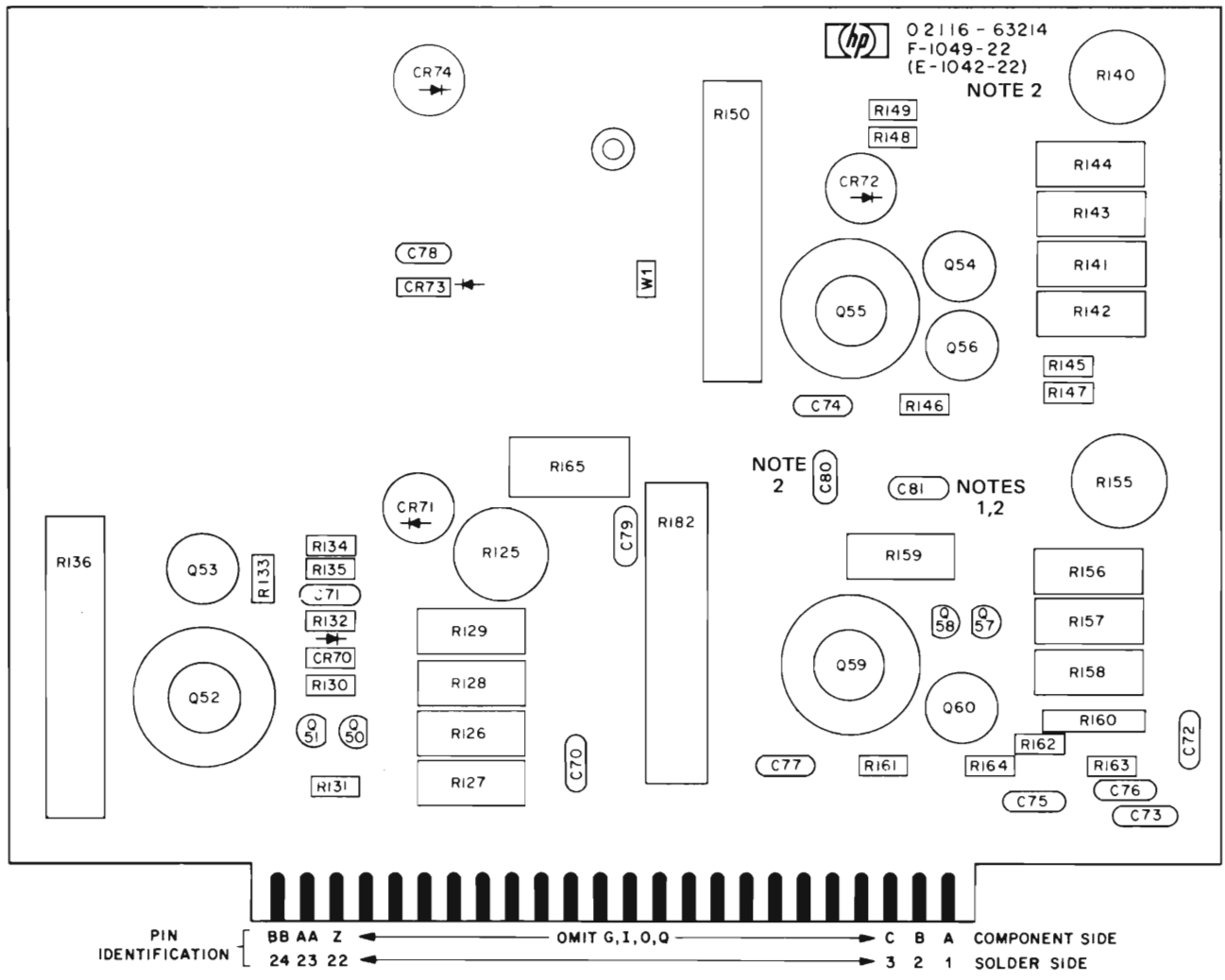
*Capacitor C60 first used on card revision E-1049-22.

Figure 7-22. A301 Logic Supply Regulator Card (02116-6014), Parts Location and Connection Diagram

Table 7-59. A302 Memory Supply Regulator Card (02116-63214 or 02116-63267), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C70 thru C78	0150-0121	Capacitor, Fxd, Cer, 0.1 uF, +80-20%, 50 VDCW	56289	5C50BIS-CML
C79	0160-0174	Capacitor, Fxd, Cer, 0.47 uF, +80-20%, 25 VDCW	56289	5C1187S-CML
C80 ①	0150-0093	Capacitor, Fxd, Cer, 0.01 uF, +80-20%, 100 VDCW	28480	0150-0093
C81 ①	0160-0153	Capacitor, Fxd, My, 0.001 uF, 10%, 200 VDCW	56289	192P10292-PTS
CR70	1902-0071	Diode, Breakdown, 9.0V, 5%	28480	1902-0071
CR71,72,74	1902-0379	Diode, Breakdown, 20V, 10%, 1.5W	28480	1902-0379
CR73	1902-3182	Diode, Breakdown, Si, 12.1V, 5%	28480	1902-3182
Q50,51,57,58	1853-0036	Transistor, Si, PNP	28480	1853-0036
Q52,59	1853-0041	Transistor, Si, PNP	02735	38640
Q53,60	1850-0062	Transistor, Ge, Alloy Junction	01295	GA287
Q54	1854-0221	Transistor, Si, NPN	28480	1854-0221
Q55	1854-0022	Transistor, Si, NPN	07263	S17843
Q56	1851-0071	Transistor, Ge, NPN	01295	2N1304
R125	2100-0755	Resistor, Var, ww, 1k, 5%	28480	2100-0755
R126	0811-2033	Resistor, Fxd, ww, 1100 ohms, 1%, 1/4W	28480	0811-2033
R127	0811-2032	Resistor, Fxd, ww, 880 ohms, 1%, 1/4W	28480	0811-2032
R128	0811-2036	Resistor, Fxd, ww, 1800 ohms, 1%, 1/4W	28480	0811-2036
R129	0757-0834	Resistor, Fxd, Flm, 5.62k, 2%, 1/2W	28480	0757-0834
R130	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R131	0757-0914	Resistor, Fxd, Flm, 390 ohms, 2%, 1/8W	28480	0757-0914
R132,146,161	0757-0924	Resistor, Fxd, Flm, 1k, 2%, 1/8W	28480	0757-0924
R133,147,162	0757-0900	Resistor, Fxd, Flm, 100 ohms, 2%, 1/8W	28480	0757-0900
R134	0757-0910	Resistor, Fxd, Flm, 270 ohms, 2%, 1/8W	28480	0757-0910
R135	0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154
R136	0770-0003	Resistor, Fxd, Flm, 3300 ohms, 5%, 4W	28480	0770-0003
R140,155	2100-1429	Resistor, Var, ww, 2000 ohms, 5%, 1W	28480	2100-1429
R141	0757-0839	Resistor, Fxd, Flm, 10k, 1%, 1/2W	28480	0757-0839
R142	0698-3411	Resistor, Fxd, Flm, 3.48k, 1%, 1/2W	28480	0698-3411
R143	0757-0159	Resistor, Fxd, Flm, 1k, 1%, 1/2W	28480	0157-0159
R144	0757-0196	Resistor, Fxd, Flm, 6.19k, 1%, 1/2W	28480	0757-0196
R145	0757-0931	Resistor, Fxd, Flm, 2k, 2%, 1/8W	28480	0757-0931
R148	0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W	28480	0757-0417
R149,163	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442
R150,182	0770-0002	Resistor, Fxd, Met Ox, 2400 ohms, 5%, 4W	28480	0770-0002
R156	0811-2039	Resistor, Fxd, ww, 8000 ohms, 1%, 1/4W	28480	0811-2039
R157	0811-2098	Resistor, Fxd, ww, 2.75k, 1%, 1/4W	28480	0811-2098
R158	0811-2037	Resistor, Fxd, ww, 2400 ohms, 1%, 1/4W	28480	0811-2037
R159	0698-3411	Resistor, Fxd, Flm, 3.48k, 1%, 1/2W	28480	0698-3411
R160	0757-0744	Resistor, Fxd, Flm, 3920 ohms, 1%, 1/4W	28480	0757-0744
R164	0757-0920	Resistor, Fxd, Flm, 680 ohms, 2%, 1/8W	28480	0757-0920
R165	0764-0063	Resistor, Fxd, Flm, 620 ohms, 5%, 2W	28480	0764-0063

① For computers with serial number prefix 1127A and above, the Memory Supply Regulator Card part number is changed to 02116-63267 and capacitors C80 and C81 are deleted.



PIN	TO/FROM
A	A308R19
B	A303C11(-)
C	– –
D	XA302-B
E	A306R54
F	A303C23(-)
H	A308R19
J	A306R52
K	– –
L	– –
M	A303E12
N	Ground Bus
P	– –
R	A303C10(-)
S	– –
T	XA301-2
U	– –
V	– –
W	A307R22
X	– –
Y	– –
Z	A307R40
AA	XA302-R
BB	A303E8

PIN	TO/FROM
1	A100TB2-6
2	A303C13(+)
3	– –
4	X302-2
5	A307R51
6	XA302-F
7	XA302-H
8	– –
9	– –
10	A306R50
11	XA302-M
12	XA302-N
13	XA301-F
14	– –
15	– –
16	– –
17	– –
18	– –
19	XA301-3
20	– –
21	– –
22	XA302-Z
23	A306R49
24	XA302-BB

NOTES:

1. CAPACITOR C81 FIRST USED ON CARD REVISION E-1049-22.
2. FOR COMPUTERS WITH SERIAL NUMBER PREFIX 1127A AND ABOVE, USE PART NUMBER 02116-63267 WITH CARD REVISION F-1127-22, AND DELETE CAPACITORS C80 AND C81.

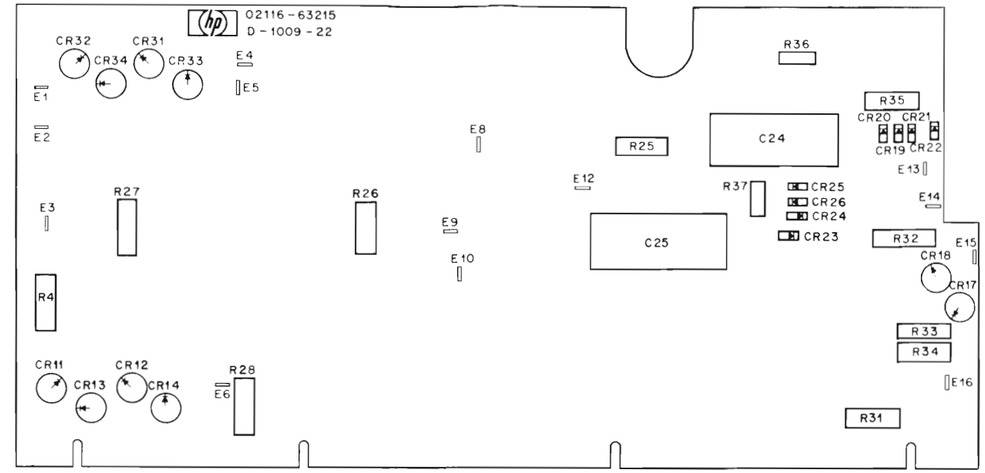
Figure 7-23. A302 Memory Supply Regulator Card (02116-63214 or 02116-63267), Parts Location and Connection Diagram

Table 7-60. A303 Capacitor Board Assembly (02116-63236), Reference Designation Index

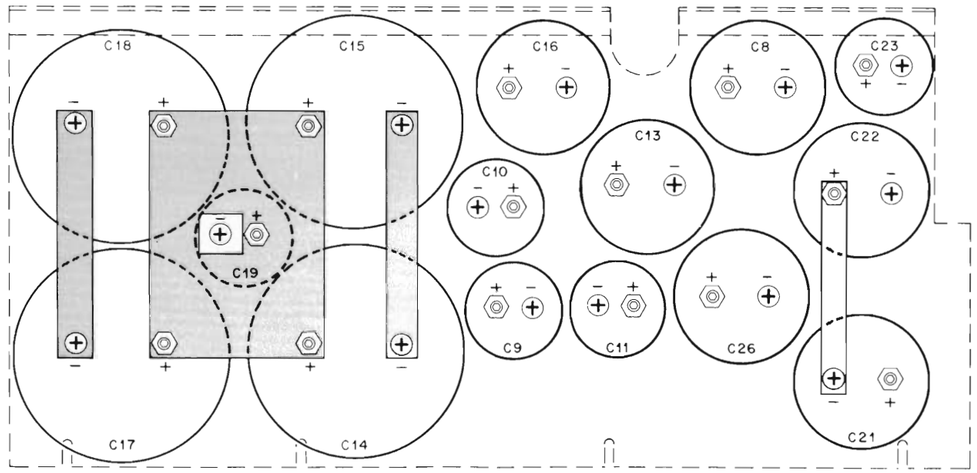
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C8,16	0180-1874	Capacitor, Fxd, Elect, 51,000 uF, +75 -10%, 7.5 VDCW	28480	0180-1874
C9,10	0180-1870	Capacitor, Fxd, Elect, 10,000 uF, +75 -10%, 20 VDCW	28480	0180-1870
C11	0180-1868	Capacitor, Fxd, Elect, 4900 uF, +75 -10%, 40 VDCW	28480	0180-1868
C13	0180-1869	Capacitor, Fxd, Elect, 8700 uF, +75 -10%, 50 VDCW	28480	0180-1869
C14,15,17,18	0180-1875	Capacitor, Fxd, Elect, 100,000 uF, +75 -10%, 20 VDCW	28480	0180-1875
C19	0180-1871	Capacitor, Fxd, Elect, 12,000 uF, +75 -10%, 25 VDCW	28480	0180-1871
C23	0180-1977	Capacitor, Fxd, Elect, 5900 uF, +75 -10%, 50 VDCW	28480	0180-1977
C21,22	0180-1873	Capacitor, Fxd, Elect, 21,000 uF, +75 -10%, 30 VDCW	28480	0180-1873
C24,25	0180-1866	Capacitor, Fxd, Elect, 500 uF, +75 -10%, 75 VDCW	56289	39D507G075HL4-DSB
C26	0180-1978	Capacitor, Fxd, Elect, 8800 uF, +50 -10%, 75 VDCW	28480	0180-1978
CR11 thru CR14,17,18,CR31 thru CR34	1901-0416	Diode, Si, 200 PIV, 3A	28480	1901-0416
CR19 thru CR26	1901-0191	Diode, Si, 0.75A, 100 PIV	04713	SR1358-2
R4,33,34	0813-0038	Resistor, Fxd, ww, 0.5 ohm, 3%, 3W	28480	0813-0038
R25	0764-0017	Resistor, Fxd, Met Ox, 1.6k, 5%, 2W	28480	0764-0017
R26,27	0811-2138	Resistor, Fxd, ww, 120 ohms, 5%, 3W	28480	0811-2138
R28	0811-1858	Resistor, Fxd, ww, 500 ohms, 5%, 5W	28480	0811-1858
R35	0812-0099	Resistor, Fxd, ww, 1k, 5%, 5W	28480	0812-0099
R31,32	0811-1857	Resistor, Fxd, ww, 400 ohms, 5%, 5W	28480	0811-1857
R36,37	0686-1235	Resistor, Fxd, Comp, 12k, 5%, 1/2W	01121	EB1235
R38	0812-0050	Resistor, Fxd, ww, 3k, 5%, 5W	28480	0812-0050

NOTE: Capacitors C8 thru C23, and C26 are not part of Capacitor Board Assembly A303, and must be ordered separately. They are listed here for convenience only.

A303 CONNECTION	DESTINATION
C8(–)	–2V bus bar
C9(+)	XA301-2, A306R16, A100TB2-1
C10(–)	A000R220, A100TB2-2, XA301-K, XA302-R, A307R48
C11(–)	A100TB2-4, XA301-7, XA302B, A306R52
C13(+)	A100TB2-3, XA302-2, A306R50
C13(–)	A300J2-6, A308CR9, ground bus bar
C14(+)	+4.5V bus bar
C14(–)	A304-E1
C15(+)	XA301-N, XA301-P, A310R23
C15(–)	A309CR1
C17(+)	A311TB7-20
C17(–)	A100TB1-5, A304-E2, A312K1
C18(–)	A309CR3
C19(–)	XA301-Z, XA304-1
C21(+)	A307R46, A308R5, A308R17
C22(+)	A311TB4-2
C22(–)	XA305-4, A307R51, A308R6
C23(–)	XA301-S, XA302F, XA305-2
C26(+)	A100TB2-8, XA305-1, A306R39, A308R19, A308R7
E1	A311TB6-5
E2	A311TB2-3
E3	A311TB2-4
E4	A100TB1-7
E5	A100TB1-6
E6	A311TB4-1
E8	XA302-BB
E9	A311TB2-5
E10	A311TB1-6
E12	XA302-M
E13	A311TB1-7
E14	A311TB2-1
E15	A311TB6-4
E16	A311TB6-1



TOP VIEW



PHANTOM VIEW

NOTES:

1. CAPACITORS ARE BENEATH THE PRINTED CIRCUIT BOARD WITH THE EXCEPTION OF C24 AND C25.
2. METAL BARS (SHADED AREAS) ARE ON THE COMPONENT SIDE OF THE PRINTED CIRCUIT BOARD.
3. THE CATHODE OF ALL DIODES IS THE OUTER CASE OF THE DIODE. A BEAD IS INSTALLED ON THE CATHODE LEAD.
4. REFERENCE DESIGNATION PREFIX IS A303.

2107-30A

Figure 7-24. A303 Capacitor Board Assembly (02116-63236), Parts Location and Connection Diagram

Table 7-61. A304 Large Heat Sink Assembly (02116-63237), Reference Designation Index

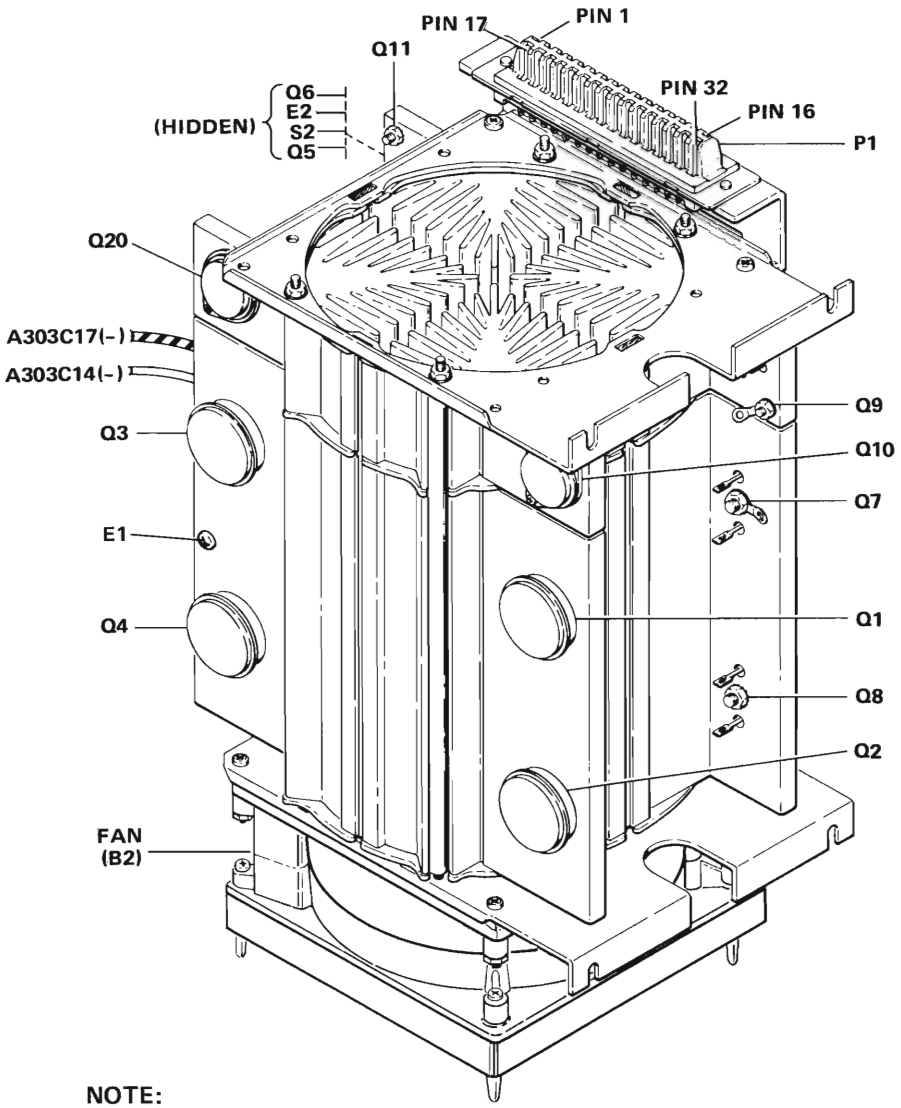
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
B2①	3160-0072	Fan, Tubeaxial, 115V, 60 Hz	28480	3160-0072
B2②	3160-0224	Fan Assembly, 115V, 60 Hz	28480	3160-0224
P1	1251-0136	Connector, 32 Pin, Male	02660	26-4100-32P
Q1 thru Q8	1850-0198	Transistor, Ge, PNP	04713	2N2156
Q9,20	1854-0264	Transistor, Si, NPN	04713	2N3715
Q10,11	1850-0098	Transistor, Ge, PNP	28480	1850-0098
S2	3103-0004	Thermal Switch, 115V, 2A	28480	3103-0004
XA304	1251-0137	Connector, 32 Contact, Female	02660	26-4200-32S

① Used on computers with serial number prefix below 1108A.

② First used on computers with serial number prefix 1108A.

A304 CONNECTIONS

PIN	TO/FROM
1	A303C19(-)
2	A308R17
3	A307R45
4	A308R17
5	A310R8
6	XA304-5
7	A310R9
8	XA304-7
9	A310R10
10	XA304-9
11	A310R11
12	XA304-11
13	A307R46
14	A308R18
15	A310R12
16	XA304-15
17	A310R13
18	XA304-17
19	A310R14
20	XA304-19
21	A310R15
22	XA304-21
23	A307R47
24	A306R16
25	– –
26	A311TB1-1
27	A311TB1-3
28	XA305-20
29	A100TB1-2
30	A306R21
31	– –
32	– –



NOTE:

REFERENCE DESIGNATION PREFIX IS A304

2107-31B

Figure 7-25. A304 Large Heat Sink Assembly (02116-63237), Parts Location and Connection Diagram

Table 7-62. A305 Small Heat Sink Assembly (02116-63238), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
B3 ①	3160-0072	Fan Tubeaxial, 115V, 60 Hz	28480	3160-0072
B3 ②	3160-0224	Fan Assembly, 115V, 60 Hz	28480	3160-0224
C1 ③	0160-0161	Capacitor, Fxd, My, 0.01 uF, 10%, 20 VDCW	56289	192P10392-PTS
P1	1251-0136	Connector, 32 Pin, Male	02660	26-4100-32P
Q12,15,21	1853-0063	Transistor, Si, PNP	04713	MJ2268
Q13	1850-0098	Transistor, Ge, PNP	28480	1850-0098
Q14,16,17	1854-0264	Transistor, Si, NPN	04713	2N3715
S1	3103-0004	Thermal Switch, 115V, 2A	28480	3103-0004
XA305	1251-0137	Connector, 32 Contact, Female	02660	26-4200-32S

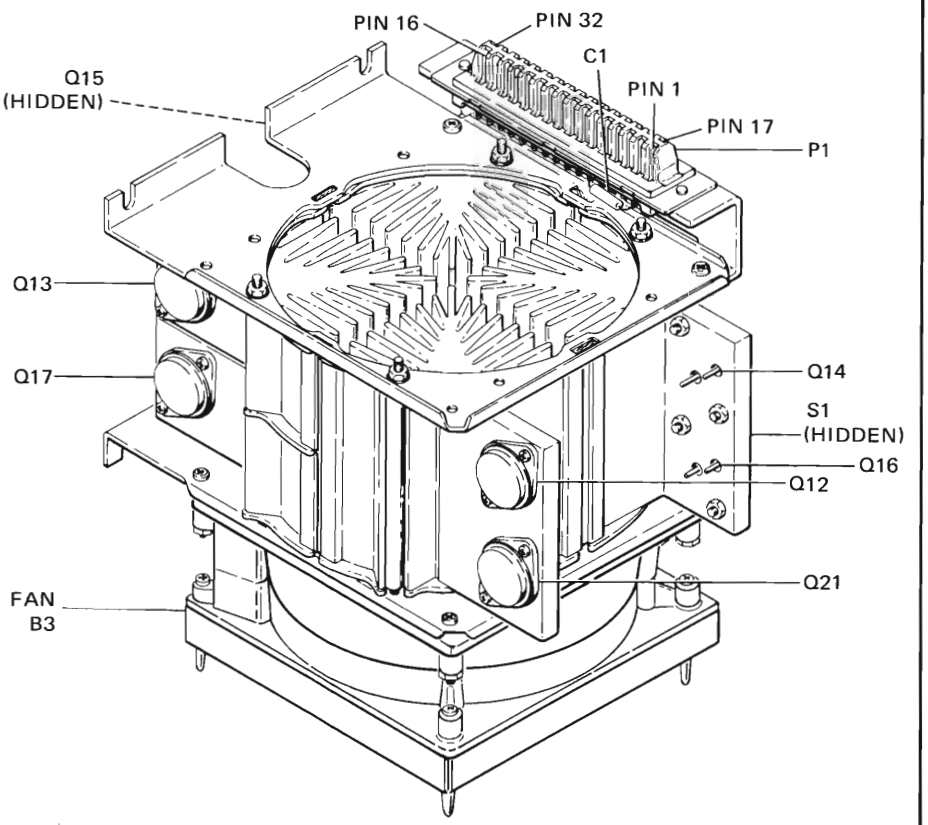
① Used on computers with serial number prefix below 1108A.

② First used on computers with serial number prefix 1108A.

③ First used on computers with serial number prefix 1127A.

A305 CONNECTIONS

PIN	TO/FROM
1	A303C26(+)
2	A303C23(-)
3	A306R53
4	A303C22(-)
5	A307R51
6	A306R50
7	A306R54
8	– –
9	– –
10	A306R52
11	A306R40
12	A307R22
13	– –
14	A306R49
15	A306R39
16	A307R48
17	A311TB1-2
18	A311TB1-4
19	A307 Jumper A
20	XA304-28
21	– –
22	– –
23	– –
24	– –
25	– –
26	– –
27	– –
28	– –
29	– –
30	– –
31	– –
32	– –



NOTE:
REFERENCE DESIGNATION PREFIX IS A305

2107-32B

Figure 7-26. A305 Small Heat Sink Assembly (02116-63238), Parts Location and Connection Diagram

Table 7-63. A306 Component Board Assembly (02116-63229), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R16,21	0811-2097	Resistor, Fxd, ww, 0.25 ohms, 3%, 5W	28480	0811-2097
R39,49,54	0811-2139	Resistor, Fxd, ww, 2.2k, 5%, 3W	28480	0811-2139
R50,53	0812-0014	Resistor, Fxd, ww, 0.5 ohms, 3%, 5W	28480	0812-0014
R52	0812-0046	Resistor, Fxd, ww, 2.0 ohms, 5%, 5W	28480	0812-0046

Table 7-64. A307 Component Board Assembly (02116-63242), Reference Desgination Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R22,48	0811-2097	Resistor, Fxd, ww, 0.25 ohms, 3%, 5W	28480	0811-2097
R40	0811-1339	Resistor, Fxd, ww, 500 ohms, 5%, 5W	28480	0811-1339
R45,46	0761-0058	Resistor, Fxd, Met Ox, 750 ohms, 5%, 1W	28480	0761-0058
R47	0811-1858	Resistor, Fxd, ww, 500 ohms, 5%, 5W	28480	0811-1858
R51	0761-0003	Resistor, Fxd, Met Ox, 62 ohms, 5%, 1W	28480	0761-0003
W1	No Number	Bus Wire, No. 18	00000	OBD

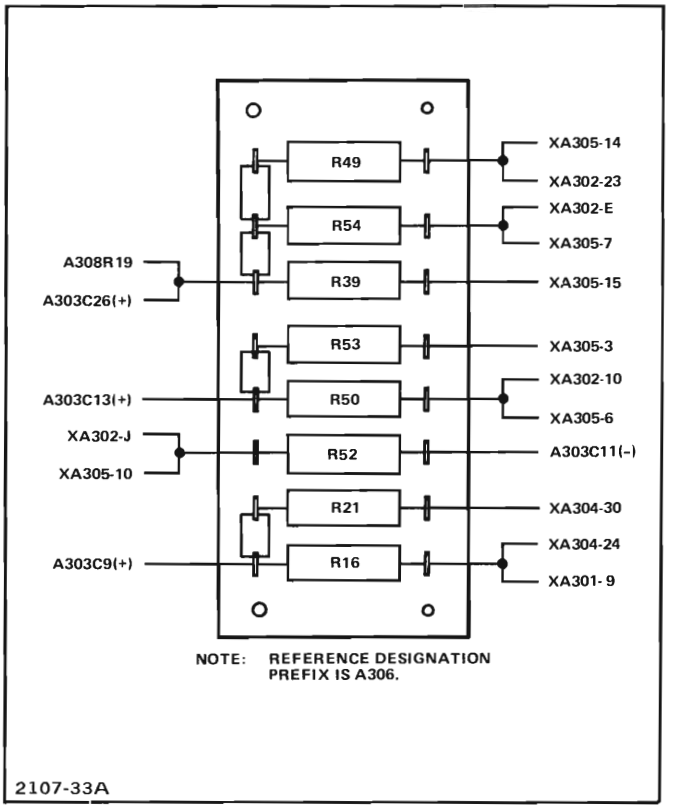


Figure 7-27. A306 Component Board Assembly (02116-63229), Parts Location and Connection Diagram

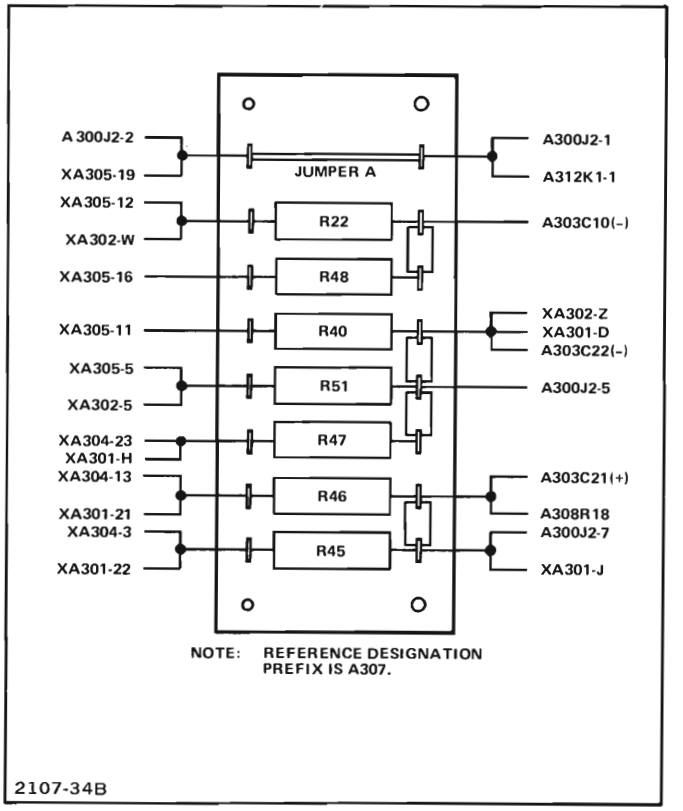
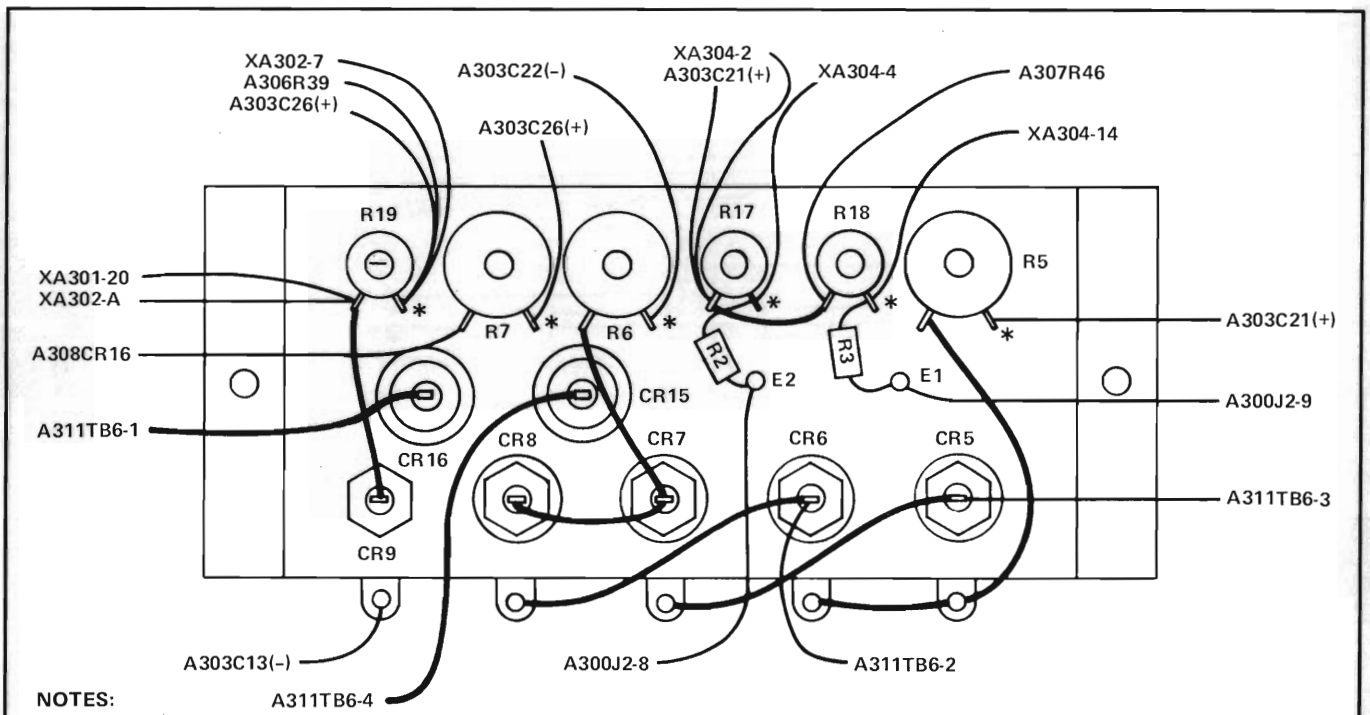


Figure 7-28. A307 Component Board Assembly (02116-63242), Parts Location and Connection Diagram

Table 7-65. A308 Component Board Assembly (02116-63235), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
CR5 thru CR8,15,16	1901-0496	Diode, Si, 100 PIV, 12A	04713	MR1121
CR9	1902-1215	Diode, Breakdown, 20.0V, 2%, 10W	04713	1N2984
R2,R3	0757-0159	Resistor, Fxd, Met Ox, 1k, 1%, 1/2W	28480	0757-0159
R5,6	0811-2510	Resistor, Fxd, ww, 0.1 ohm, 5%, 25W	28480	0811-2510
R7	0811-2079	Resistor, Fxd, ww, 0.25 ohms, 10%, 25W	28480	0811-2079
R17,18	0811-2107	Resistor, Fxd, ww, 75 ohms, 5%, 10W	28480	0811-2107
R19	0815-0005	Resistor, Fxd, ww, 62 ohms, 5%, 10W	28480	0815-0005



NOTES:

1. * INDICATES ATTACHMENT TO OUTER LUG OF RESISTOR.
2. FRAME GROUND FOR THE ENTIRE POWER SUPPLY IS MADE AT DIODE CR9.
3. DIODES CR5, CR6, CR7, CR8, CR15, AND CR16 ARE INSULATED FROM THE MOUNTING BRACKET BY MICA WASHERS AND TEFLON INSULATORS.
4. DIODE MOUNTING NUTS ARE TIGHTENED WITH A MAXIMUM TORQUE OF 12 POUND-INCHES.
5. WHEN DIODES CR5, CR6, CR7, CR8, CR9, CR15, AND CR16 ARE INSTALLED USED HEAT-CONDUCTING COMPOUND.
6. REFERENCE DESIGNATION PREFIX IS A308.

2107-38D

Figure 7-29. A308 Component Board Assembly (02116-63235), Parts Location and Connection Diagram

Table 7-66. A309 Component Board Assembly (02116-63240), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C4 thru C7	0150-0093	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW	28480	0150-0093
CR1 thru CR4	1901-0344	Diode, Si	04713	SR2014
F11 thru F14	2110-0256	Fuse, 30A, 32V, medium blow	00000	OBD

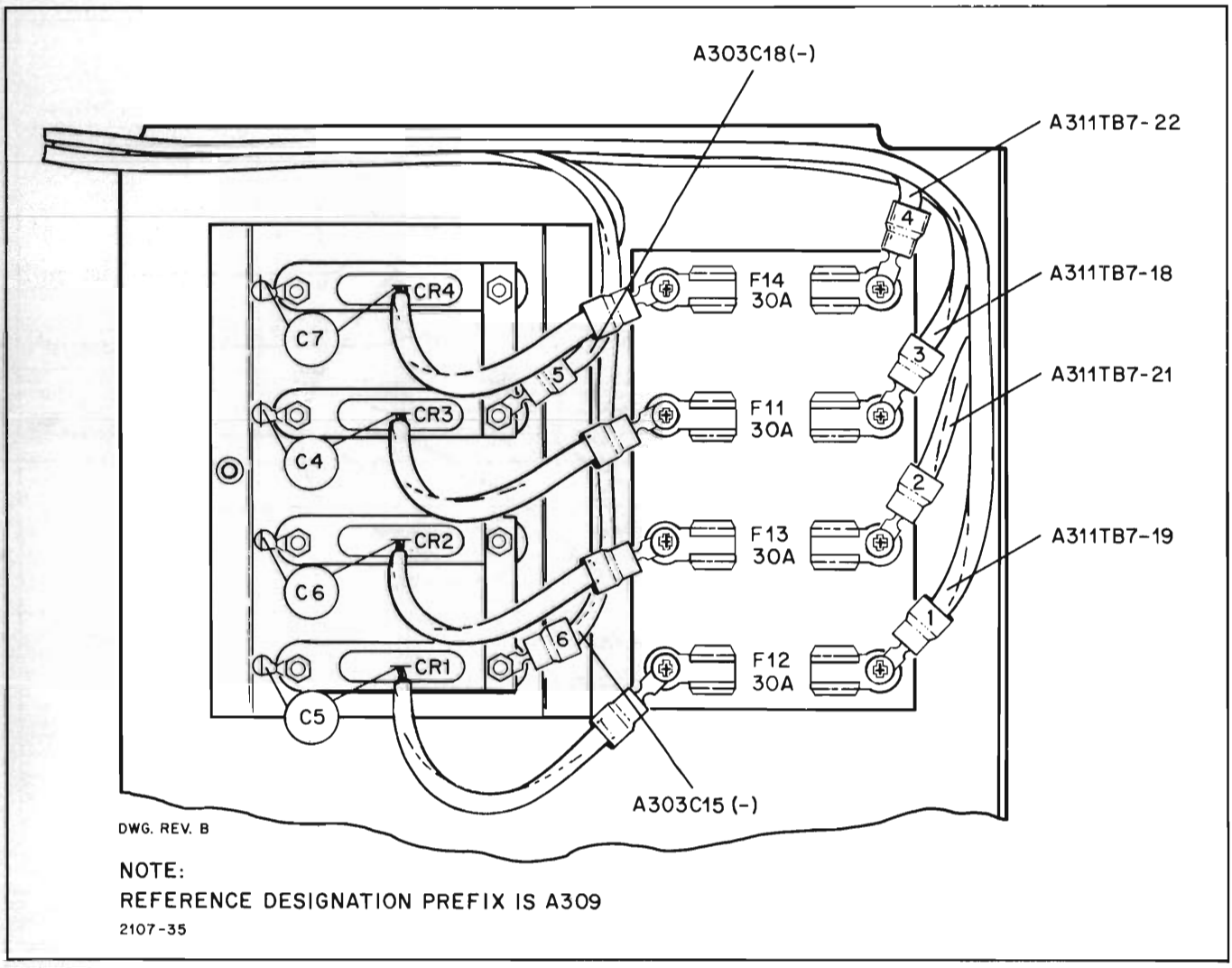
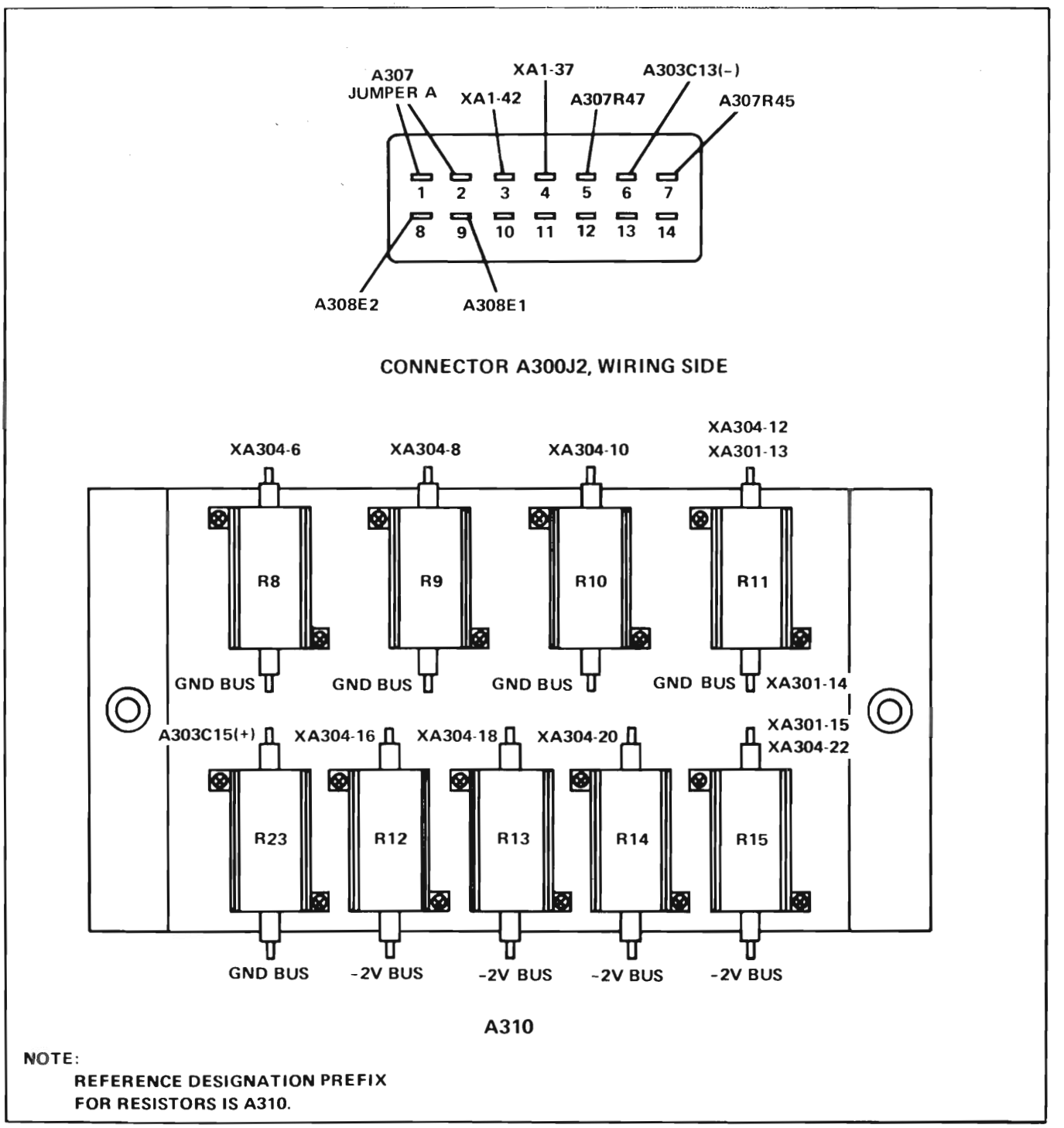


Figure 7-30. A309 Component Board Assembly (02116-63240), Parts Location and Connection Diagram

Table 7-67. A310 Component Board Assembly (02116-63241), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
R8 thru R15	0811-2078	Resistor, Fxd, ww, 0.15 ohms, 3%, 12W	28480	0811-2078
R23	0811-2648	Resistor, Fxd, ww, 5 ohms, 3%, 12.5W	28480	0811-2648



2107-36A

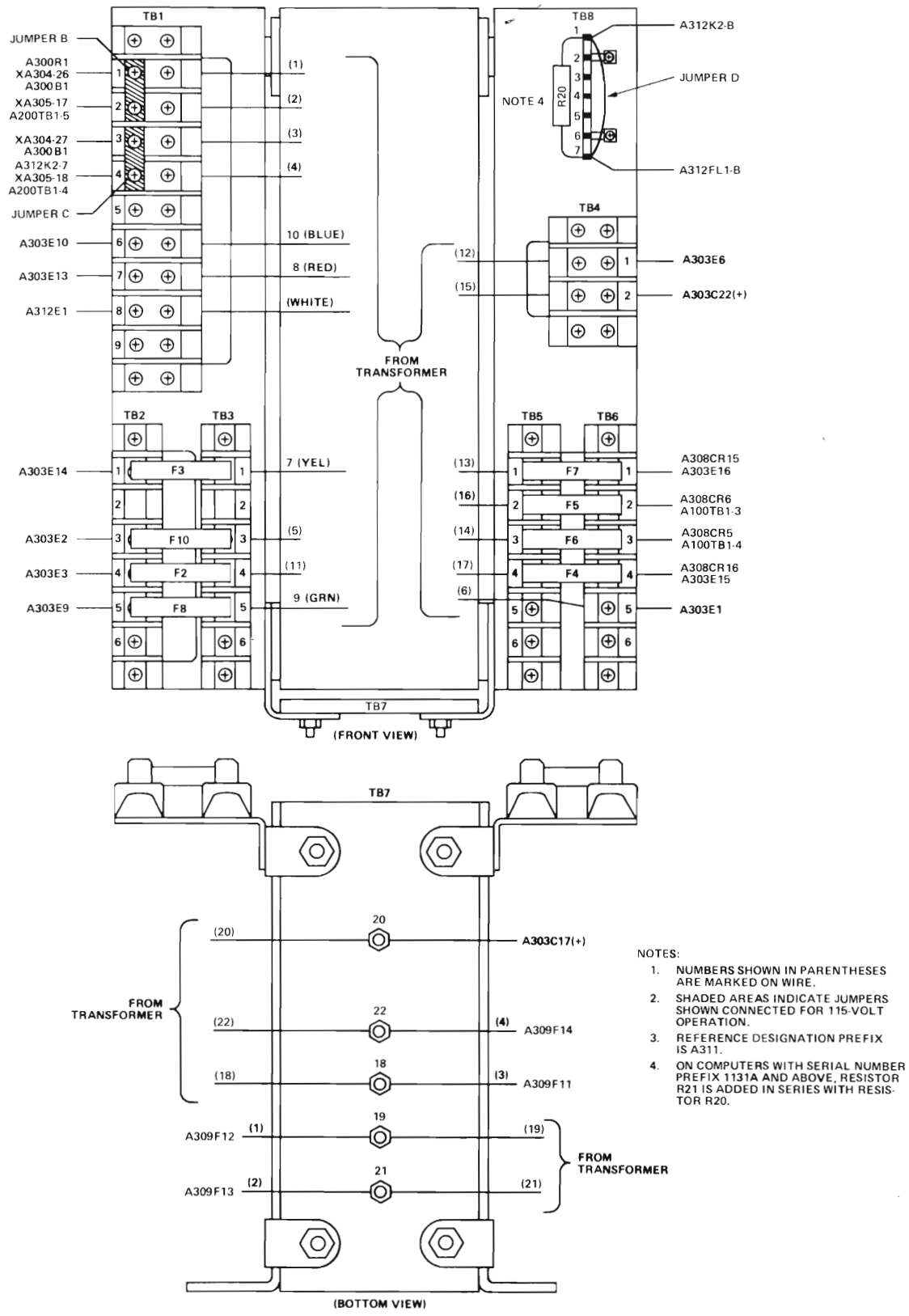
Figure 7-31. A310 Component Board Assembly (02116-63241) and Connector A300J2, Parts Location and Connection Diagram

Table 7-68. A311 Transformer Assembly (02116-63225), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
F2	2110-0013	Fuse, 3.2A, 125V, slow blow	00000	OBD
F3,8	2110-0044	Fuse, 0.3A, 250V, slow blow	00000	OBD
F4,7	2110-0035	Fuse, 8.0A, 250V, slow blow	00000	OBD
F5,6	2110-0025	Fuse, 15A, slow blow	00000	OBD
F10	2110-0014	Fuse, 4A, 125V, slow blow	00000	OBD
R20 ①	0811-2735	Resistor, Fxd, ww, 2500 ohms, 3%, 10W	28480	0811-2735
R20,21 ②	0764-0003	Resistor, Fxd, Met Ox, 3300 ohms, 5%, 2W	28480	0764-0003
T1	9100-1219	Transformer	28480	9100-1219
TB1	0360-1256	Terminal Board	00000	OBD
TB2,3,5,6	0360-1254	Terminal Board	00000	OBD
TB4	0360-1130	Terminal Board	00000	OBD
TB7	02116-0064	Terminal Block	28480	02116-0064
TB8	0360-1589	Terminal Block	28480	0360-1589

① Used on computers with serial number prefix below 1131A.

② First used on computers with serial number prefix 1131A.

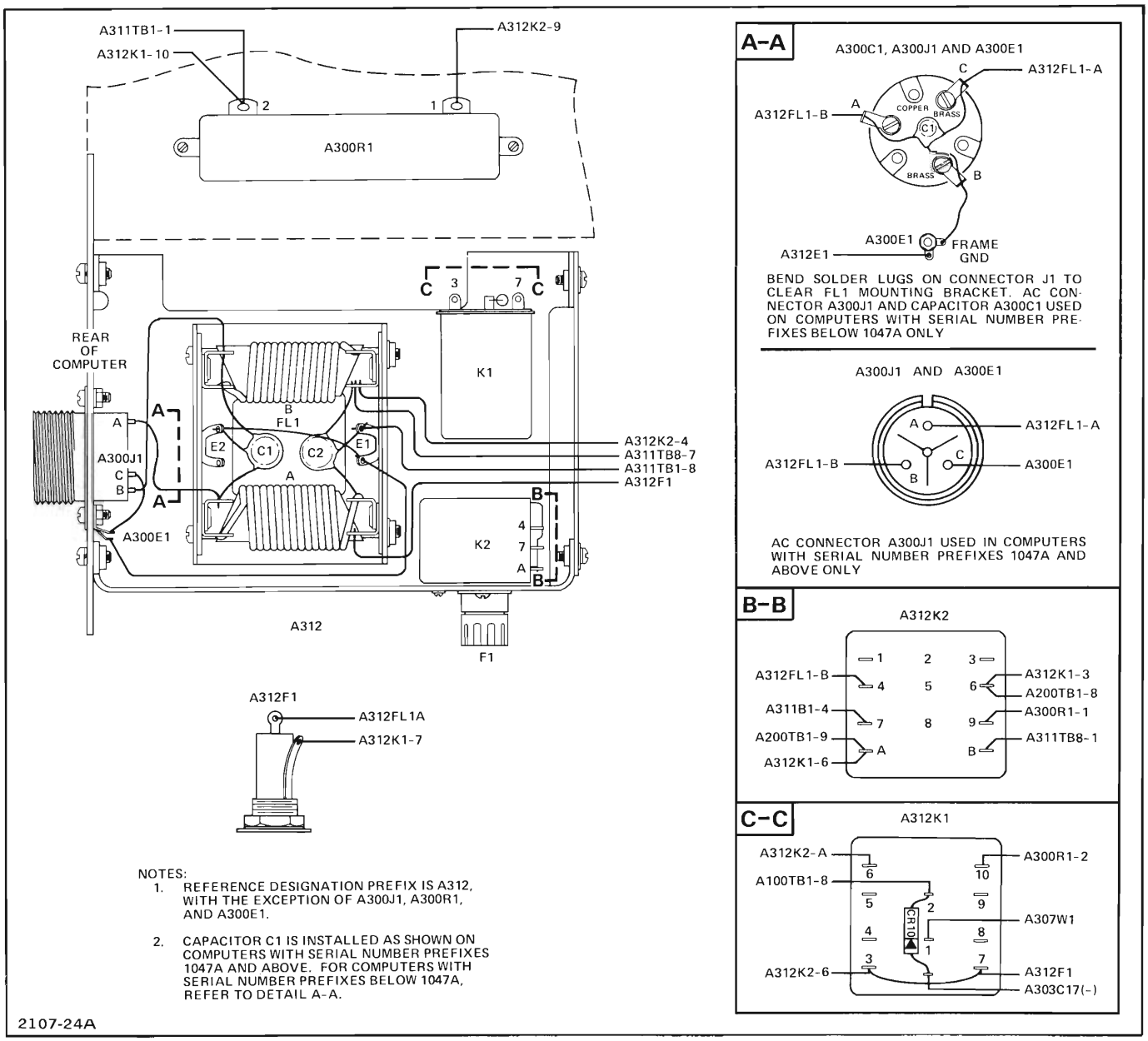


2107-37D

Figure 7-32. A311 Transformer Assembly (02116-63225), Parts Location and Connection Diagram

Table 7-69. A312 AC Input Section (02116-63228), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1A,1B,C2A,2B	0160-3043	Capacitor, Fxd, Cer, 2 x 0.005 uF, 20%, 250 VDCW	56289	29C147A-CHD
CR10	1901-0045	Diode, Si, 0.75A, 100 PIV	04713	SR1358-7
F1	2110-0327	Fuse, 15A, 250V, slow blow	00000	OBD
FL1	9100-1834	Line Filter, 20A, AC	28480	9100-1834
K1	0490-0372	Relay, 12 VDC 50-ohm coil	73096	WHV012D5-503
K2	0490-0892	Relay, 250V	28480	0490-0892
XF1	1400-0084	Fuse Holder	00000	OBD



NOTES:
1. REFERENCE DESIGNATION PREFIX IS A312, WITH THE EXCEPTION OF A300J1, A300R1, AND A300E1.
2. CAPACITOR C1 IS INSTALLED AS SHOWN ON COMPUTERS WITH SERIAL NUMBER PREFIXES 1047A AND ABOVE. FOR COMPUTERS WITH SERIAL NUMBER PREFIXES BELOW 1047A, REFER TO DETAIL A-A.

2107-24A

Figure 7-33. A312 AC Input Section, A300C1 Capacitor, A300J1 Connector, and A300R1 Resistor, Parts Location and Connection Diagram

Specifications, Transformer A311T1

XFMR WIRES	AC VOLTAGE (RMS)		MAXIMUM CURRENT (AMPS, DC)	WINDING RESISTANCE (OHMS)
	UNLOADED	LOADED		
1-3	115.0	115.0	– –	0.130 ± 10%
2-4	115.0	115.0	– –	0.150 ± 10%
5-6	8.9	8.5	4.0	0.032 ± 10%
7-8 (yellow-red)	37.6	36.0	0.1	1.448 ± 10%
9-10 (green-blue)	37.6	36.0	0.1	1.443 ± 10%
11-12	12.3	12.0	2.0	0.042 ± 10%
13-17	56.0	53.5	4.0	0.128 ± 10%
14-16	37.8	35.5	12.0	0.093 ± 10%
18-22	18.8	17.8	22.5	0.018 ± 10%
19-21	15.3	14.2	22.5	0.010 ± 10%

NOTES:

FOR SECONDARY WINDINGS, THE UNLOADED VOLTAGE IS THE OPEN CIRCUIT VOLTAGE (FUSE REMOVED). THE LOADED VOLTAGE IS FOR A FULLY LOADED SECONDARY (MAXIMUM DC CURRENT DRAWN FROM THE RECTIFIER). DEPENDING ON THE OPTIONAL DEVICES INSTALLED, SECONDARIES MAY NOT BE FULLY LOADED WHEN FUSE IS INSTALLED.

THE MAXIMUM CURRENT CITED IS THE DC CURRENT DRAWN FROM THE RECTIFIER.

Memory Supply Regulator Card A302 Typical Voltages
(See Note 9)

TEST POINT		DC VOLTAGE
Q50	Emitter	- 8.3V
	Base	- 9.0V
	Collector	-14.0V
Q51	Emitter	- 8.3V
	Base	- 9.1V
Q52	Emitter	-13.0V
Q53	Base	-11.0V
Q54A	Emitter	- 0.7V
	Base	- 0.020V
	Collector	+22.0V
Q55	Emitter	+21.4V
Q56	Base	+19.0V
Q57	Emitter	+ 0.62V
	Base	- 0.15V
	Collector	-22.0V
Q58	Emitter	+ 0.62V
Q59	Emitter	-21.0V
Q60	Base	-19.0V
A302-1 (+20V temp sense)		- 6.5V

Logic Supply Regulator Card A301 Typical Voltages
(See Note 9)

TEST POINT		DC VOLTAGE
Q30	Base	+ 4.5V
Q31	Base	+ 4.5V
Q32	Emitter	- 0.84V
Q33	Base	+ 0.39V
	Collector	- 1.6V
Q35	Base	+ 0.03V
Q37	Emitter	- 3.1V
Q38	Base	- 1.8V
	Collector	- 4.0V
Q39	Base	+ 0.61V
Q41	Emitter	+13.0V
Q42	Base	+11.0V
	Collector	+14.0V

Capacitor Board Assembly A303 Typical Voltages
(See Note 9)

TEST POINT	DC VOLTAGE
A303C14(-)	- 3.7V
A303C17(-)	- 5.7V
A303C19(-)	- 8.1V
A303C21(+)	+23.0V
A303C22(-)	-24.0V
A303C23(-)	-36.0V
A303C26(+)	+35.0V
A303E8	-84.0V
A303E12	+83.0V

Table 7-70. A501 Display Board Assembly (02116-6043), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
DS1 thru DS86	2140-0035	Lamp, Incandescent, 6.3V, 0.75A	71744	1775
S111 thru S113	3101-0973	Switch, Slide, DPDT, 125V, 0.5A, AC/DC	79727	8126-0016

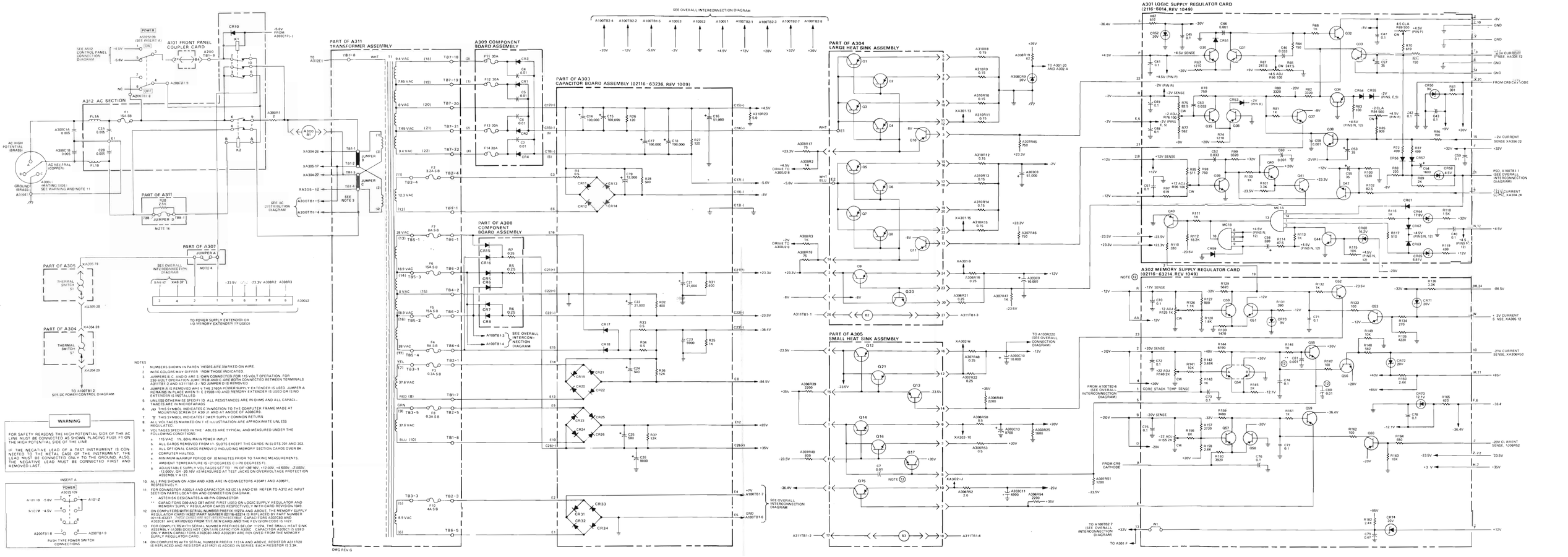
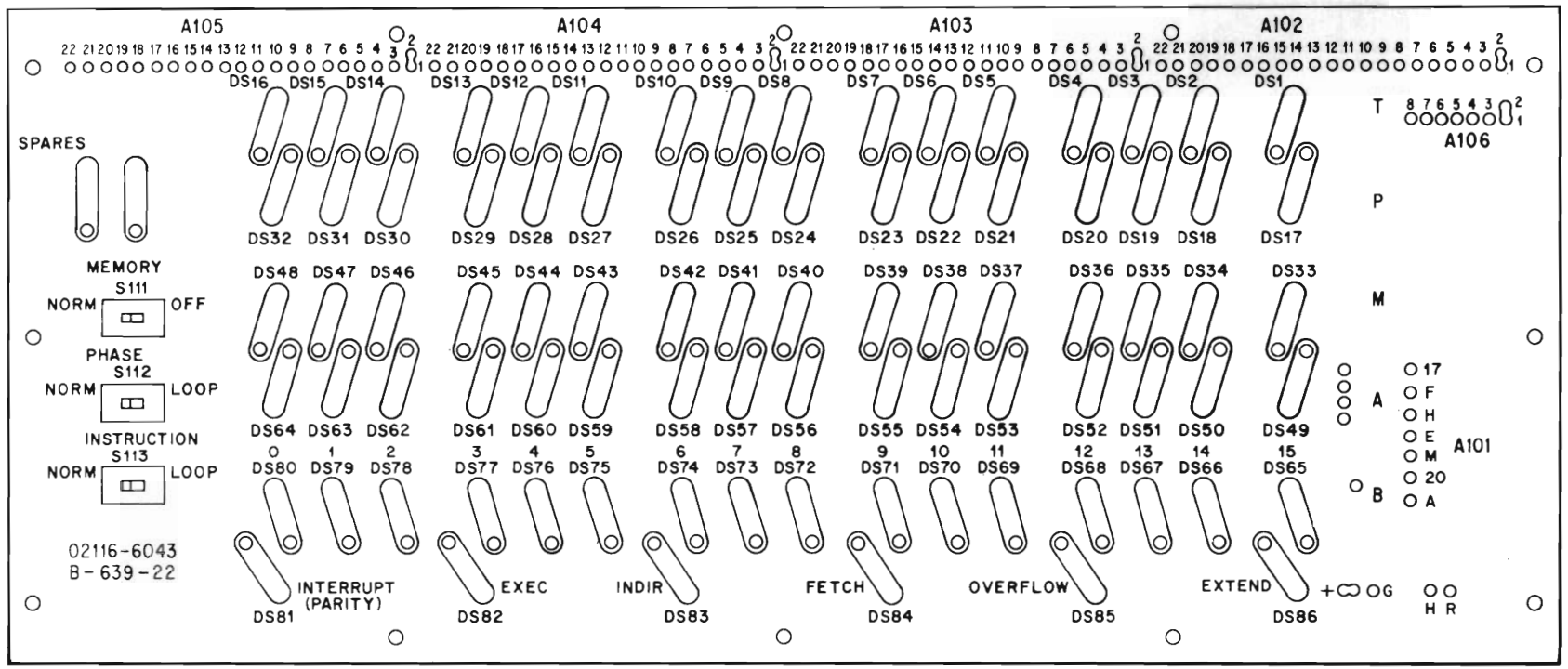


Figure 7-34. Power Supply Assembly (02116-63217) Schematic Diagram



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NOTES:

1. CONNECTIONS A101 THRU A106 ARE CABLE CONNECTIONS. REFER TO THE OVERALL INTERCONNECTION DIAGRAM AND TO THE DOOR ASSEMBLY SCHEMATIC DIAGRAM FOR FURTHER INFORMATION.

Figure 7-35. A501 Display Board Assembly (02116-6043), Parts Location Diagram

Table 7-71. A502 Control Panel Assembly, Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
DS106 thru DS108	2140-0035	Lamp, Incandescent, 6.3V, 0.75A	71744	1775
DS109††	2140-0035	Lamp, Incandescent, 6.3V, 0.75A	71744	1775
S1 thru S16	3101-1051	Switch, Toggle, spst, 125V, 3A	88140	8908K507
S100 thru S108	3101-0715	Switch, Lighted Pushbutton	28480	3101-0715
S109††	3101-0714	Switch, Lighted Pushbutton	28480	3101-0714
S109†	3101-0005	Switch, Toggle, dpdt, 125V, 6A	28480	3101-0005

† Applies to late model computers with serial prefix 980- only.
†† Applies to early model computers with serial prefix 980- only.

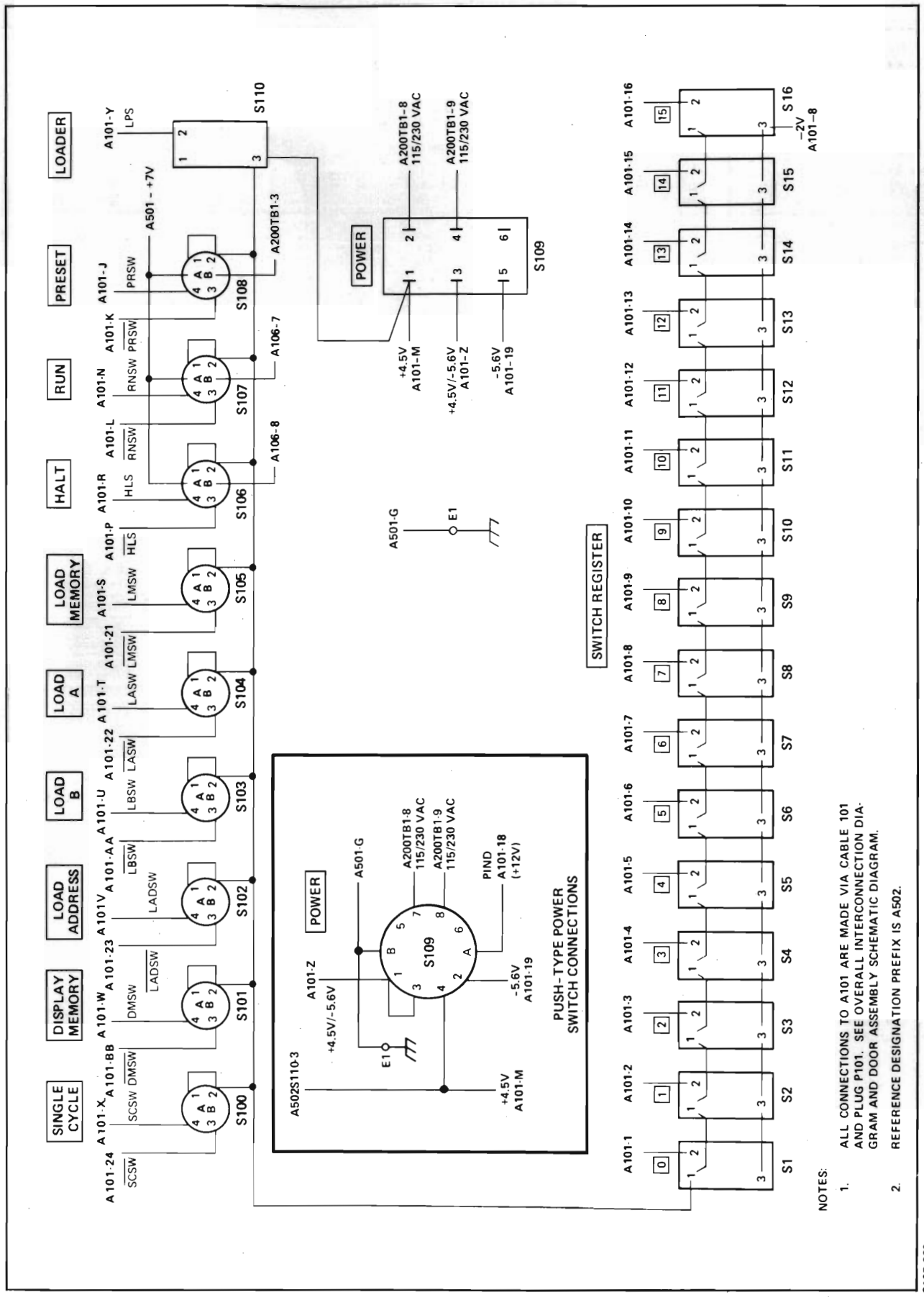


Figure 7-36. A502 Control Panel Assembly, Parts Location and Connection Diagram

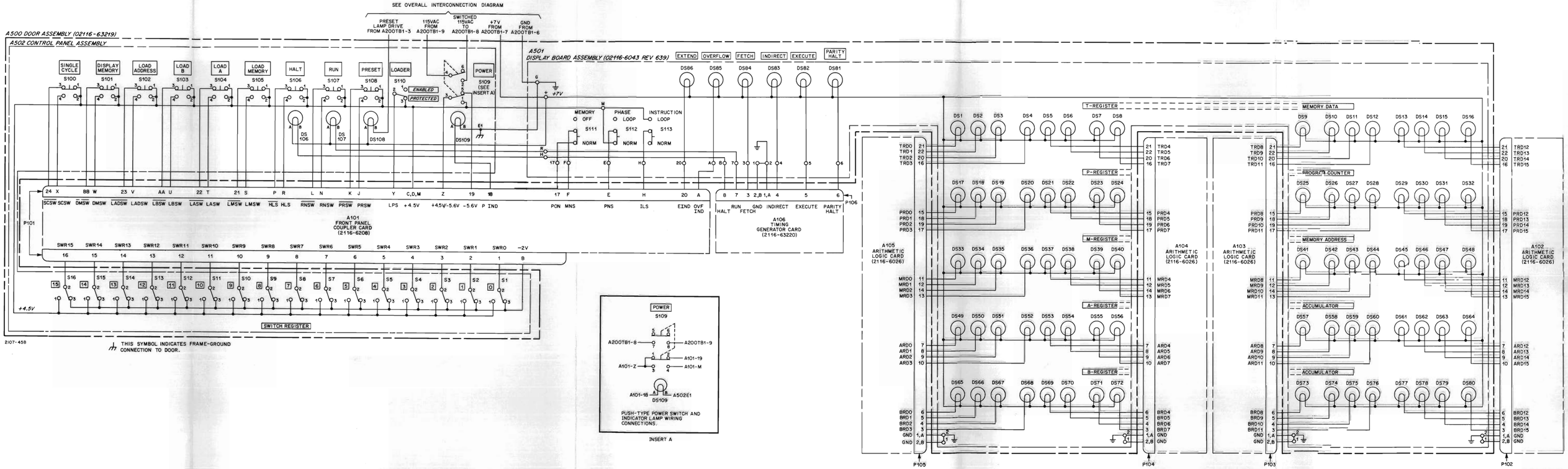


Figure 7-37. A500 Door Assembly (02116-63219), Schematic Diagram

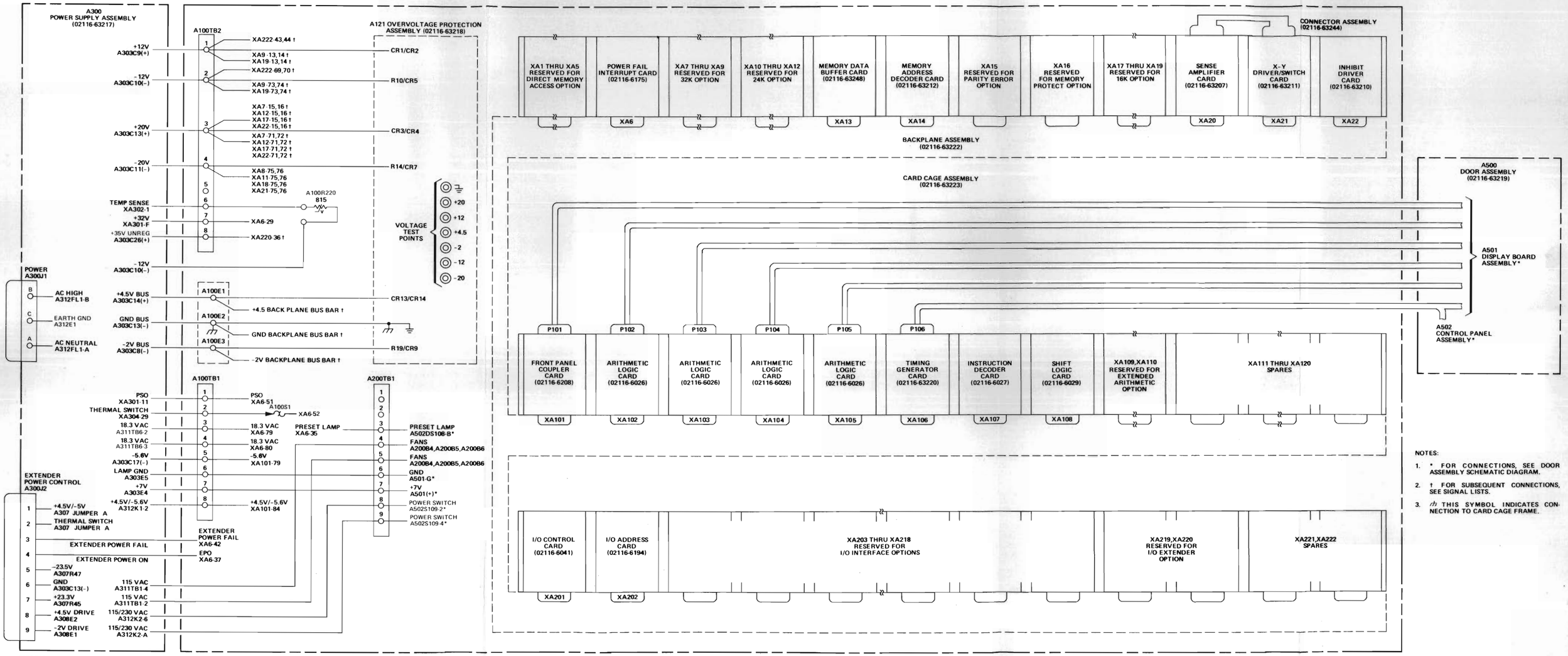


Figure 7-38. Overall Interconnection Diagram

APPENDIX A

BASIC LOGIC SYMBOLS

A-1. CATEGORIES OF LOGIC SYMBOL.

A-2. On logic diagrams in this manual, the three major categories of electronic logic element are distinguished by three basic types of symbol. These symbols are for the following circuits:

a. Gates.
b. Multivibrators.
c. Amplifiers.

A-3. The three symbols, and the variations of each type, are described in this appendix.

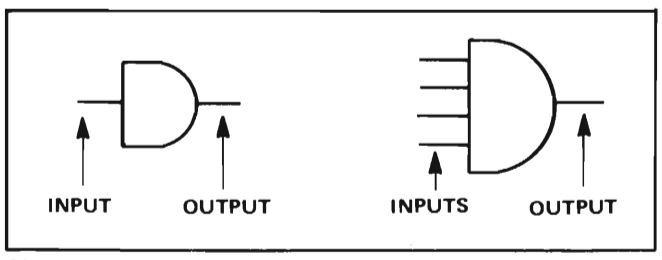
A-4. INVERSION.

A-5. Logical inversion is indicated by a dot at the input or output of a logic symbol. When the dot appears at the input of a gate or amplifier symbol, logical inversion of applied signals takes place. That is, true signals become false, and false signals become true, before application to the gate or amplifier. An inverting dot at the output of a gate or amplifier symbol indicates logical inversion of the output of the gate or amplifier.

A-6. In the case of multivibrators, an inverting dot at the input indicates that applied signals are effective when they are false, or in some cases when they are false-going. The lack of a dot at an input indicates that input signals are effective when true or true-going. The inverting dot is not used at the output of a multivibrator.

A-7. GATES.

A-8. A gate is a circuit which produces a logical-true or logical-false output when certain input conditions are met. The gate symbol has one or more inputs connected to the flat side of the symbol (figure A-1), and one output connected to the curved side. Since input and output are readily identifiable, the symbol may be shown left-facing, right-facing, or facing up or down.



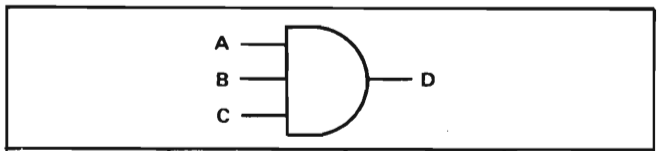
2039-25

Figure A-1. Gate Symbols

A-9. There are four basic types of gate: "and", "or", "nand", and "nor", each named for the logic function it performs. These gates are described below.

A-10. "AND" GATE.

A-11. The "and" gate (figure A-2) performs a logical "and" function. It produces a true output only when all inputs to the gate are true. To illustrate the functioning of this type of gate, the various states of a three-input "and" gate are shown in the truth table included in figure A-2.



A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

2107-94

Figure A-2. Three-Input "And" Gate, Logic Symbol and Truth Table

A-12. "OR" GATE.

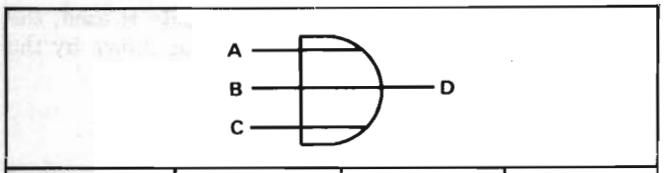
A-13. The "or" gate (figure A-3) performs a logical "or" function. It produces a true output when one or more inputs are true. The truth table in figure A-3 shows the various states of a three-input "or" gate.

A-14. "NAND" GATE.

A-15. The "nand" gate (figure A-4) is similar to the "and" gate described previously, except that its output is inverted. The gate generates a false output when all inputs are true. The various states of a three-input "nand" gate are shown in the truth table in figure A-4.

A-16. "NOR" GATE.

A-17. The "nor" gate (figure A-5) is identical with the "or" gate described previously, except that its output is inverted. The gate furnishes a false output when one or more inputs are true. The various states of a three-input "nor" gate are shown in the truth table in figure A-5.



A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Figure A-3. Three-Input "or" Gate, Logic Symbols and Truth Table

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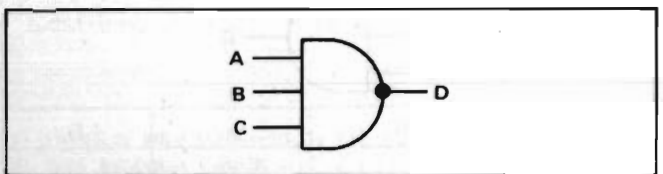

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure A-4. Three-Input "Nand" Gate, Logic Symbol and Truth Table

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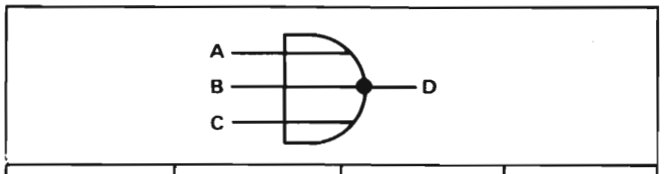
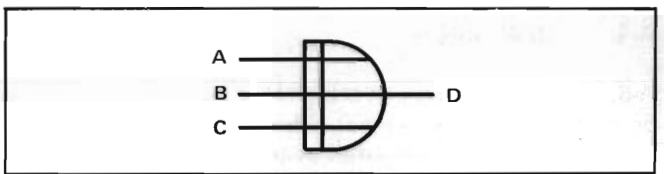


A	B	C	C
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure A-5. Three-Input "Nor" Gate, Logic Symbol and Truth Table

2107-96



A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure A-6. Three-Input Exclusive "Or" Gate, Logic Symbol and Truth Table

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A-18. EXCLUSIVE "OR" GATE.

A-19. The exclusive "or" gate (figure A-6) is a variation of the basic "or" gate. It has two or more input signals. The output is true when an odd number of inputs are true.

A-20. The truth table in figure A-6 shows the functioning of a three-input exclusive "or" gate.

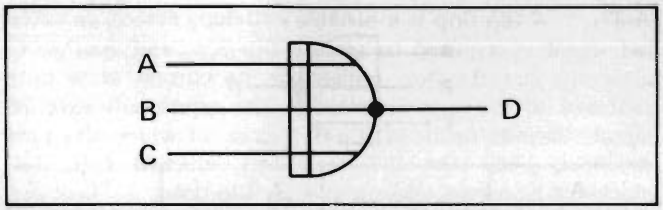
A-21. It will be noted that operation of the exclusive "or" gate is independent of the electrical polarity of the true and false conditions. The device therefore cannot be described as either positive-true or negative-true.

A-22. EXCLUSIVE "NOR" GATE.

A-23. The exclusive "nor" gate (figure A-7) is similar to the exclusive "or" gate, except that its output is inverted. The output is therefore true when an even number of inputs are true.

A-24. EXPANDER GATE.

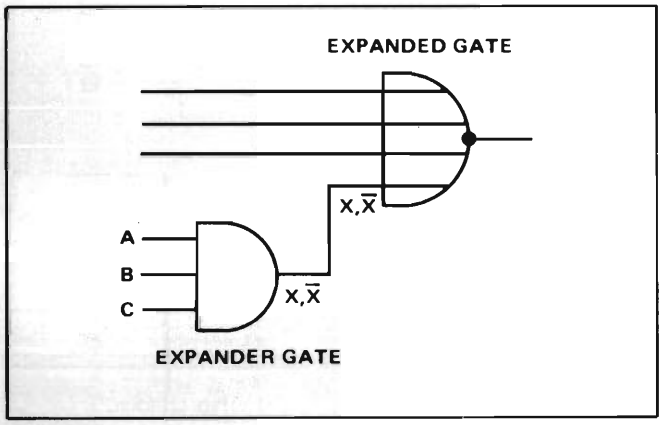
A-25. The expander gate provides a means for increasing the number of inputs to a gate. Figure A-8 shows a simplified method of illustrating this type of gate, and figure A-9 shows the actual connections between the gates involved. The X and $\overline{X}$ outputs of the expander gate are not logical



2107-76

Figure A-7. Three-Input Exclusive "Nor" Gate, Logic Symbol

opposites, but they do carry a voltage differential with respect to each other. When one or more inputs to the expander gate are false, there is a voltage difference of a few volts between X and $\overline{X}$. When all inputs to the expander gate are true, the voltage difference decreases; the two outputs of the expander then act as a true input to the expanded gate. The actual output-voltage differential of the expander gate depends on the type used.



2039-30

Figure A-8. Simplified Expander Gate, Logic Symbol

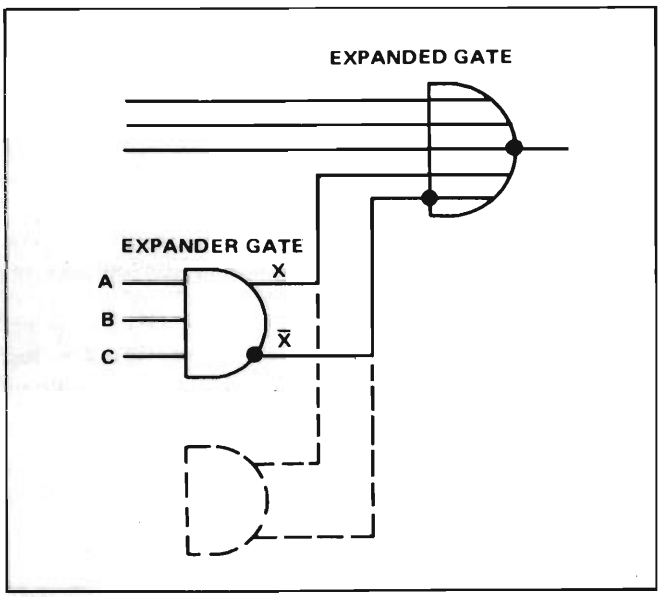


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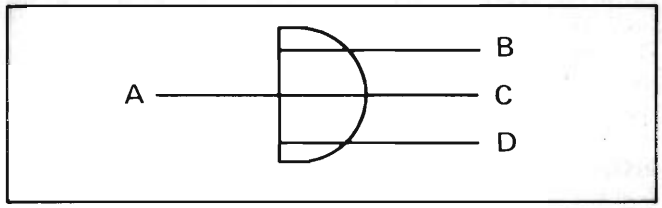
Figure A-9. Actual Expander Gate, Logic Symbol

A-26. When more than one expander gate is used, the gate outputs are connected as in parallel, as shown by the dashed lines in figure A-9.

A-27. ENCODING GATE.

A-28. The encoding gate (figure A-10) has one input and multiple outputs. Assuming no inverting dot at input A to the symbol, when the input is true all outputs (B, C, and D) are true. When the input is false, the outputs are either true or false, in accordance with the state of the logic element to which each is connected.

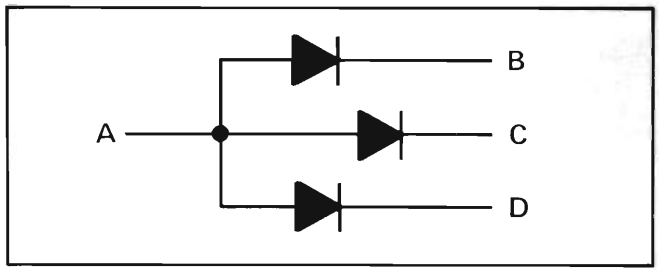


2107-77

Figure A-10. Three-Input Encoding Gate, Logic Symbol

A-29. A typical circuit for an encoding gate is shown in figure A-11. With A positive, all diodes conduct and all outputs are clamped positive. With A negative, each diode is practically an open circuit, and points B, C, and D assume the voltage level of the circuit to which each is connected.

A-30. If there is an inverting dot at A on the logic symbol, when the input is false all outputs are false. When the input is true, each input assumes the state of the logic element to which it is connected.



2107-98

Figure A-11. Circuit of Typical Encoding Gate

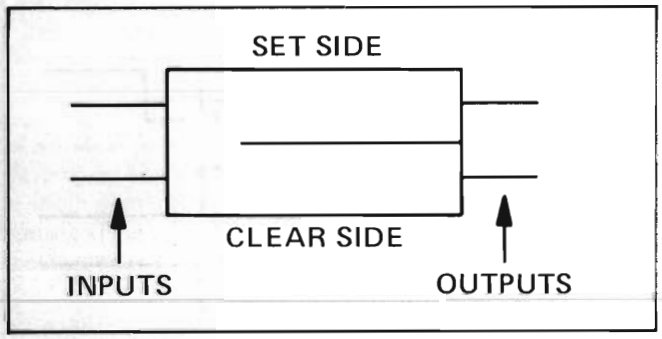
A-31. MULTIVIBRATORS.

A-32. The multivibrators described here are of four main types: flip-flops, Schmitt trigger circuits, one-shot multivibrators, and free-running multivibrators. All furnish a binary output. However, unlike gate circuits, the duration of a multivibrator output signal is not dependent on the duration of an input signal.

A-33. Although there is a logic symbol for each type of multivibrator, these circuits do not perform a logic function. Rather, they perform time-related electrical operations essential to computer functioning. To elaborate, there

are only two logic operators in Boolean algebra; these indicate the "and" and "or" function in this type of algebra, and correspond to "and" and "or" operations in a computer. There is no Boolean operator corresponding to the function performed by a multivibrator. Multivibrator output signals can be represented as terms in a Boolean equation, but they are present as variables, not as logic operators.

A-34. The basic logic symbol for a multivibrator is a rectangle (figure A-12). Letters in the symbol indicate the type of multivibrator. The rectangle is divided horizontally, with the upper portion representing the "set side" of the unit, and the lower portion representing the "clear side". The multivibrator is "set" when the output from the set side is true. It is "clear" or "reset" when the output from the clear side is true. To avoid confusion, the symbol is always oriented as shown in figure A-12. Inputs are on the left, outputs on the right.

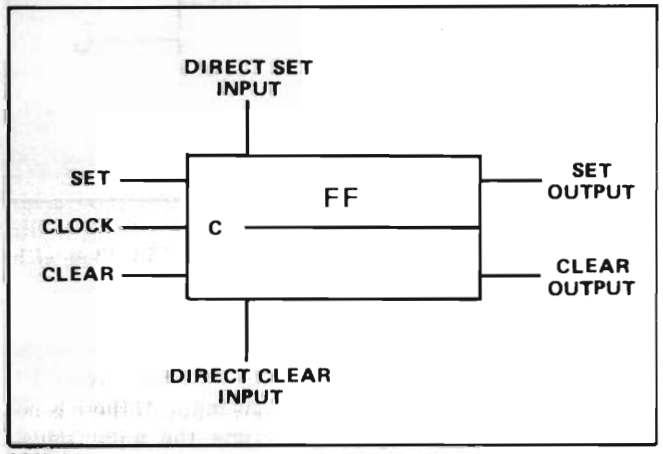


2107-85

Figure A-12. Basic Logic Symbol for Multivibrator

A-35. FLIP—FLOP.

A-36. The symbol for a flip-flop is shown in figure A-13. The letters "FF", preceded by the name of the flip-flop, distinguish this symbol from other types of multivibrator. Additional identification, described later, identifies the particular type of flip-flop among the seven types.

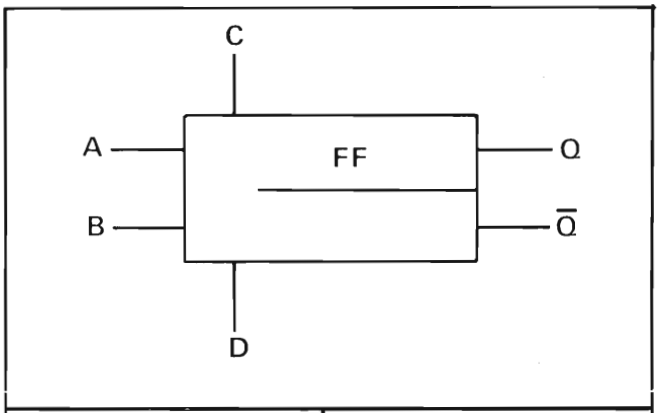


2039-33

Figure A-13. Flip-Flop Logic Symbol (General)

A-37. A flip-flop is a bistable switching device; an external signal is required to set the flip-flop, and another to clear it. The flip-flop remains in its current state until switched to the opposite state by the appropriate external signal. Various forms of flip-flop exist, of which seven are described here: the R-S (reset-set), clocked R-S, J-K, clocked J-K, toggle, latch, and delay flip-flops.

A-38. R-S FLIP-FLOP. The symbol for the R-S flip-flop (figure A-14) can be recognized by the fact that there is no information in the symbol identifying it as one of the other six types. The R-S flip-flop has a minimum of two input terminals (A and B in figure A-14) and one or two output terminals Q and $\overline{Q}$. One or two additional input terminals, C and D, may be used.



Input		Output	
A	B	Q	$\overline{Q}$
0	0	No change	
1	0	1	0
0	1	0	1
1	1	1	1

2107-87

Figure A-14. R-S Flip-Flop, Logic Symbol and State Table

A-39. The R-S flip-flop is set by a true input at A (assuming no inverting dot at this point). It can also be set by a true input at C, if this input terminal is present. The A and C inputs "or" together. The flip-flop is cleared by a true input at B or D; these also "or" together. Figure A-14 includes a state table, showing the flip-flop outputs resulting from various input conditions.

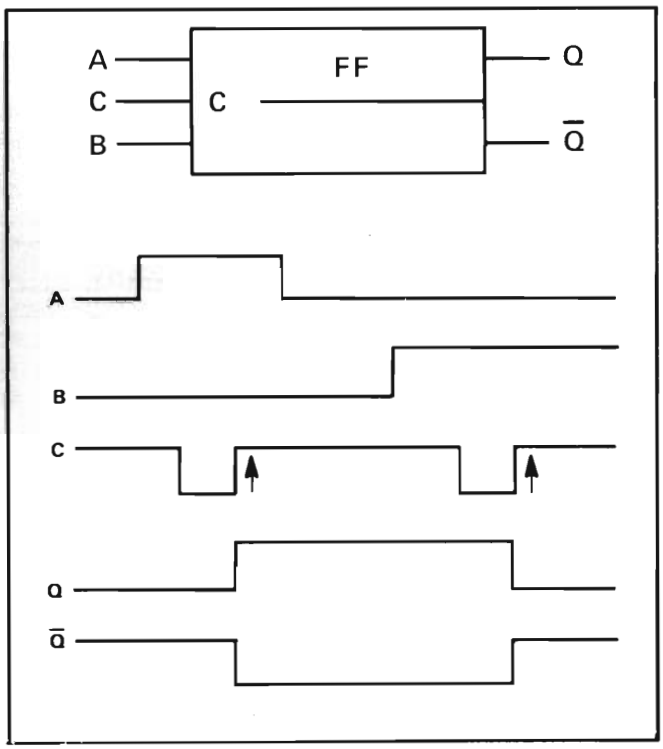
A-40. An inverting dot at any input to the flip-flop indicates that a false signal is required to change the state of the flip-flop.

A-41. After being set or cleared, the R-S flip-flop remains in that condition after termination of the set or clear pulse.

A-42. If the flip-flop is either set or clear and it receives an input to place it in the existing state, no change takes place in the flip-flop output signals.

A-43. Simultaneous set and clear input signals normally are not permitted, and circuit design usually prevents occurrence of this condition at a time when the flip-flop outputs are used. If simultaneous set and clear inputs are received, both outputs of the flip-flop are true for the duration of the simultaneous inputs. The eventual state of the flip-flop is determined by the input that remains longest in the activating condition.

A-44. CLOCKED R-S FLIP-FLOP. This flip-flop is similar to the R-S flip-flop, but it has a clock pulse input (figure A-15). The logic symbol can be recognized by the letter "C" at this input terminal. At the true-going transition of the clock pulse, the flip-flop becomes set if input A is true, or it becomes clear if input B is true (assuming no inverting dot at the clock pulse input terminal). If inputs A and B are both false at the transition of the clock pulse, the flip-flop does not change state. It is not permissible that A and B both be true when true-going clock pulse transition takes place.

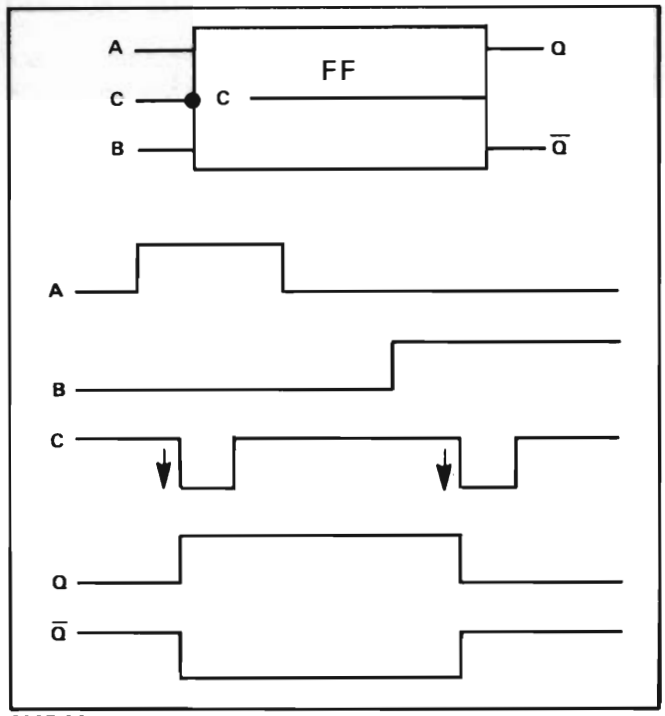


2107-80

Figure A-15. Clocked R-S Flip-Flop, Logic Symbol and Switching Waveforms

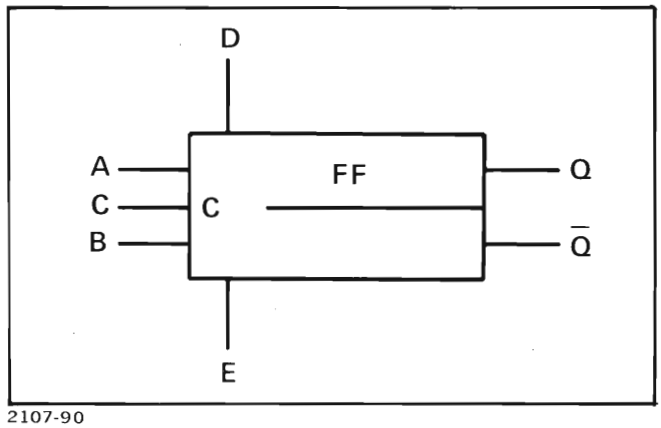
A-45. When the clocked R-S flip-flop has an inverting dot at the clock pulse input (figure A-16), the false-going transition of the clock pulse is the transition that is effective in setting or clearing the flip-flop.

A-46. In some cases the clocked R-S flip-flop has a set and clear input at the top and bottom of the logic symbol (inputs D and E, figure A-17). These inputs are independent of the clock pulse, and are referred to as the direct set and direct clear inputs. They function as a result of a true or false level, rather than a true- or false-going transition. An inverting dot at the direct set or clear input indicates that a false level is required to set or clear the flip-flop. No dot indicates that a true level is required. The direct set and clear input is also used on other types of flip-flop.



2107-99

Figure A-16. R-S Flip-Flop with Inverted Clock Input, Logic Symbol and Switching Waveforms

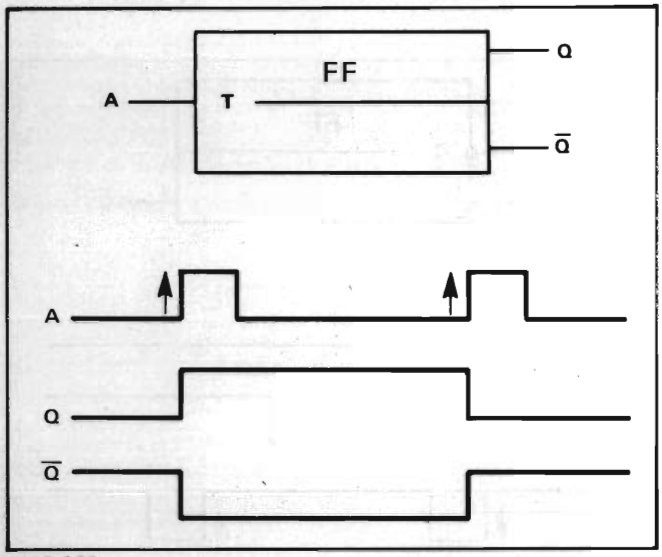


2107-90

Figure A-17. Logic Symbol for Clocked R-S Flip-Flop with Direct Set and Direct Clear Inputs

A-47. TOGGLE FLIP-FLOP. The symbol for the toggle flip-flop (figure A-18) can be recognized by the letter "T" in the symbol. This flip-flop has a single input. If there is no inverting dot at this input, each time the input signal becomes true, outputs Q and $\overline{Q}$ change state. Since two input pulses are required to produce one complete cycle of

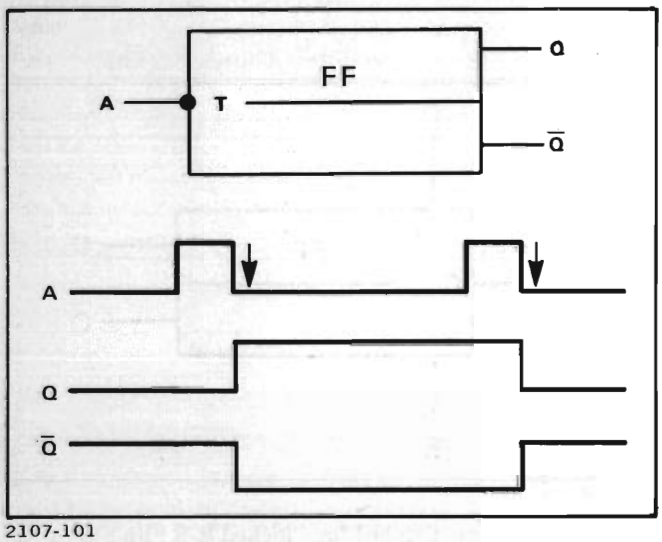
the output, the toggle flip-flop functions as a divide-by-two element, and is commonly used in groups in counting circuits, with the output of one flip-flop driving the next. Figure A-18 shows the switching waveforms for one flip-flop.



2107-100

Figure A-18. Toggle Flip-Flop, Logic Symbol and Switching Waveforms

A-48. If a toggle flip-flop symbol has an inverting dot at the input connection, the flip-flop changes state at the false-going transition of the input. The symbol and waveforms for this type of flip-flop are shown in figure A-19.

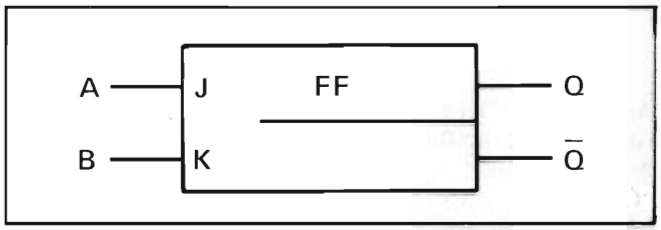


2107-101

Figure A-19. Toggle Flip-Flop with Inverted Input, Logic Symbol and Switching Waveforms

A-49. J-K FLIP-FLOP. The J-K flip-flop (figure A-20) is similar to the R-S flip-flop described earlier. However, the set and clear inputs of the J-K flip-flop can be permitted to simultaneously attempt to operate the flip-flop. When this occurs, the signal received first operates the flip-flop, and the other has no effect.

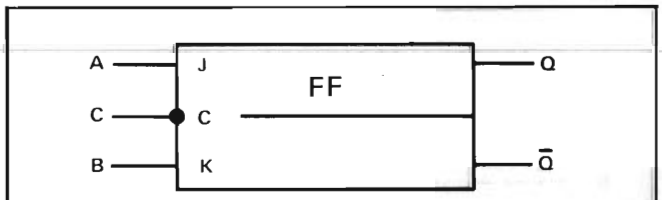
A-50. The state table for the J-K flip-flop is the same as for the unclocked R-S flip-flop.



2107-93

Figure A-20. J-K Flip-Flop, Logic Symbol

A-51. CLOCKED J-K FLIP-FLOP. The clocked J-K flip-flop (figure A-21) is similar to the clocked R-S flip-flop. However, simultaneous set and clear inputs to the J-K flip-flop are permissible. Under these conditions, the J-K flip-flop changes its state at the occurrence of each true-going clock pulse transition, assuming there is no inverting dot at the clock pulse input. With an inverting dot at the clock pulse input, the flip-flop changes state at the false-going clock pulse transition. When used with simultaneous set and clear inputs, the J-K flip-flop operates in a manner similar to the toggle flip-flop.



Input		Initial Output*		Final Output**	
A	B	Q	$\overline{Q}$	Q	$\overline{Q}$
1	1	0	1	1	0
1	1	1	0	0	1
0	0	Either		No change	
1	0	Either		1	0
0	1	Either		0	1

*Before clock pulse transition
**After clock pulse transition

2107-102

Figure A-21. Clocked J-K Flip-Flop, Logic Symbol and State Table

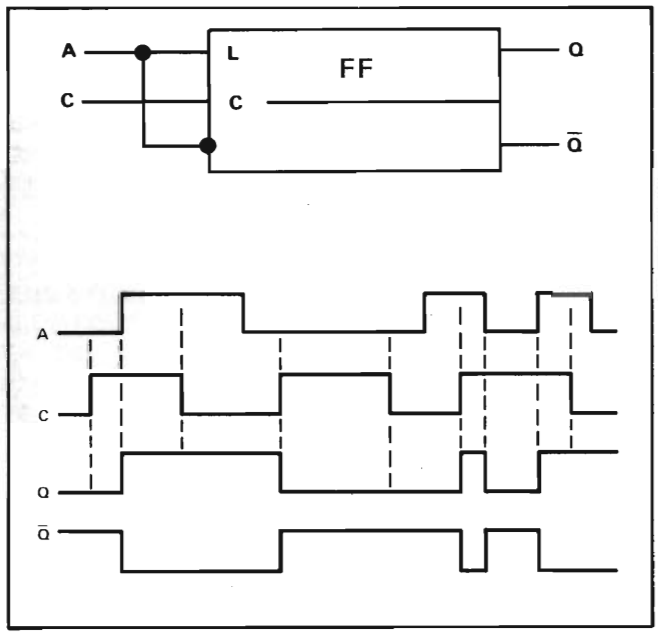
A-52. The J-K flip-flop can also be operated with one true input and one false input. It then functions in the same manner as the clocked R-S flip-flop.

A-53. Figure A-21 includes a state table showing operation of the J-K flip-flop. Note that with both inputs true at the time of clock pulse transition, the final state of the

flip-flop (after clock pulse transition) depends on the state before the transition. With only one input true, the initial state of the flip-flop is immaterial.

A-54. In some cases the J-K flip-flop consists of two separate flip-flops, with the output of one applied to the input of the other. Usually, a single flip-flop logic symbol is used to illustrate this circuit. The clock pulse inverting dot, or the lack of it, indicates the clock pulse transition that affects the output flip-flop of the pair.

A-55. LATCHING FLIP-FLOP. The latching flip-flop (figure A-22) can be recognized by the letter "L" in the symbol. The flip-flop has a clock input and a single signal input. Although the logic symbol shows two input-signal connections to the flip-flop, these separate inside the integrated circuit container from a single input to the unit. After separation, one input is inverted (indicated by the inverting dot) before application to the flip-flop proper.



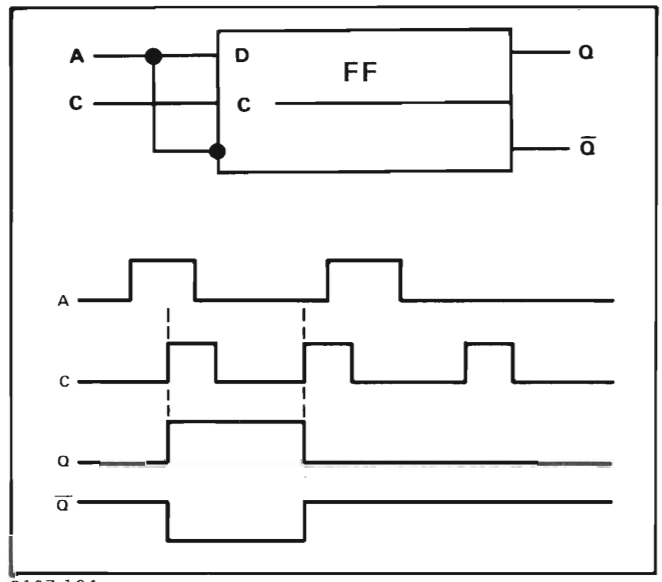
2107-103

Figure A-22. Latching Flip-Flop, Logic Symbol and Switching Waveforms

A-56. The set input is responsive to true signal levels at A (figure A-22), and the clear input is responsive to false signal levels at A. If there is no inverting dot at the clock input, this response takes place when the clock pulse is true. While the clock pulse remains true, the outputs follow any changes in the logic level at A as these changes take place. When the clock pulse becomes false, the flip-flop retains its current state, and no longer responds to changes in the input signal.

A-57. If the clock input connection of a latching flip-flop has an inverting dot, the flip-flop responds to the input signal while the clock pulse is false.

A-58. DELAY FLIP-FLOP. The delay flip-flop (figure A-23) is identified by a letter "D" inside the flip-flop symbol. This type of flip-flop is similar to the latching flip-flop, except that it responds to the input signal only at the transition of the clock pulse. The delay flip-flop thus does not follow changes in the input signal as these changes take place.

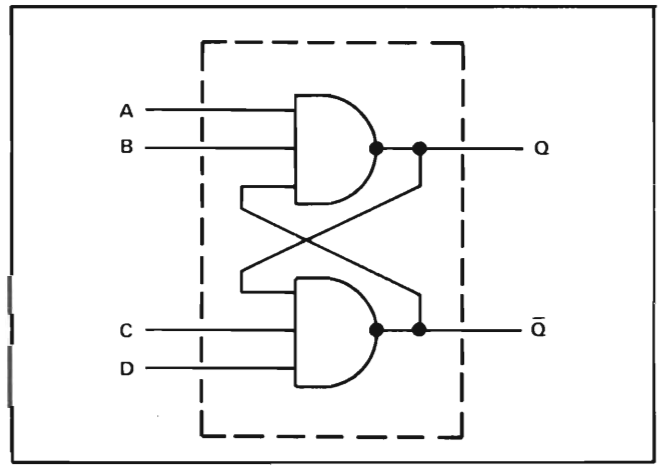


2107-104

Figure A-23. Delay Flip-Flop, Logic Symbol and Switching Waveforms

A-59. GATE FLIP-FLOP. The gate flip-flop is made up of two logic gates, connected as shown in figure A-24. The number of inputs to each gate can vary from that shown. The flip-flop can also be made up of two "nor" gates. The circuit may have a set output, a clear output, or both.

A-60. The gate flip-flop functions like an R-S flip-flop, but it has the advantage that it can "or" inputs without the addition of a separate "or" gate. Another reason for use of the gate flip-flop is that if two spare gates are available in



2039-48

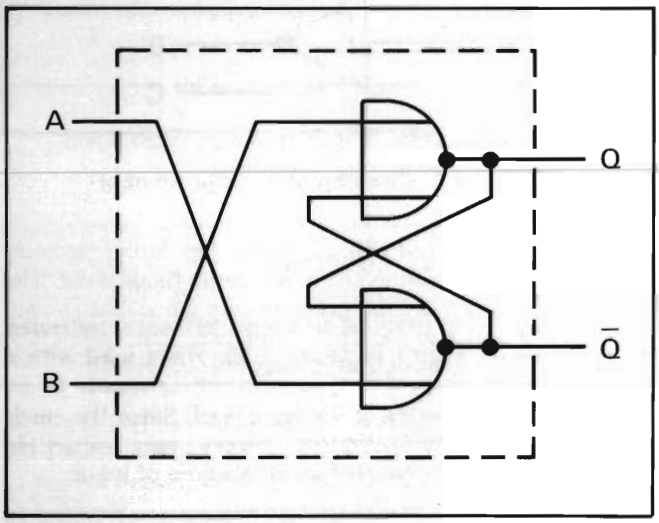
Figure A-24. "Nand" Gate Flip-Flop, Logic Symbol

integrated circuits on a circuit card, they can be employed as an R-S flip-flop without the need to add another integrated circuit to the card.

A-61. If the flip-flop is made up of two "nand" gates, as in figure A-24, it is set by a false input at either A or B. Similarly, it is cleared by a false input at C or D. When the flip-flop is in the quiescent state (not undergoing transition), the inputs at A, B, C, and D are all true.

A-62. A "nor" gate flip-flop is illustrated in figure A-25. In this type of flip-flop all inputs are false when the device is in the quiescent state. A true input at A sets the flip-flop, and a true input at B clears it. The inputs cross in the illustration in order to align the set and clear inputs with the set and clear outputs, respectively.

A-63. In most circuits using the "nand" or "nor" gate flip-flop, input signals are such that the flip-flop does not receive a set and clear input signal simultaneously. If circuit design does permit this to occur, both the set and the clear output are true for the duration of the condition. The eventual state of the flip-flop is determined by the input that remains longest in the activating condition.



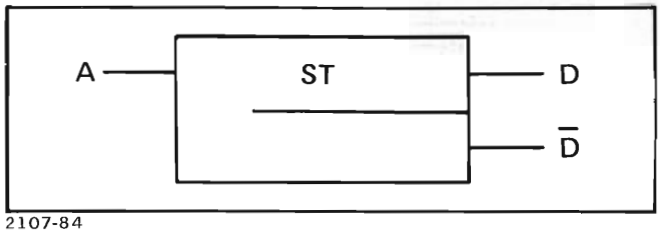
2107-86

Figure A-25. "Nor" Gate Flip-Flop, Logic Symbol

A-64. SCHMITT TRIGGER CIRCUIT.

A-65. The Schmitt trigger circuit (figure A-26) can be identified by the letters "ST" appearing in the logic-diagram symbol. Like the various types of flip-flop, this circuit is a two-state device which does not perform a Boolean function. It serves for level sensing or signal squaring. It may have a set output, a clear output, or both.

A-66. When the input voltage at A is below a certain level, the Schmitt trigger is in the clear state. When the input voltage rises above the reference level, the trigger assumes the set state. Circuit constants establish the reference level.



2107-84

Figure A-26. Schmitt Trigger Circuit, Logic Symbol

A-67. Switching between states takes place rapidly, and the Schmitt trigger is therefore useful for squaring signals that have poor rise and fall times. It can produce a square wave from a sine wave. Other uses of the Schmitt trigger are voltage level restoration, and detection of the rise of the input signal above a given level.

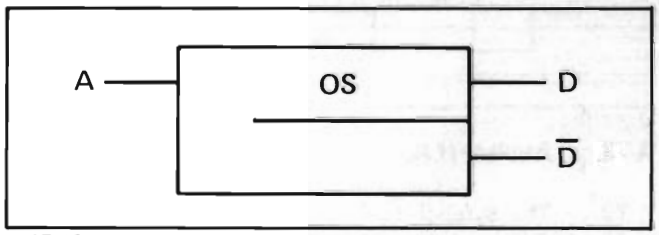
A-68. ONE-SHOT MULTIVIBRATOR.

A-69. The one-shot multivibrator (figure A-27) is a monostable switching element, used to produce a pulse of predetermined duration. The device is triggered into its unstable state by an external signal. It returns to the stable state after a time interval determined by circuit constants.

A-70. If there is no inverting dot at the input, triggering is accomplished when input A undergoes a true-going transition. If there is an inverting dot, a false-going transition is required.

A-71. The one-shot multivibrator may have a set output, a clear output, or both.

A-72. The symbol for the one-shot multivibrator is always drawn with the orientation shown in figure A-26, with the input at the left and the output or outputs at the right.



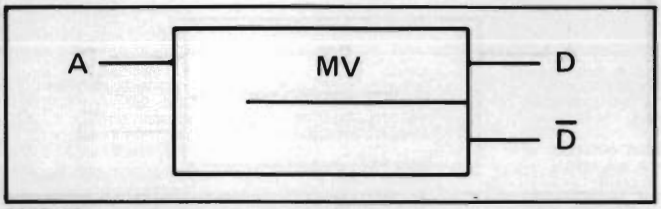
2107-81

Figure A-27. One-Shot Multivibrator, Logic Symbol

A-73. FREE-RUNNING MULTIVIBRATOR.

A-74. The free-running multivibrator (figure A-28) can be distinguished by the letters "MV" appearing in the symbol. This device produces trains of complementary pulses at D and $\overline{D}$. Pulse width is determined by circuit constants.

A-75. In some instances a control signal is applied to the free-running multivibrator. If there is no inverting dot at the signal input to the symbol, the multivibrator runs when



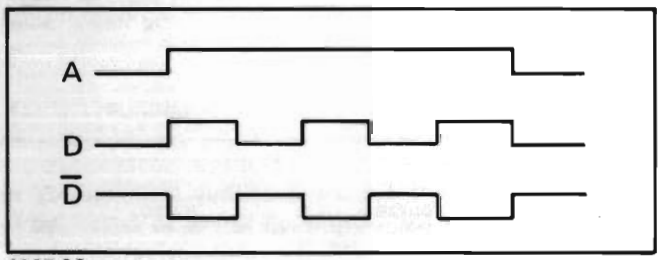
2107-82

Figure A-28. Free-Running Multivibrator, Logic Symbol

the control signal is true, and stops when the signal is false. When it is stopped, the multivibrator is in the clear condition. If there is an inverting dot at the control signal input, a false input is required to bring the multivibrator into operation. This type of multivibrator is in the set condition when it is not running.

A-76. Figure A-29 shows typical waveforms for a controlled free-running multivibrator that runs when the control signal is true. The true and false portions of the output waveforms need not be of equal duration.

A-77. The symbol for the free-running multivibrator is always drawn with the orientation shown in figure A-28, with the input (if any) at the left, and the output or outputs at the right.

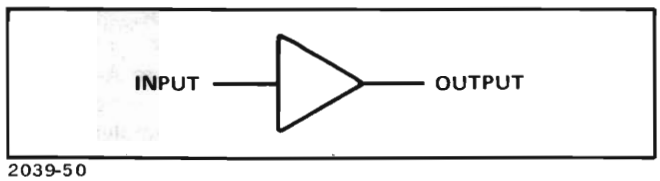


2107-83

Figure A-29. Input and Output Waveforms of Controlled Free-Running Multivibrator

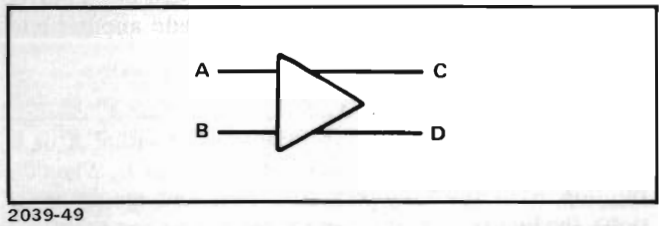
A-78. AMPLIFIER.

A-79. The symbol for an amplifier is shown in figure A-30. A differential amplifier is illustrated in figure A-31. Like gates, these symbols may be shown in any of four positions.



2039-50

Figure A-30. Amplifier, Logic Symbol



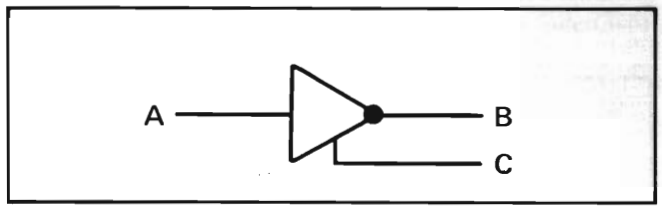
2039-49

Figure A-31. Differential Amplifier, Logic Symbol

A-80. In most instances, the amplifier symbol has a nonbinary input. A circuit which restores the voltage level of a binary input, or which furnishes a low-impedance output from a binary input, is indicated by a one-input gate symbol.

A-81. An inverting dot at the output of an amplifier symbol indicates that the amplifier inverts the input signal.

A-82. Figure A-32 is the symbol for a phase splitter.



2107-91

Figure A-32. Phase Splitter, Logic Symbol

A-83. CAPACITIVE COUPLING.

A-84. Capacitive coupling to a logic element is indicated by an arrow, as shown in figure A-33. When used with a gate or multivibrator, this type of coupling results in response only to a change in the logic level. Since the clock pulse input to multivibrators always uses capacitive coupling, the arrow is omitted from this type of input.

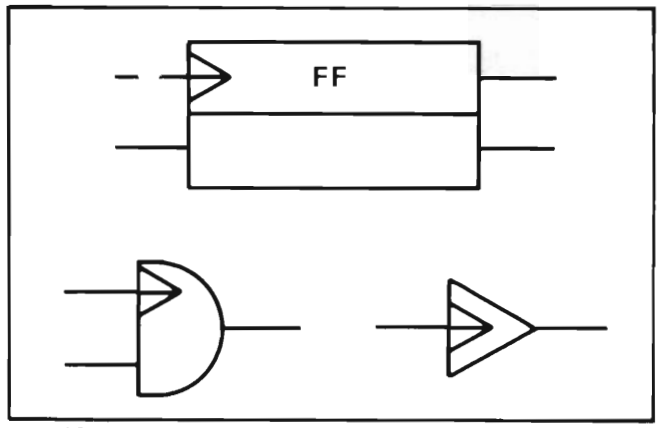


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Figure A-33. Capacitive Coupling

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ALPHABETICAL INDEX

for

VOLUME TWO

INSTALLATION AND MAINTENANCE MANUAL

MODEL 2116C
COMPUTER

This index applies to manual part number 02116-91756, printed JULY 1971.

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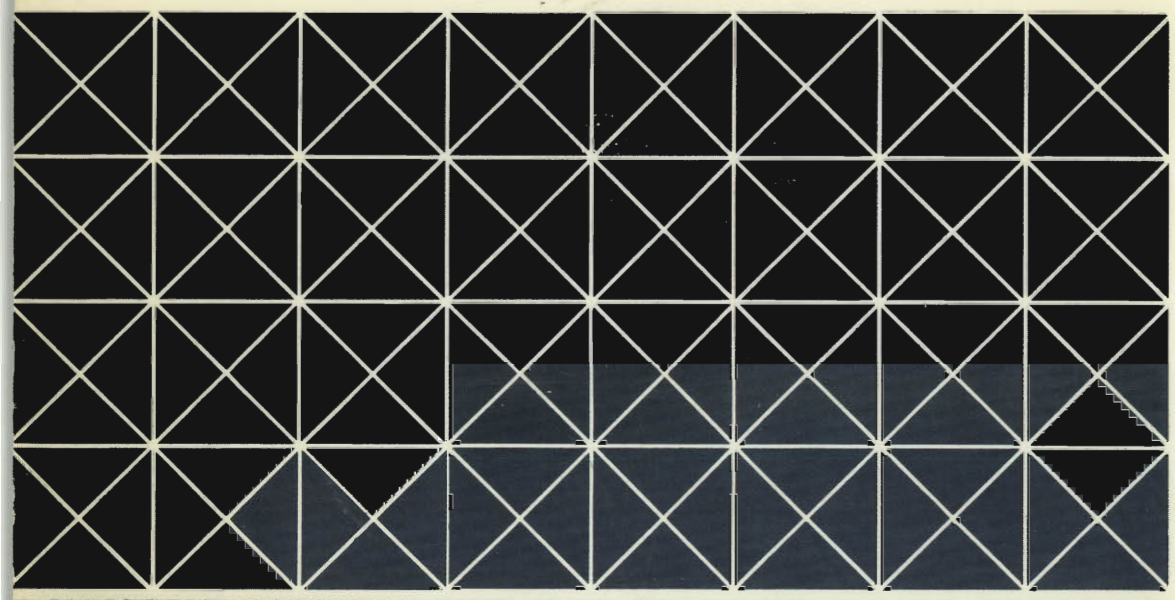

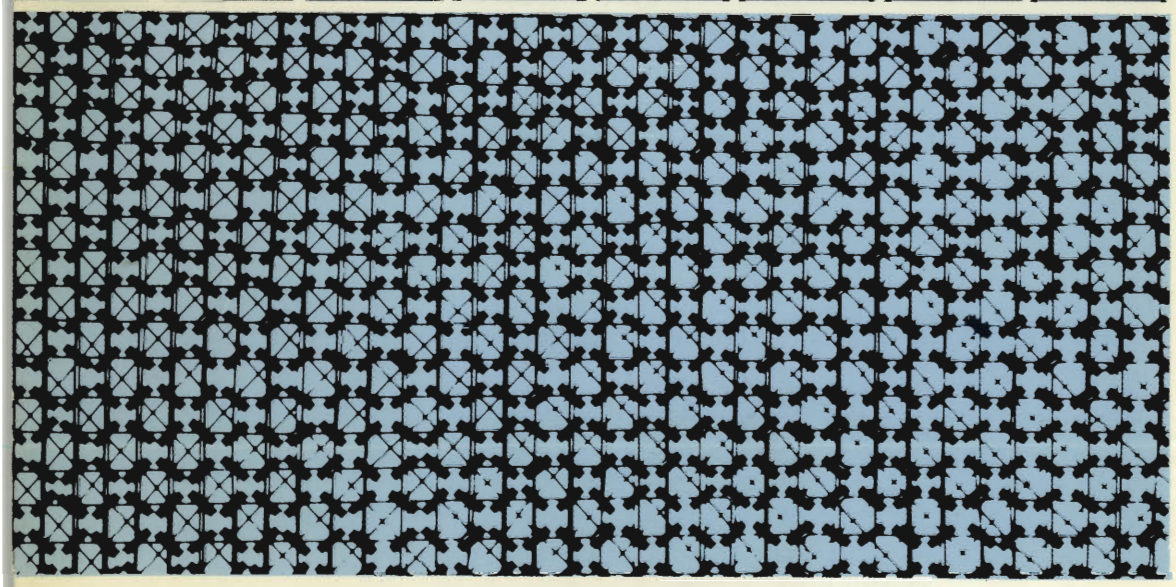

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